Explanation lecture 9 @ 1:51:40
Feb 8th, 2021

University of Windsor
Department of Electrical and Computer Engineering
ELEC 4430: Embedded System Design, Winter 2021
Instructor: Dr. Mohammed Khalid

$\frac{3}{7.5} = \frac{d}{15}$

Lab Project #1
Modeling, Simulation and Synthesis of a Data Buffering System for FPGAs
Due date: Monday, March 8, 2021

Using VHDL language, Intel Quartus Prime software and VHDL simulator, you should design and simulate a digital system for data buffering and processing whose I/O block diagram is given in a separate document. This hypothetical system can form a part of a bigger stream processing system in which data comes streaming in at a fast data rate, is buffered and processed and is output at a slower rate. Data stream coming in can represent video, audio, network traffic, etc. **This is an open-ended design and modeling project that requires you to think carefully about order of activating control signals, timing issues, using appropriate signals to represent the current state of the system, related assumptions, etc. Another challenging aspect is the utilization of two separate clock signals running at different frequencies, which is quite common in real world embedded systems.**

The system works as follows:

- The streaming data comes into the system on *DIN* at the clock frequency (rate) of *iclk*. The data is buffered (stored) and output on *DOUT* at the clock frequency (rate) of *oclk*. **Assume that the frequency of *iclk* is four times the frequency of *oclk*.** $\frac{iclk}{4} = dck$
- There are three 8 X 8 FIFO buffers inside this system that are used to store data coming in at a fast rate and then send it out at a slower rate. They are labelled as: FIFO 1, FIFO 2, FIFO 3.
- The *reset* input when active (logic 1) takes the system to its initial state.
- Note that the sender system sends data to the data buffering system using *iclk*. The receiver system receives data from the data buffering system using *oclk*.
- When any of the three FIFO buffers are empty, the *ready_to_fill* output is set to 1 for one clock cycle. The sender system sets *fill_fifo* input to 1 for one clock cycle followed by sending 8 data bytes in the subsequent clock cycles. Once the 8 data bytes are filled in an available FIFO, the fill_done output is set to 1 for one clock cycle. The FIFOs are always filled and emptied in the following order: FIFO 1, FIFO 2, FIFO 3.
- When any of the three FIFO buffers are full, the *ready_to_empty* output is set to 1 for one clock cycle. The receiver system sets *empty_fifo* input to 1 for one clock cycle. The *start_empty* output is set to 1 for one clock cycle followed by sending 8 data bytes in the subsequent clock cycles. The FIFOs are always filled and emptied in the following order: FIFO 1, FIFO 2, FIFO 3.
- **Note that sending and receiving of data may be done in parallel. This should work correctly in your modeling and simulation.**
- You can think of your model as two concurrently running subsystems: one for receiving data on *DIN* at the rate of *iclk* and the other for sending out data on *DOUT* at the rate of *oclk*. Each of these can be modeled using an ASM chart and a concurrently running

process.

- A good starting point will be design and modeling of the 8X8 FIFO that can be used to store the data. A sample I/O block diagram of the 8X8 FIFO is given in a separate document. Memory in VHDL can be easily modeled using a two-dimensional array of bits and a model can be developed to function as a FIFO of any size.
- **Each group must submit a project progress report every Monday starting on February 22.** The report should summarize the progress made towards completing the project. The VHDL code developed, ASM charts created, partial simulation results, etc. must be included in the progress report.
- **You must use testbench to test your design in the VHDL simulator (mandatory)**. The test data will be provided to you by your GA.
- **You must also synthesize your design using Quartus Prime synthesis tool and report FPGA resource usage summary. Your GA will guide you about obtaining resource usage report. Note that you cannot synthesize testbench.**
- You must start your design modeling with an ASM chart and you must submit this ASM chart in your project report.

Marking:
GA will check the results of simulation in ModelSim. Part marks will be given for all aspects.

- 35 percent for working simulation
- 35 percent for logical workflow
- 30 percent for communication and formatting

You must submit a project report, no more than 5 pages, with a brief description of how your ASM chart and your VHDL code is organized and how it works. A brief description of the testing process should also be given. You must submit the project report, the VHDL code and the simulation timing diagrams online on Blackboard.

Do not share your VHDL code with any person. Any copying of VHDL code from other students or from the Internet will result in zero points for one or both parties (those who copy and those who allow their code to be copied). More severe penalties may also apply. You can discuss this lab project with GAs. **Late submissions will be penalized and no submissions will be accepted after Monday March 15, 2021.**