SuperRes

Hardware Accelerated ML for Embedded Devices

1 Social Impact

The acceleration of super resolution imaging techniques brings revolutionary improvement in visual industry including gaming, filming, VR etc. This effectively enhances user's gaming experience by lowering the requirement for great bandwidth and internet. Moreover, while filmmakers using a high resolution camera, Image quality looks more realistic and engaging to the audience.

Motivation

With the advancement in machine learning techniques in recent years, machine learning algorithm based super resolution has been actively explored. Super resolution imaging is a technique that enhances the resolution of an image or video. In addition to enhancing image quality, we want to minimize the execution time of the upscaling algorithm, this is where FPGA comes into play. Since FPGAs are good for intensive data computation and static parallel tasks, it provides a faster approach for image processing.

2 Boost Economy

The development of image quality enhancing technologies effectively expands the visual technology market, and increases the public awareness and acceptance to niche technologies, such as VR devices. This is a key driver of economic growth of countries.

Embedded Devices

This application is implemented on PYNQ which can be easily used to design embedded systems with Zynq SOCs. Raspberry Pi embedded system is also a reasonable solution, since it has relatively low power consumption and outstanding computational power, whereas PYNQ is more suitable for system that need to process a large amount of data with high performance.

3 Environmentally Friendly

The accelerator design is based on the Xilinx PYNQ-Z1 board, which includes a Dual-core ARM Cortex-A9 processor alongside an FPGA. The reconfigurable feature of FPGA makes it more compatible with version updates and functional adjusting. Since the behaviour of FPGA can be flexibly and quickly changed, it normally lasts longer than ASICs, so that the number of waste chips can be reduced. The decreased hardware usage helps the relevant industry to battle against the shortage of chips.

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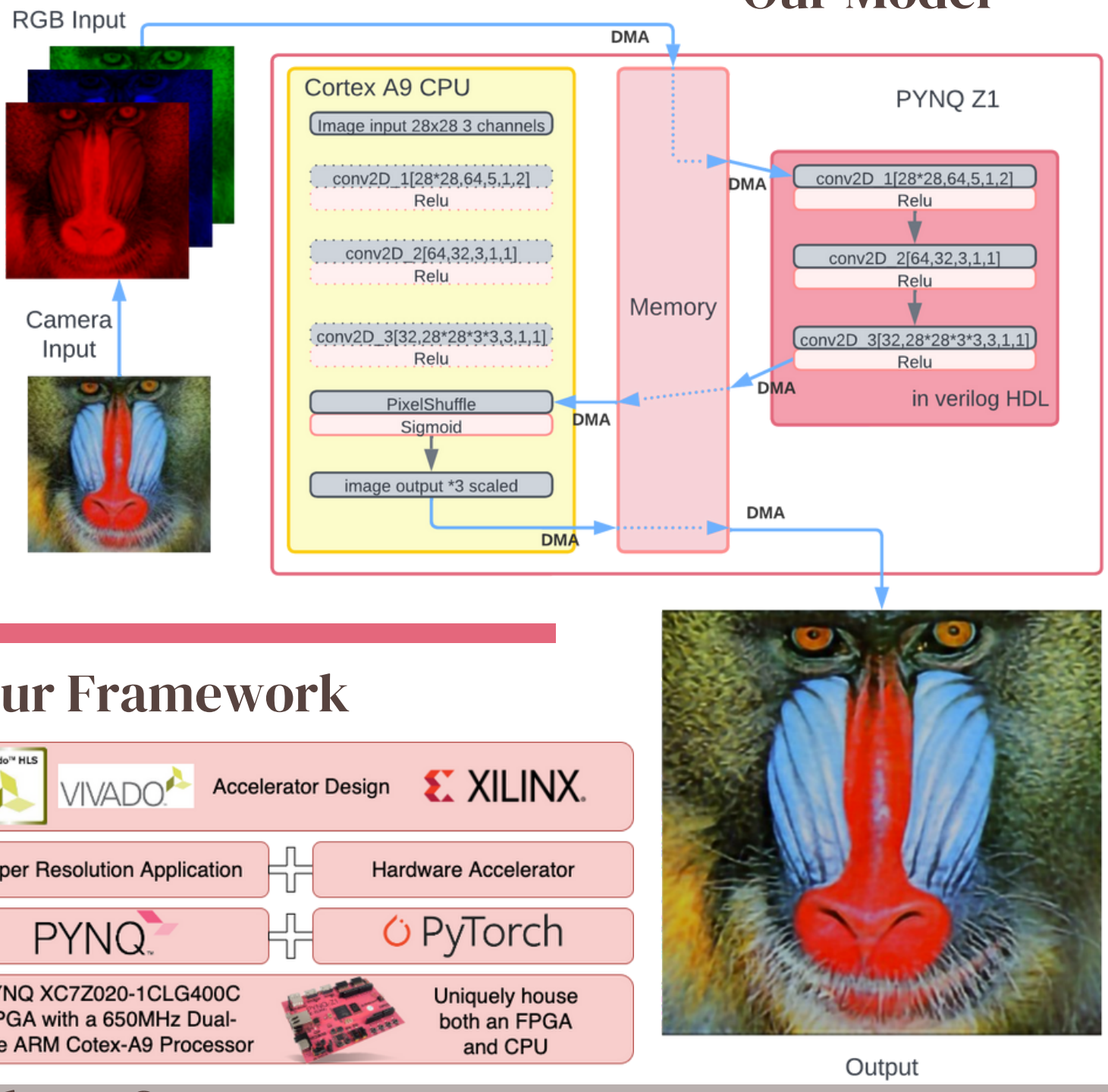
Our Approach

- Define requirements of the system
- Task partitioning to maximise performance of the system
- Customise hardware IPs for intensive data computation
- Ensure stable and efficient data transmission between FPGA and CPU
- Output the high resolution video on a display device

Our Model



Our Framework

Vivado™ HLS VIVADO Accelerator Design XILINX

Super Resolution Application + Hardware Accelerator

PYNQ + PyTorch

ZYNQ XC7Z020-1CLG400C FPGA with a 650MHz Dual-Core ARM Cotex-A9 Processor

Uniquely house both an FPGA and CPU

Output

Why us?

- Quantization aware training ensures the highest accuracy
- Since all the complex operations of ESPCN model are performed on low resolution, the computational and memory complexity is reduced, so its execution time is less than other models, and it is further reduced by pipelining on hardware
- The wide use of neural networks in the AI industry can benefit from our framework, especially the neuron IP and customizable interconnected layers

https://github.com/Terrortorpe/FPGA-Consultancy

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