There CPLD operates in 3 different modes:
1. CPU. Where the CPU is control. (PGM_MODE = H)
2. Peripheral Processing board is programming the EEPROM(PGM_MODE = L and JLINK_Mode = H)
3. Peripheral Processing board act like a J-LINK device (PGM_MODE = L and JLINK_Mode = L)

CPU. Where the CPU is control.
The Memory Map is valid.

Memory Map		
Peripheral	Description	Memory Address
INT_CTRL_CS	Interrupt Control	0x7FFE
PGR_CS	Rom Page Register	0x7FFF
PCS_CTRL_CS	Expansion Bus Select(PC0-PC11, PCZ80)	0x7FF0-0x7FFD
ROM	Rom Page Register	0x8000-0XFFFF
RAM	RAM	0x0000-0X7FEF

CPU(6502)

U1
W65C02S6TQG-14

R1 1k, R2 1k, R3 1k, R4 1k

BE — R7 0R — IRQB — R11 0R — TP3 — RWB — R18 0R — RDY — R20 0R — nCPUReset — R22 0R — System_Clock — R24 0R — R27 0R — TP25 RDY — R31 1k

TP4, TP6, TP2, TP5, TP1, TP7

42	PHI1O	D0	30
37	PHI2O	D1	29
36	SOB	D2	28
2	SYNC	D3	27
40	VPB	D4	26
6	NC_1	D5	25
33	NC_2	D6	24
		D7	23
34	BE	A0	4
43	IRQB	A1	5
44	MLB	A2	7
1	NMIB	A3	8
32	RWB	A4	9
41	RDY	A5	10
38	RESB	A6	11
35	PHI2	A7	12
		A8	13
		A9	14
		A10	15
		A11	16
		A12	19
		A13	20
		A14	21
		A15	22

VDD_1 (3), VDD_2 (31); VSS_1 (17), VSS_2 (18), VSS_3 (39) → GND

RAM

U2
CY62256NLL-55SNXI

D0	11	D0	
D1	12	D1	
D2	13	D2	
D3	15	D3	
D4	16	D4	
D5	17	D5	
D6	18	D6	
D7	19	D7	
A0	21	A0	
A1	23	A1	
A2	24	A2	
A3	25	A3	
A4	26	A4	
A5	1	A5	
A6	2	A6	
A7	3	A7	
A8	4	A8	
A9	5	A9	
A10	6	A10	
A11	7	A11	
A12	8	A12	
A13	9	A13	
A14	10	A14	
		CE	20 RAM_CE#
		WE	27 RWB
		OE	22 RAM_OE#

VCC (28), GND (14)

ROM

U3
SST39SF040-55-4C-NHE-T

D0	13	DQ0	
D1	14	DQ1	
D2	15	DQ2	
D3	17	DQ3	
D4	18	DQ4	
D5	19	DQ5	
D6	20	DQ6	
D7	21	DQ7	
A0	12	A0	
A1	11	A1	
A2	10	A2	
A3	9	A3	
A4	8	A4	
A5	7	A5	
A6	6	A6	
A7	5	A7	
A8	27	A8	
A9	26	A9	
A10	23	A10	
A11	25	A11	
A12	4	A12	
A13	28	A13	
A14	29	A14	
Page_0	3	A15	
Page_1	2	A16	
Page_2	30	A17	
Page_3	1	A18	
		CE#	22 ROM_CE#
		WE#	31 RWB
		OE#	24 ROM_OE#

VDD (32), VSS (16) → GND

Control

U4
ATF1502AS-10JU44

RWB	4	I/O_1	I/O/TCK 32 TCK
PRGM_RAM_ROM	5	I/O_2	I/O/TDO 38 TDO
PRGM_RAM_ROM_CS	6	I/O_3	I/O/TMS 13 TMS
PGM_Mode	8	I/O_4	I/O/TDI 7 TDI
PageRegister_CS	9	I/O_5	
BE	12	I/O_6	
PSC_Cntrl_CS	14	I/O_7	
PSC_D3	16	I/O_8	
PSC_D2	17	I/O_9	GCLR/I 1 Page_Register
PSC_D1	18	I/O_10	
PSC_D0	19	I/O_11	OE1/I 44 OE1_I
RAM_CE#	20	I/O_12	GCLK2/OE2/I 2 JLink_Mode
RAM_OE#	21	I/O_13	GCLK1/I 43 CPLD_Clock
ROM_CE#	24	I/O_14	GCLK3/I/O 41 PCZ80_Extra — TP57
ROM_OE#	26	I/O_15	
A15	27	I/O_16	
A1	28	I/O_17	
A2	29	I/O_18	PD1/I/O 11 RDY
A3	31	I/O_19	PD2/I/O 25 Int_Cntrl_CS
A4	33	I/O_20	
A5	34	I/O_21	
A6	36	I/O_22	
A0	37	I/O_23	
A14_A11	39	I/O_24	
A10_A7	40	I/O_25	

VCC_1 (3), VCC_2 (15), VCC_3 (23), VCC_4 (35); GND_1 (10), GND_2 (22), GND_3 (30), GND_4 (42) → GND

Page Register and System Reset

IC1
AVR64DD32-I_PT

TP8 — PG_PA2, PG_PA3, PG_PA4, PG_PA5, PG_PA6, PG_PA7, PG_PD1, PG_PD2 — TP_1X10 → GND

PageRegister_CS	30	PA0	
RWB	31	PA1	
PG_PA2	32	PA2	
PG_PA3	1	PA3	
PG_PA4	2	PA4	
PG_PA5	3	PA5	
PG_PA6	4	PA6	
PG_PA7	5	PA7	
D0	6	PC0	
D1	7	PC1	
D2	8	PC2	
D3	9	PC3	
		PF7_(UPDI)	27 — P1 pin 1 — PG_UPDI
		PF6_(RESET)	26 — R58 0R — nSystemReset
		PF5	25 — R59 0R — POW_Reset
		PF4	24 — R60 0R — nCPUReset
		PF3	23 Page_3
		PF2	22 Page_2
		PF1	21 Page_1
		PF0	20 Page_0
		PD7	17 PSC_D3
		PD6	16 PSC_D2
		PD5	15 PSC_D1
		PD4	14 PSC_D0
		PD3	13 PGM_Mode
		PD2	12 PG_PD2
		PD1	11 PG_PD1

VDDIO2 (10), VDD_1 (18), VDD_2 (28); GND_1 (19), GND_2 (29) → GND

P1: MHDR1X3_100 → GND

In PGM_Mode,
PSC_D0-D3 will be the page register values for the ROM. The current value will be saved.

The Page Resister will see the PGM_Mode low and set the Page0-3 to the correct value. When PGM_Mode goes Hi
the saved value will be restored.

POW_Reset is controlled by the button and the Programmer. The nSysteReset is used to reset all other parts except the CPU. This will allow for Hardware dela before the CPU is brought out of reset using the nCPUReset line

Reset

R56 1k

X1 SKRAAME010

C1 100nf

POW_Reset

CPLD Configuration

R12 10k — Page_Register

R13 10k DNI — JLink_Mode

R14 10k — OE1_I

R15 10k DNI

R16 10k DNI

R17 10k DNI

B1

CD74HCT20MT

A7	1	1A	
A8	2	1B	
A9	4	1C	
A10	5	1D	
A14	9	2A	
A13	10	2B	
A12	12	2C	
A11	13	2D	
		1Y	6 A14_A11 — TP17
		2Y	8 A10_A7 — TP24
		NC_1	3
		NC_2	11

VCC (14), GND (7) → GND

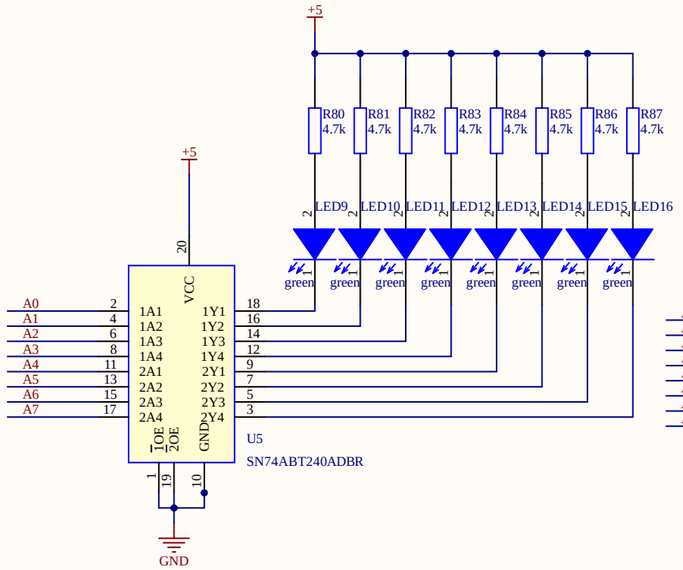
Title: CPU Board

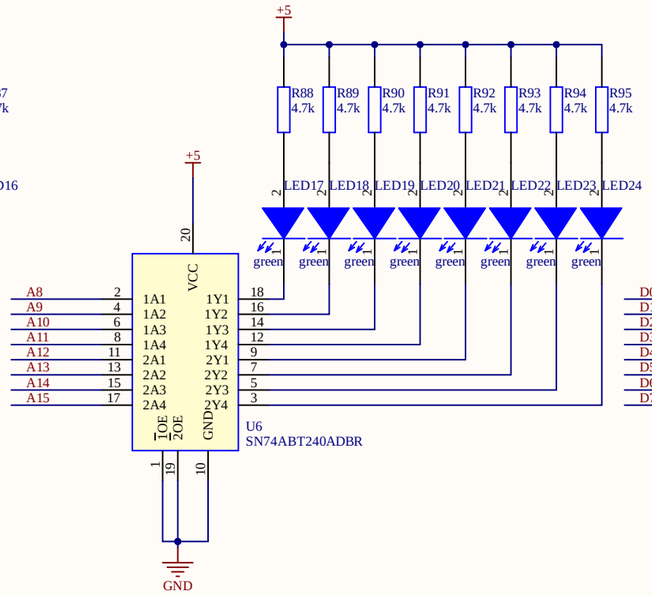
Project: CPU_Board_V1_2.PrjPcb

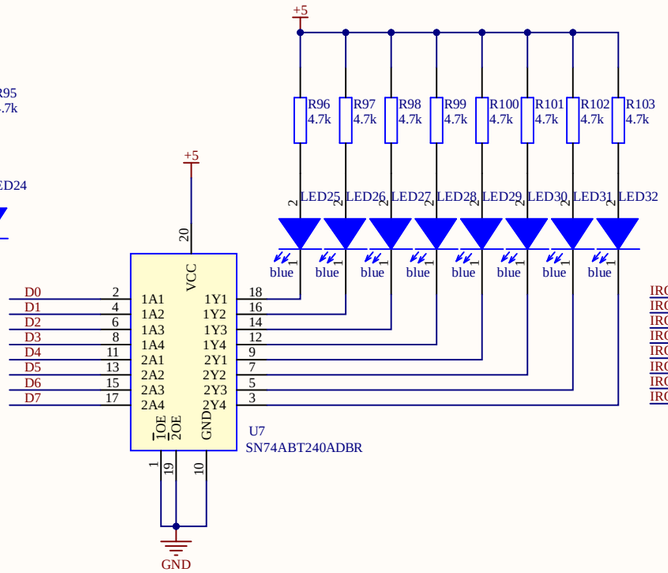
ABS Data Systems, Inc.
317 Sebastian Crossings Blvd
Sebastian, FL 32958
(858) 254-7776
www.absdatasystems.com

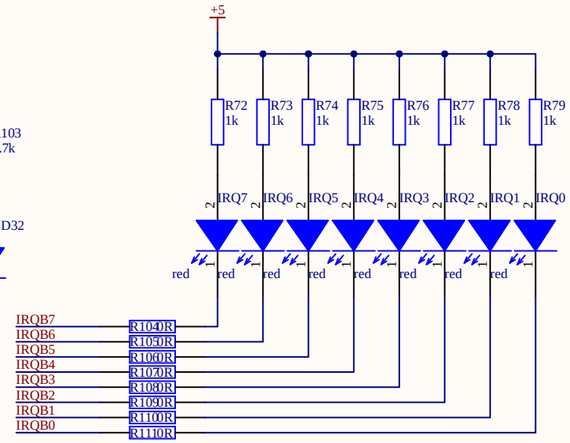
Engineer:
Terry D. Schevker

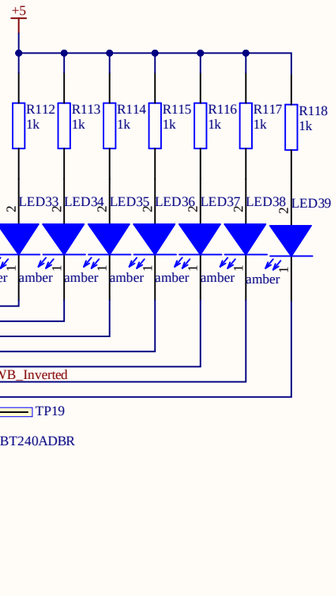
Date: 03/13/2023
Revision 1.0
Print Date 09/27/2025
Sheet 1 of 8

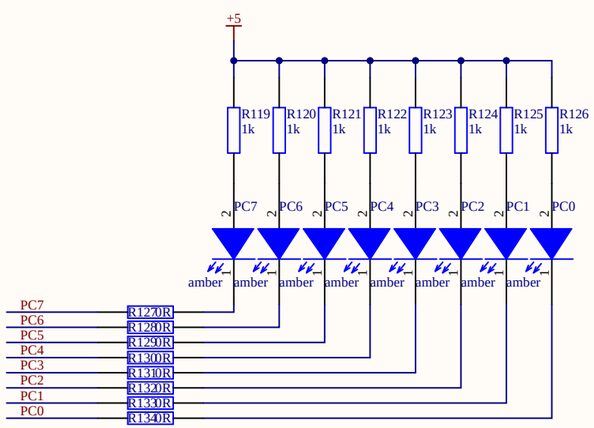


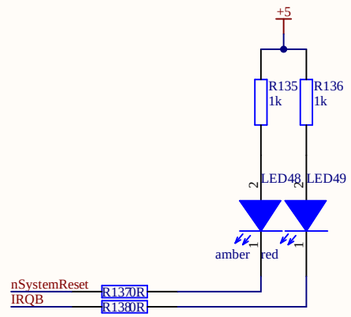




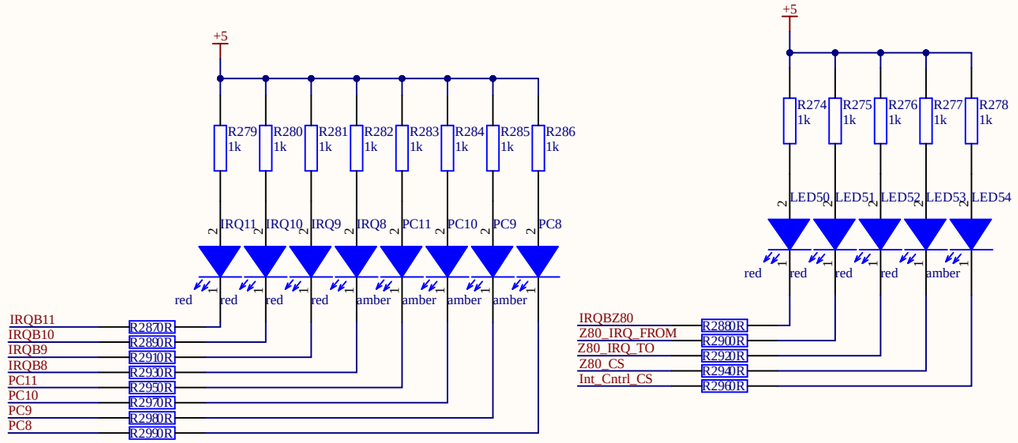


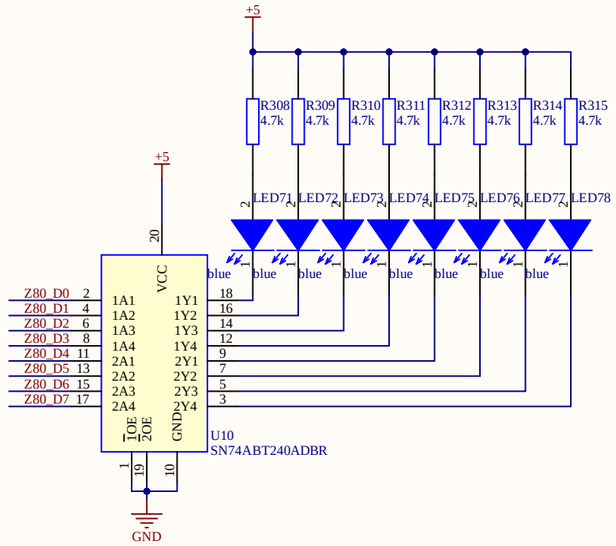


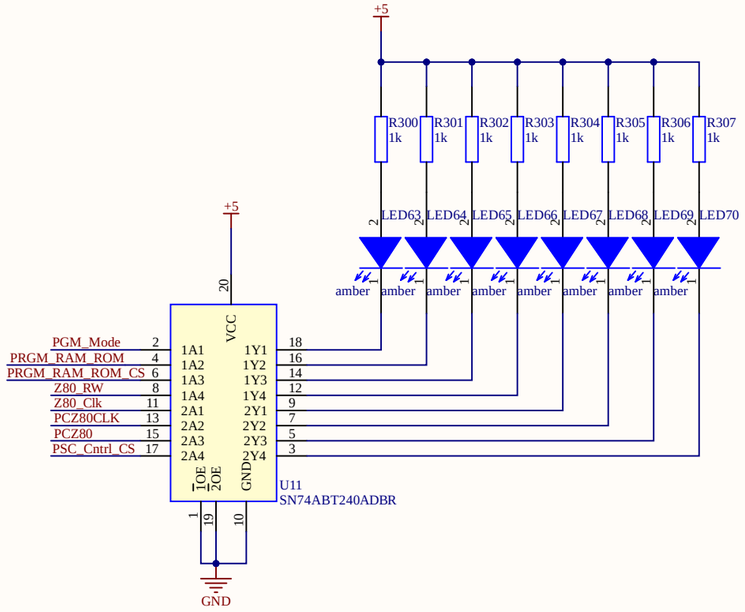




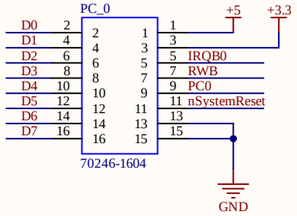
Title: LED Monitor	
Project: CPU_Board_V1_2.PrjPcb	
ABS Data Systems, Inc. 317 Sebastian Crossings Blvd Sebastian, FL 32958 (858) 254-7776 www.absdatasystems.com	Engineer: Terry D. Schevker
	Date: 12/20/2022 Revision 1.0
	Sheet 2 of 8 Print Date 09/27/2025

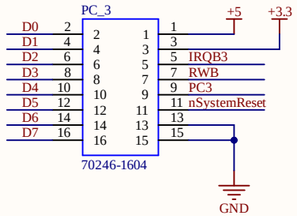


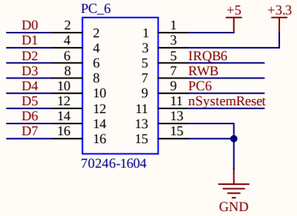


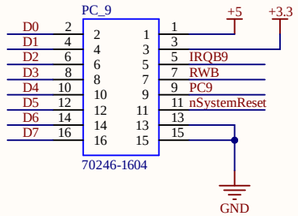


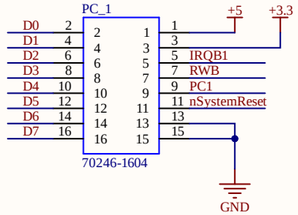
Title: *	
Project: CPU_Board_V1_2.PrjPcb	
ABS Data Systems, Inc. 317 Sebastian Crossings Blvd Sebastian, FL 32958 (858) 254-7776 www.absdatasystems.com	Engineer: * Date: * Revision * Sheet 3 of 8 Print Date 09/27/2025

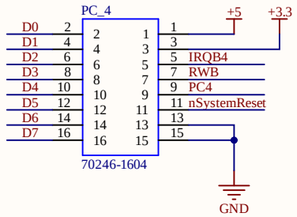


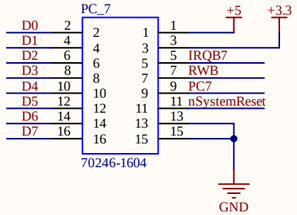


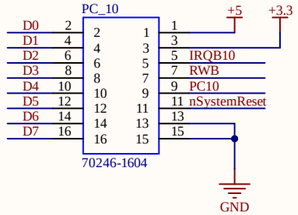


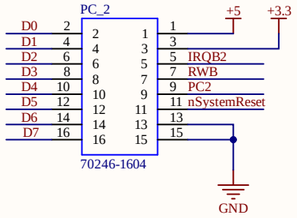


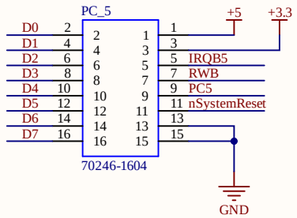


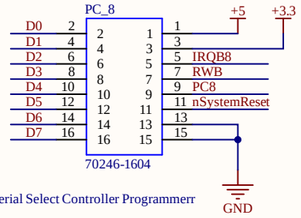


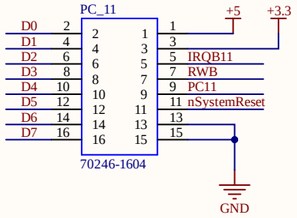


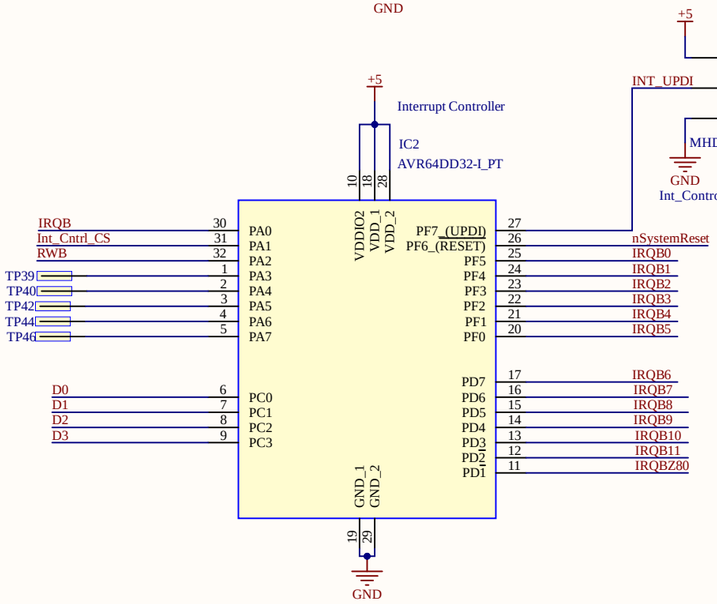




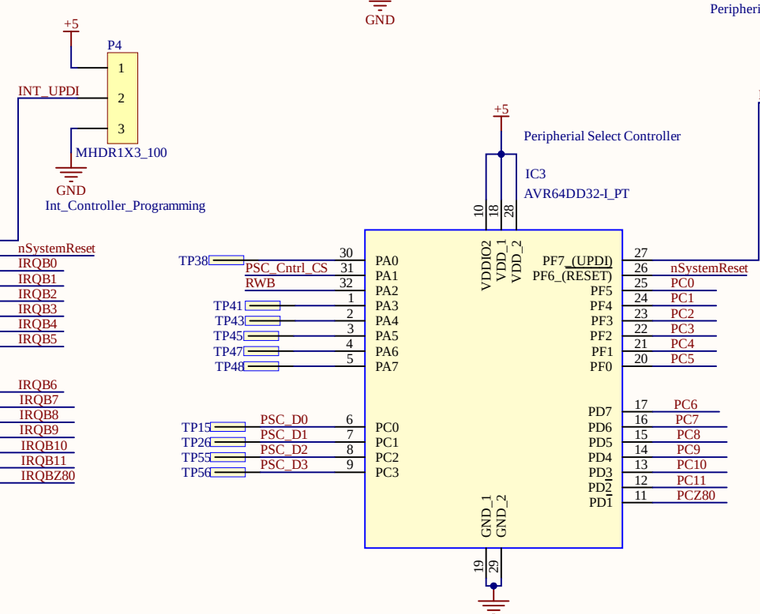








Peripherial Select Controller Programmerr



Title:	Peripheral Bus
Project:	CPU_Board_V1_2.PrjPcb
ABS Data Systems, Inc. 317 Sebastian Crossings Blvd Sebastian, FL 32958 (858) 254-7776 www.absdatasystems.com	Engineer: Terry D. Schevker
Date: 03/13/2023	Revision 1.0
Sheet 4 of 8	Print Date 09/27/2025

LED Monitor

CPU(6502)

Control(CPLD)

RAM

ROM

System Clock

+5

C2 100nf
C3 100nf
C4 100nf
C5 100nf
C6 100nf
C7 1nf
C8 1uf
C9 100nf
C10 1nf
C11 1uf
C12 0.22uf
C13 0.22uf
C14 0.22uf
C15 0.22uf
C16 100nf
C17 100nf
C18 100nf

GND

J1 1803439

GND GND

+5 +3.3

U9
LD1117DT33CTR
VIN VOUT GND

C20 1uf
C19 47uF

GND GND GND

Power

+5

X2 On/Off Switch

TP20 TP21

JS202011SCQN

D1

S3AFGHM3

Oscillator Selection

+5

X3
LFSPXO025876Reel
13.56 Clock

VCC Clock Enable GND

R1400R

R1390R

P7

OSC_Out
OSC_14MHz

Jumper 1 - 2 to use 13.56 MHZ clock
Jumper 2 - 3 to use 14 MHz clock

P2

OSC_Out
System_Clock
External_System_Clock

Jumper 1 - 2 to use Internal clock
Jumper 2 - 3 to use External clock
Remove Jumper to allow Programmer to act like J-Link Device

P3

External_System_Clock

GND

For External Crystal Oscilator board

+5 +3.3

TP22 TP23 TP14 TP16

GND GND

+3.3 +3.3

R5 10k
R6 10k

+3.3

28MHz

X4
XLH736056000000X

E/D_1 E/D_2 VDD GND OUT OUT2

28Mhz_Clock

TP11

GND

+5

Level Shifter

U12
74HCT14D_BJ

28Mhz_Clock
OSC_14MHz_FF_Out
28Mhz_Clock
CPLD_Clock_FB
TP9
TP12

1A 2A 3A 4A 5A 6A VCC GND 1Y 2Y 3Y 4Y 5Y 6Y

OSC_28MHz
OSC_14MHz
CPLD_Clock_FB
CPLD_Clock_28MHz
TP10
TP13

GND

+5 +5 +5

R8 R9 R10
10k 10k 10k

+5

Divider

U13
MC74AC74DTR2

Clk_FB
OSC_28MHz

Data1 SD1 CD1 CLK1 Data2 SD2 CD2 CLK2 VCC GND Q1 /Q1 Q2 /Q2

OSC_14MHz_FF_Out
Clk_FB

TP49
TP50
TP51
TP53

TP52
TP54

14MHz Clock

GND

System_Clock
CPLD_Clock
CPLD_Clock_28MHz

P8

Jumper 1 - 2 to use System clock
Jumper 2 - 3 to use 28 MHZ clock

Default Jumpers
P2 1-2 System Clock Internal
P7 2-3 14 MHZ Clock
P9 1-2 CPLD Clock System Clock

+5 +5 +5

R141 1k
R147 1k
R148 1k

J_Tag
CPLD

+5

H2

TCK
TDO
TMS
TDI

R1490R
R1500R
R1510R
R1550R

Header_IDC_2x5
SAM10835-ND

GND GND

Title:	Power Board
Project:	CPU_Board_V1_2.PrjPcb
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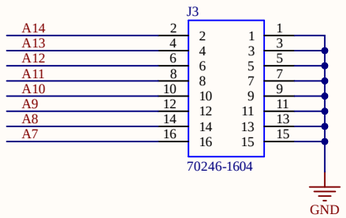
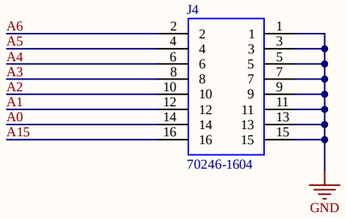
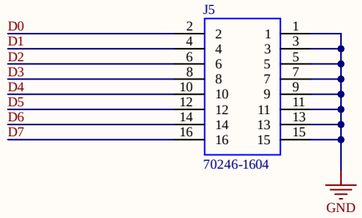
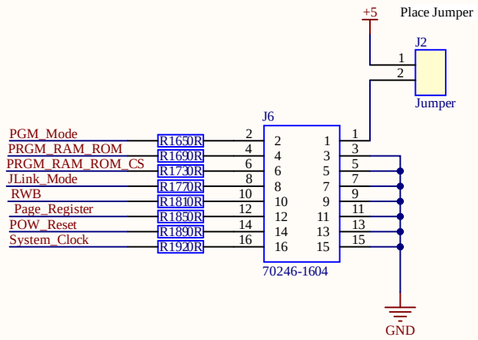
Programmer Interface









Title: Programmer Interface	
Project: CPU_Board_V1_2.PrjPcb	
ABS Data Systems, Inc. 317 Sebastian Crossings Blvd Sebastian, FL 32958 (858) 254-7776 www.absdatasystems.com	Engineer: Terry D. schevker
	Date: 02/08/2023 Revision 1.0
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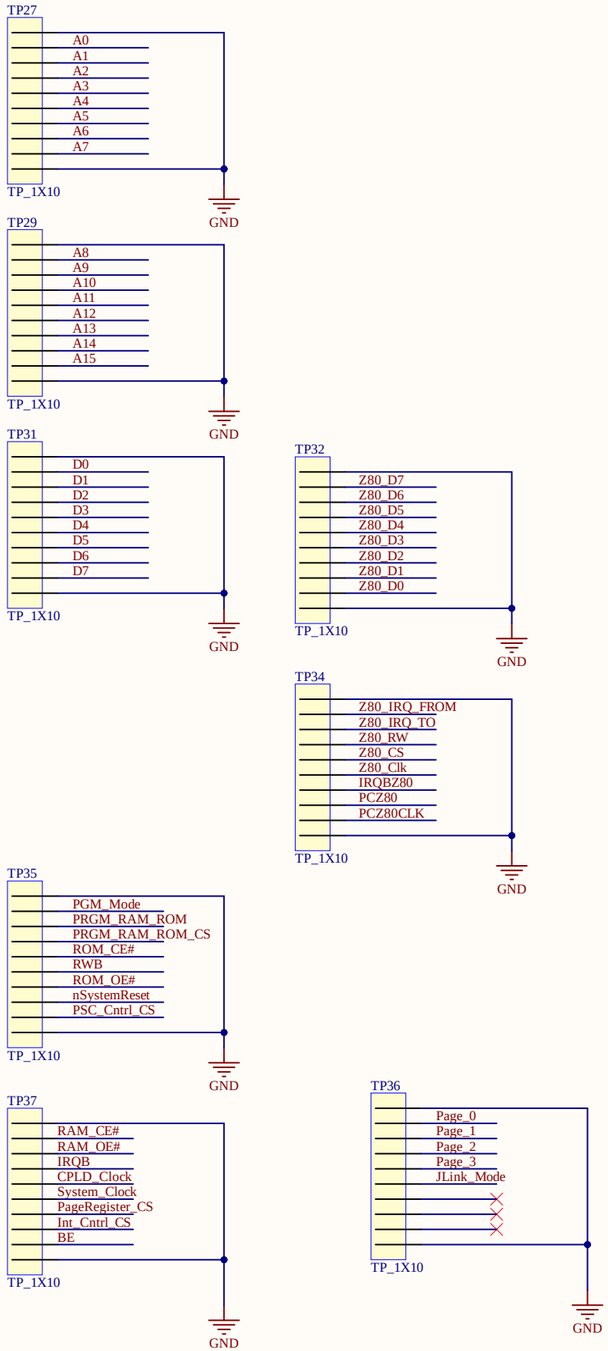

Title:	Test Points
Project:	CPU_Board_V1_2.PrjPcb
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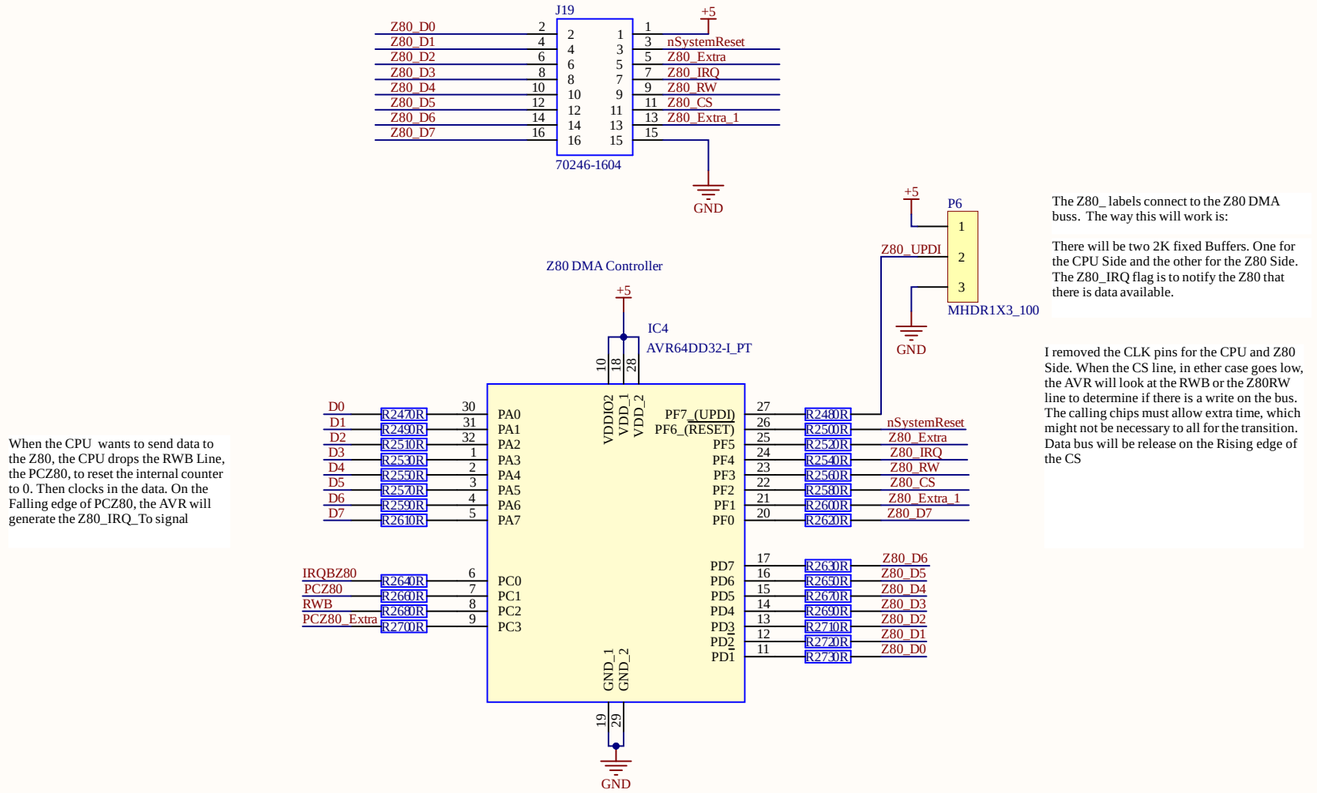

When the CPU wants to send data to the Z80, the CPU drops the RWB Line, the PCZ80, to reset the internal counter to 0. Then clocks in the data. On the Falling edge of PCZ80, the AVR will generate the Z80_IRQ_To signal

The Z80_ labels connect to the Z80 DMA buss. The way this will work is:

There will be two 2K fixed Buffers. One for the CPU Side and the other for the Z80 Side. The Z80_IRQ flag is to notify the Z80 that there is data available.

I removed the CLK pins for the CPU and Z80 Side. When the CS line, in ether case goes low, the AVR will look at the RWB or the Z80RW line to determine if there is a write on the bus. The calling chips must allow extra time, which might not be necessary to all for the transition. Data bus will be release on the Rising edge of the CS

Title: Z80 Interface	
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