SIEMENS

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DisplayPort Link Layer

Isochronous Transport Services Interface Document

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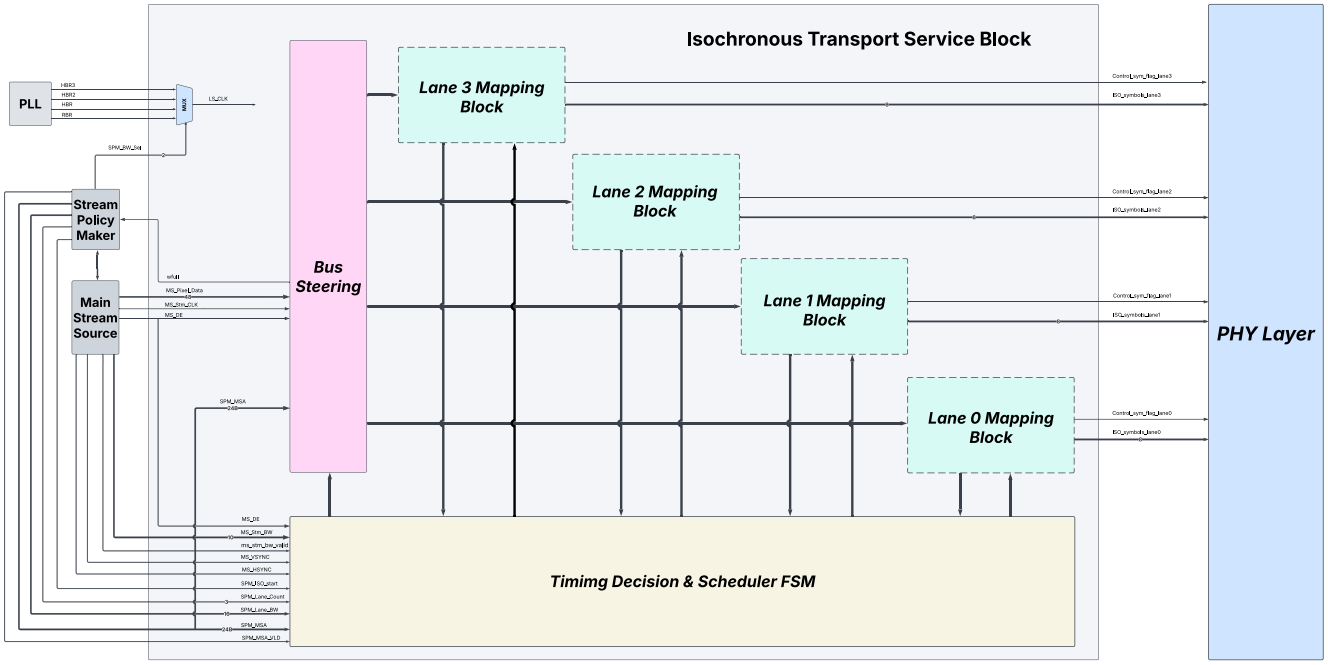


- System Description:

The Isochronous Transport Services block ensures the reliable transmission of time-sensitive data streams over the Main-Link. DisplayPort's Main-Link can operate with one, two, or four lanes, each capable of transmitting 8-bit data per Link Symbol Clock cycle *(LS_Clk)*. The primary functions of these services include:

- **Mapping video stream data to and from the Main-Link lanes**
  - Packing and unpacking pixel data from the uncompressed video stream into structured data units.
  - Inserting and removing stuffing data to maintain proper data alignment.
  - Framing and deframing data for transmission.

- **Stream clock regeneration for synchronization with the source clock**
  - The incoming video stream is received at its original clock rate (Stm_Clk) and mapped to the Link Layer output, where it is transmitted to the PHY Layer at the Link Symbol Clock rate (LS_Clk).

- **Stream clock regeneration for synchronization with the source clock**

- **Embedding Main Stream Attribute (MSA) data to define video format and timing parameters**

- **Optional insertion of Secondary-data Packets (SDP) with Error Correction Code (ECC) for auxiliary data transmission**
  - Audio_Stream SDP for encapsulating audio data.
  - CTA-861 INFOFRAME SDP for transmitting metadata such as colorimetry, aspect ratio, and other display attributes.

(Note: SDP insertion is not implemented as it is optional.)

By performing these functions, the Isochronous Transport Services block enables efficient transmission of uncompressed video streams over the DisplayPort interface while maintaining synchronization and data integrity across the link.

- Interface Signal Description:

Signal	Interface	Type	Width *(Bits)*	Description
spm_iso_start	*Stream Policy Maker*	*Input*	1	The signal marks the beginning of a new video transmission and is asserted by the Stream Policy Maker to indicate that the main video stream is valid and should be processed. When de-asserted, it signifies either the end of the video stream or an error that requires stopping stream data transmission.
spm_lane_count			3	The signal represents the number of lanes that will be used for the stream transmission.
spm_lane_bw			16	The signal indicates the bandwidth of a single lane for stream transmission after link training. The 16-bit value is multiplied by 0.27 to determine the lane bandwidth (e.g., 1.62 Gbps, 2.7 Gbps).
spm_msa			24 Byte	The signal defines the Main Stream Attributes (MSA), which includes Hactive, Hblank, Vactive, Vblank, Color Depth, and other video timing details.
spm_msa_vld			1	This signal represents the valid flag of the MSA Data, asserting when the MSA input is valid and ready for use.
spm_bw_sel			2	It represents the selection line for the PLL-generated clock, corresponding to the different rates supported by 8b/10b DisplayPort devices. It selects the proper

				clock based on the lane bandwidth after link training.
Wfull		*Output*	1	This signal is asserted when the internal FIFO becomes full while the stream source is actively sending pixels. It indicates that a pixel overflow is imminent, as there is no more space to store incoming pixel data before it can be transmitted.
ms_pixel_data	*Main Stream Source*	*Input*	48	A 48-bit pixel data signal representing the pixel values for the transmitted frame.
ms_stm_clk			1	This signal represents the clock signal for the stream rate.
ms_de			1	This signal indicates the active period of the stream when HIGH and the blanking period when LOW.
ms_stm_bw			10	This signal indicates the bandwidth of the stream source (e.g, 60 MHz, 80 MHz, etc.)
ms_stm_bw_valid			1	This signal represents the valid flag of the MS_Stm_BW, asserting when the MS_Stm_BW input is valid and ready for use.
ms_vsync			1	This signal is asserted to indicate the start of the vertical blanking period and is activated after the front porch phase at its beginning.
ms_hsync			1	This signal is asserted to indicate the start of the horizontal blanking period and is activated after the front porch phase at its beginning.
ms_rst_n			1	Main stream source reset
hbr3_clk	*PLL*	*Input*	1	810 Msymbol/s per lane (HBR3)
hbr2_clk			1	540 Msymbol/s per lane (HBR2)
hbr_clk			1	270 Msymbol/s per lane (HBR)
rbr_clk			1	162 Msymbol/s per lane (RBR)
iso_symbols_lane0	*PHY Layer*	*Output*	8	Four 8-bit signals carry the processed main video stream data output from the Isochronous Transport Services Block. They are transmitted over the active lanes with the selected video format.
iso_symbols_lane1				
iso_symbols_lane2				
iso_symbols_lane3				
control_sym_flag_lane0			1	This signal is asserted when the block outputs control symbols, enabling the Physical Layer to distinguish between control and data symbols.
control_sym_flag_lane1				
control_sym_flag_lane2				
control_sym_flag_lane3				

- Flow of Operation:

Before the display transmission begins, the link layer continuously sends an **idle pattern** on the main link lanes, indicating that **no active stream** is present. This is achieved by enabling the **IDLE Pattern blocks** through the signals ***SCHED_Idle_EN_lane0***, ***SCHED_Idle_EN_lane1***, ***SCHED_Idle_EN_lane2***, and ***SCHED_Idle_EN_lane3*** by the **scheduler**.

Once link training is successfully completed, the **Stream Policy Maker (SPM)** provides the stream attributes (including ***SPM_MSA***, ***SPM_MSA_VLD***, ***SPM_Lane_BW***, and ***SPM_Lane_Count***) to the **Isochronous Transport Services (ISO)**. At the same time, SPM instructs the **ISO** to begin transmission by asserting ***SPM_ISO_start***. During this, the **Main Stream source (MS)** transmits essential stream information (such as ***MS_Pixel_Data***, ***MS_Stm_CLK***, ***MS_DE***, ***MS_Stm_BW***, ***MS_VSYNC***, and ***MS_HSYNC***).

The ***MS_Pixel_Data*** from the Main Stream source is then passed through a **Time Base Converter (TBC) (an asynchronous FIFO)**, which converts it from the Stream domain to the Link Symbol domain. The data is subsequently stored in a **FIFO**, from where the **Main Bus Steering** reads it when required.

Simultaneously, the **Timing Decision Block** receives stream attributes from the **SPM** and additional signals from the **Main Stream source**, including ***SPM_MSA***, ***SPM_MSA_VLD***, ***SPM_Lane_BW***, ***SPM_Lane_Count***, ***MS_DE***, ***MS_Stm_BW***, ***MS_VSYNC***, and ***MS_HSYNC***. It processes this information to:

1. Calculate and set the required counter values for the **Scheduler**.
2. Extract and forward necessary parameters to the **Scheduler** for scheduling blanking periods and active video transmission.

Upon receiving this information, the **Scheduler** initiates a **VBlank period** by enabling the **Blank Mapper Block(s)** using ***SCHED_Blank_EN_lane0***, ***SCHED_Blank_EN_lane1***, ***SCHED_Blank_EN_lane2***, and ***SCHED_Blank_EN_lane3*** according to the number of active lanes (derived from ***TD_Lane_Count***), while the remaining lanes continue transmitting the **idle pattern**.

During the **VBlank period**, the **Scheduler** instructs the **Blank Mapper Blocks** on the appropriate actions using ***SCHED_Blank_State*** and identifies the type of blanking period using ***SCHED_Blank_ID***. The **Blank Mapper Block(s)** then generate the required symbols, such as:

- **BS + BF + BF + BS.**
- **VBID** + **Mvid** (from the **Secondary Bus Steering Block**) + **Maud.**
- **MSA transmission** (including: **SS + SS**, **MSA** (from the secondary bus steering) and **SE**).
- **dummy symbols**.
- **BE** (only at the end of the **HBlank**).

This process repeats for each line in the **VBlank period**, except that **MSA is only sent once per VBlank period**.

Once **VBlank** ends, the **HBlank period** begins. The **Scheduler** follows a similar process, directing the

Blank Mapper Blocks through ***SCHED_Blank_State*** and ***SCHED_Blank_ID***, repeating the blanking sequence without resending **MSA**.

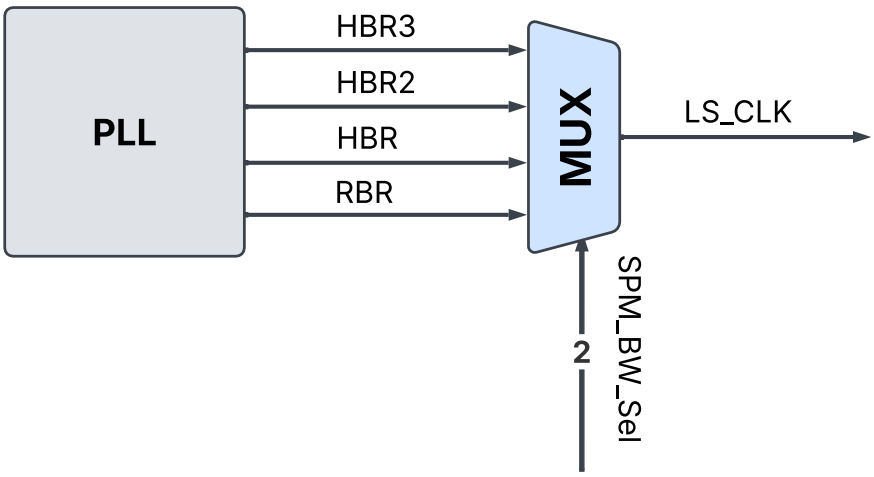
After **HBlank**, the first active video line starts. The **Scheduler** activates the **Active Mapper Blocks** using ***SCHED_Stream_EN_lane0***, ***SCHED_Stream_EN_lane1***, ***SCHED_Stream_EN_lane2***, and ***SCHED_Stream_EN_lane3*** signals based on ***TD_Lane_Count***. The remaining lanes continue transmitting the **idle pattern**.

During the active video phase, the **Scheduler** use the received (***TD_TU_VLD_Data_Size***, ***TD_TU_STUFFED_Data_Size***, ***TD_TU_Alternate_UP***, and ***TD_TU_Alternate_Down*** signals), so it can direct the **Active Mapper Blocks** using ***SCHED_Blank_State***. The **Active Mapper Blocks** handle the transmission of active pixel data from the **Main Bus Steering** and stuff it with dummy symbols by inserting stuffing symbols, including:

- **FS (Fill Start)**
- **Stuffing dummy symbols**
- **FE (Fill End)**

This ensures complete **Transfer Units (TUs)** for each video line before entering the next **HBlank**. This process repeats for each subsequent line of pixels until the full frame is transmitted. Once the frame is complete, a new frame begins with **VBlank**, and the cycle continues until the **SPM signals the end of the display** by **de-asserting** ***SPM_ISO_start***, so the scheduler turns all lanes to the **Idle state.**

Clock Calculation



In DisplayPort, the Main Link lanes operates at specific rates at the PHY-to-PHY serial link as following:

- 1.62 Gbps/lane (RBR)
- 2.7 Gbps/lane (HBR)
- 5.4 Gbps/lane (HBR2)
- 8.1 Gbps/lane (HBR3)

Since the PHY layer employs **8b/10b encoding**, every 8 bits of data are mapped to 10 transmitted bits. As a result, the effective data rate at the Link Layer is as follow:

- **162 Msymbol/s per lane (RBR)**
- **270 Msymbol/s per lane (HBR)**
- **540 Msymbol/s per lane (HBR2)**
- **810 Msymbol/s per lane (HBR3)**

By using a pipelined architecture where each internal block processes data in a single cycle, the Link Layer clock should also run at **the same** effective data rates as above to ensure synchronized data processing. Therefore, the Link Layer clock must operate at the same effective data rate. Based on the ***SPM_BW_Sel*** signal, a corresponding clock is applied within the ISO to match the selected bandwidth mode.

The **Phase-Locked Loop (PLL)** generates multiple clock frequencies based on a reference clock input as listed above, ensuring stable and precise timing for various system operations. It plays a crucial role in high-speed data transmission and synchronization by maintaining consistent clock signals across different components.

Value in DBCD register	Bandwidth Per Lane	Description
06h	1.62 Gbps/lane	***RBR*** (Reduced Bit Rate)
0Ah	2.7 Gbps/lane	***HBR*** (High Bit Rate)
14h	5.4 Gbps/lane	***HBR2*** (High Bit Rate 2)
1Eh	8.1 Gbps/lane	***HBR3*** (High Bit Rate 3)