VRISC-V

minimalism they said….

First, i want to apologize because i’m not very good in english

I

Why i need a very reduced ISA as RISC is already a reduced ISA ?

Some history

The RISC vs CISC war

RISC |

- Quick instructions execution

- Less versatile but less subject to heat up

CISC |

- Slow instructions execution

- More versatile but more subject to heat up

And now :

VRISC-V |

- Very quick instructions execution

- Less versatile than RISC and the temp factor is unknow at this time.

« According to our current understanding of physics, the planck length is the shortest unit of length possible in spacetime due to the impossibility of observing anything smaller. »

Planck lenght - wikipedia

II

Very Reduced Instruction

- Need more assembly code
- Almost no branching possibility
- More simple to understand especially for beginners
- Few pseudoinstructions
- Garbage Unit to « destroy » incorrect instructions, further details in PDF ISA Spec.

Personal hypothesis :

- ASM code will need far more lines but will also be less difficult to read.
- Need less electric power input
- Eventually became very good CPU for simple embedded system. (graphic calculator , smartwatch, even talkie-walkie….).

III

To finish this small paper, i wish i could make a sample of the same function written in RV32I and VRV32I but the ISA is in… well we can say i’m in crunch time at this moment for the ISA spec.

Thanks for reading.

CLEMENT Dylan