

1. Introduction

At this time most peoples in the whole world use an automated digital clock in their everyday use. Starting from the hand watch we were to those huge street clocks every one of us are dependent on the display the make. In 21th century time being more than money, regarding this change our hobbies of checking our time every minute is dramatically increasing. About 99% of today's digital clocks are made using microcontrollers which make them more hand able from the rest, those we can set the time to start any minute or second we want and also set an alarm for reminder so that the system will store the value in a memory and then when the time reaches the alarm will be on. As the microcontroller consists almost all the logical devices external logic gates doesn't exist.

In order to be used properly and for a long life usage digital clocks must cover a very small place as much as it could but the size of most of the digital clocks manufactured this time is unexpectedly increasing as the use the give increases. This are the list of problems that exists in today's digital clocks

- An extensive range of large.
- Use of independent LED matrix digital wall for the display that takes a huge space in the circuit and a lot of matrix code in the controller.
- Displays only hour and minute. This makes the use they give us limited on the range given.
- Not easy to maintain. When the clock gets damaged some can't tell where the problem is easily, on the microcontroller or on the other driver ICS.
- Very costly.

The system that is anticipated to be built consists of a 6 digit clock including hour, minute and second using a very cheap devices that covers a very favorable place. The design consists of all the features that a digital clock should consist and as the design is synchronous the overall delay is negligible.

2. Objective

Our proposed system will be using a JK flip flop to make the synchronous counter that counts the hour, minute and second and also uses three push buttons to set those outputs.

3. Significance of the project

Digital clocks are being a very useful components of our lives. Regarding this change the need of accurate and simple materials also dramatically increasing. Our proposed project uses a very simple logic devices to build an accurate synchronous digital clock that is expected to satisfy the need of those materials.

4. Scope of the project

This project will extend its range till the far possible reach having a negligible delay, a setting buttons and a second display.

5. Literature review

In all walks of life, digitals system are making sophisticated approach to the mankind. Of course the machines cannot be replaced by human beings in exact accuracy in some fields. For a long time humans were using analog devices in our case analog clocks in their daily life.

The first digital pocket watch was the invention of Austrian engineer Josef Pallweber who created his "jump-hour" mechanism in 1883. Instead of a conventional dial, the jump-hour featured two windows in an enamel dial, through which the hours and minutes are visible on rotating discs. The second hand remained conventional. By 1885 Pallweber mechanism was already on the market in pocket watches by Cortébert and IWC; arguably contributing to the subsequent rise and commercial success of IWC. The principles of Pallweber jump-hour movement had appeared in wristwatches by the 1920s (Cortébert) and are still used today (Chronoswiss Digiteur). While the original inventor didn't have a watch brand at the time, his name has since been resurrected by a newly established watch manufacturer.

Plato clocks used a similar idea but a different layout. These spring-wound pieces consisted of a glass cylinder with a column inside, affixed to which were small digital cards with numbers printed on them, which flipped as time passed. The Plato clocks were introduced at the St. Louis World Fair in 1904, produced by Ansonia Clock Company. Eugene Fitch of New York patented the clock design in 1903. 13 years earlier Josef Pallweber had patented the same invention using digital cards (different from his 1885 patent using moving disks) in Germany (DRP No. 54093). The German factory Aktiengesellschaft für Uhrenfabrikation Lenzkirch made such digital clocks in 1893 and 1894.

The earliest patent for a digital alarm clock was registered by D.E Protzmann and others on October 23, 1956, in the United States. Protzmann and his associates also patented another digital clock in 1970, which was said to use a minimal amount of moving parts. Two side-plates held digital numerals between them, while an electric motor and cam gear outside controlled movement.

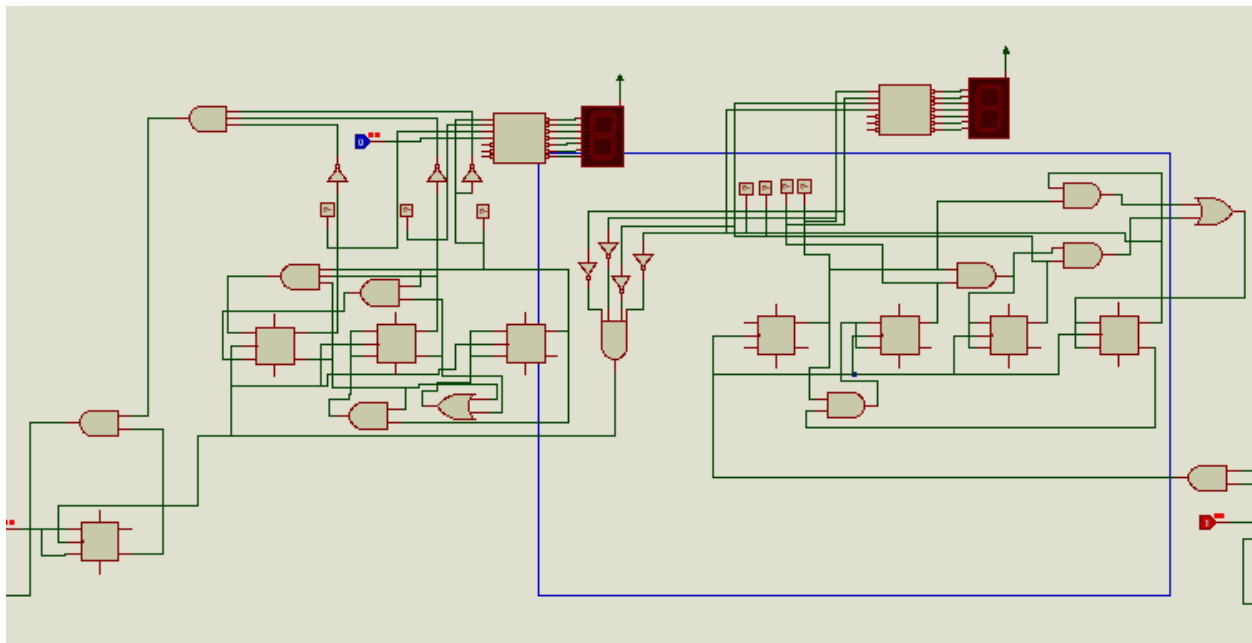
In 1970, the first digital wristwatch with an LED display was mass-produced. Called the Pulsar, and produced by the Hamilton Watch Company, this watch was hinted at two years prior when the same company created a prototype digital watch for Kubrick's *2001: A Space Odyssey*. Throughout the 1970s, despite the initial hefty cost of digital watches, the popularity of said devices steadily rose.

6. System design and analysis

6.1 Minute and second counter design

6.1.1 Decade counter

The minute and the second display counters are exactly the same design but in the consecutive clocking stage. The schematic diagram is given below.



Step 1 deciding the type and number of flip flops

The first one to design were the decade counter that will count from 1 to 9. In designing this counter there are four bits from X0 to X3 so there need to be four outputs or flip flops.

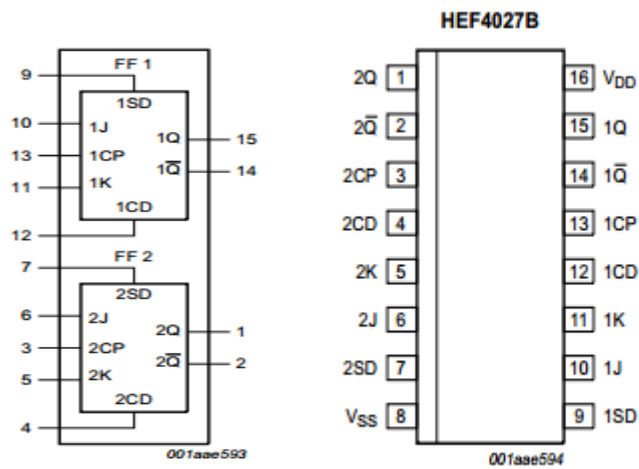
There are three types of flip flops that can be used to design this counter the one with one input, D and T types, decrease the number k-maps we solve but increase the number of logic units we use in the circuit and the two input, JK type, increase the number of k-map we solve but decrease the number logical circuits we use. So in order to decrease the cost we have chosen the JK type flip flops (HEF4027B).

The HEF4027B is a edge-triggered dual JK flip-flop which features independent set-direct (SD), clear-direct (CD), clock (CP) inputs and outputs (Q, Q̄). Data is accepted when CP is LOW, and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (CD) and set-direct (SD) inputs are independent and override the J, K, and CP inputs. The outputs are buffered for

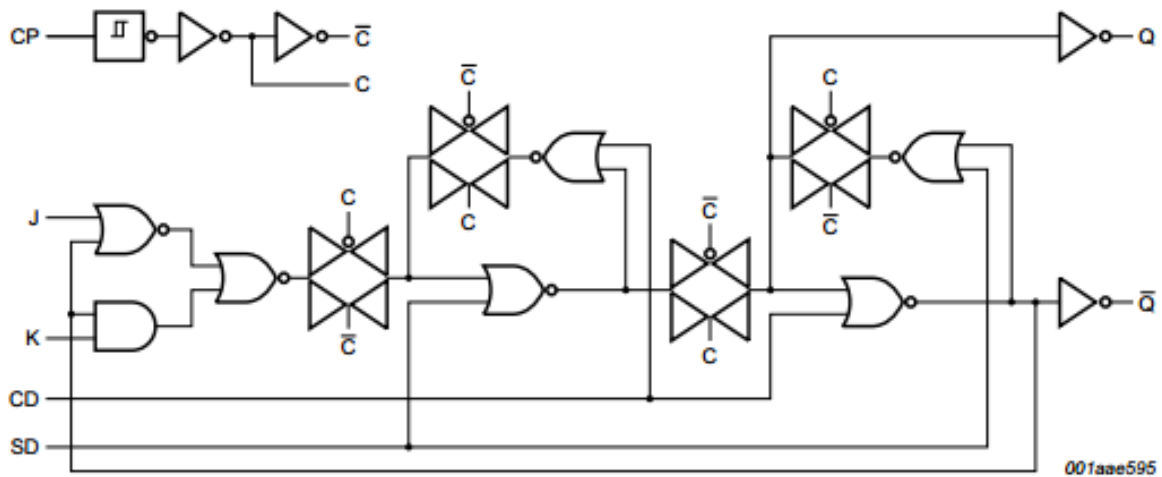
best system performance. Schmitt trigger action makes the clock input highly tolerant of slower rise and fall times. It operates over a recommended VDD power supply range of 3 V to 15 V referenced to VSS (usually ground). Unused inputs must be connected to VDD, VSS, or another input.

Features and benefits of HEF4027B

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to $+85^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B



Functional diagram



Logic diagram of one flip-flop

Pin description

Symbol	Pin	Description
V _{SS}	8	ground supply voltage
1SD, 2SD	9, 7	asynchronous set-direct input (active HIGH)
1J, 2J	10, 6	synchronous input
1K, 2K	11, 5	synchronous input
1CD, 2CD	12, 4	asynchronous clear-direct input (active HIGH)
1CP, 2CP	13, 3	clock input (LOW-to-HIGH edge-triggered)
1Q̄, 2Q̄	14, 2	complement output
1Q, 2Q	15, 1	true output
V _{DD}	16	supply voltage

Truth table

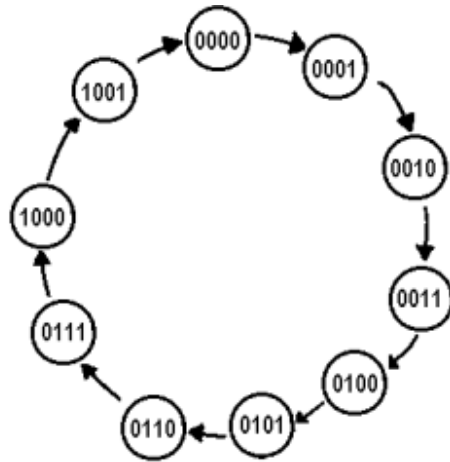
Inputs					Outputs	
nSD	nCD	nCP	nJ	nK	nQ	nQ̄
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H	H
L	L	↑	L	L	no change	no change
L	L	↑	H	L	H	L
L	L	↑	L	H	L	H
L	L	↑	H	H	nQ̄	nQ

Step 2 Excitation table of JK flip flop

Initial state	Next state	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step 3 State diagram and circuit excitation table

By the relation 2^n we will have 16 states but as our design is a decade counter it will stop in number 9 so we will have 10 states.



The excitation table of the counter will be like the table give below

Present State				Next State				Output							
Q ₃	Q ₂	Q ₁	Q ₀	Q ₃	Q ₂	Q ₁	Q ₀	J ₃	K ₃	J ₂	K ₂	J ₁	K ₁	J ₀	K ₀
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1

Step 4 obtain simplified equation using k map.

The Karnaugh maps of the output J_0 , K_0 , J_1 , K_1 , J_2 , K_2 , J_3 , and K_3 are shown below.

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	X	X	X	X
10	1	X	X	X

$J_0 = 1$

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	X	X	X
10	X	1	X	X

$K_0 = 1$

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00		1	X	X
01		1	X	X
11	X	X	X	X
10			X	X

$J_1 = \bar{Q}_3 Q_0$

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	X	1	
01	X	X	1	
11	X	X	X	X
10	X	X	X	X

$K_1 = \bar{Q}_3 Q_0$

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00			1	
01	X	X	X	X
11	X	X	X	X
10			X	X

$J_2 = Q_1 Q_0$

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	X	X	X
01			1	
11	X	X	X	X
10			X	X

$K_2 = Q_1 Q_0$

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00				
01			1	
11	X	X	X	X
10	X	X	X	X

$J_3 = Q_3 Q_0 + Q_2 Q_1 Q_0$

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10		1	X	X

$K_3 = Q_3 Q_0 + Q_2 Q_1 Q_0$

6.1.2 Module 6 (0-5) counter

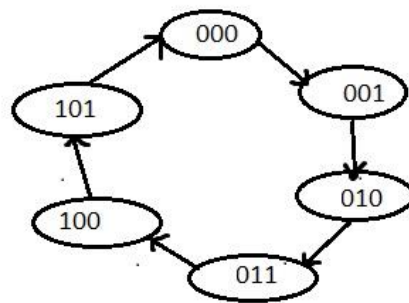
This is the left hand side of the counter that counts 0 up to 5 for the minute and second.

Step 1 Decide the type and the number of flip flops

The type of the flip flop is already chosen and the number of the flip flops in this case will be 3 because in order to count up to 5 we only need 3 bit output pins or flip flops.

Step 2 state diagram and circuit excitation table

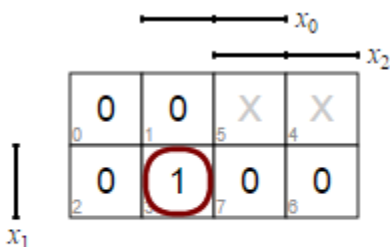
State diagram of the circuit consists of 6 states from 0 up to 5.



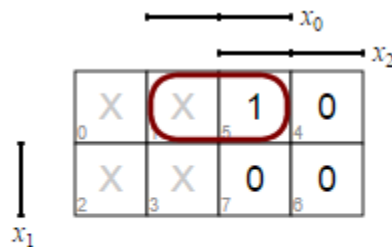
The excitation table for the circuit is given below

Initial state	Final state	J2	K2	J1	K1	J0	K0
000	001	0	X	0	X	1	X
001	010	0	X	1	X	X	1
010	011	0	0	X	0	1	X
011	100	1	1	X	1	X	1
100	101	X	X	0	X	1	X
101	000	X	X	0	x	x	1

For J2 and K2

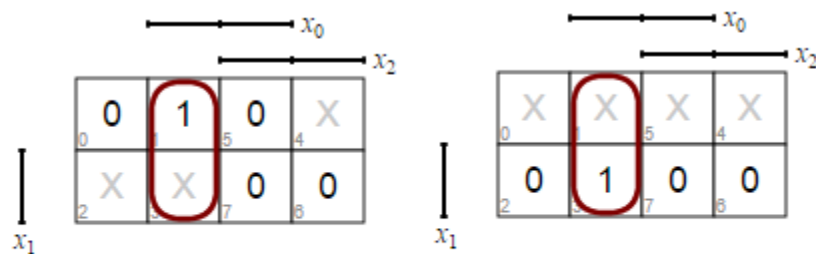


$$y = (\bar{x}_2 x_1 x_0)$$



$$y = (\bar{x}_1 x_0)$$

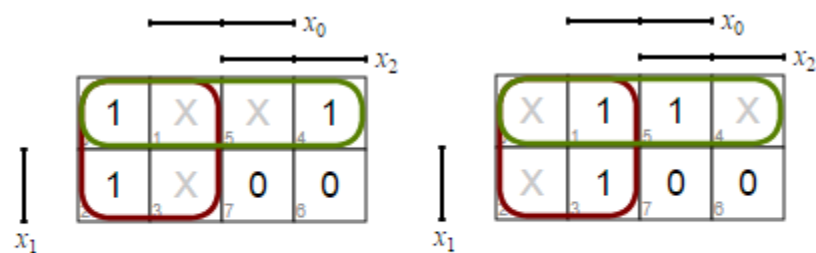
For J1 and K1



$$y = (\bar{x}_2 x_0)$$

$$y = (\bar{x}_2 x_0)$$

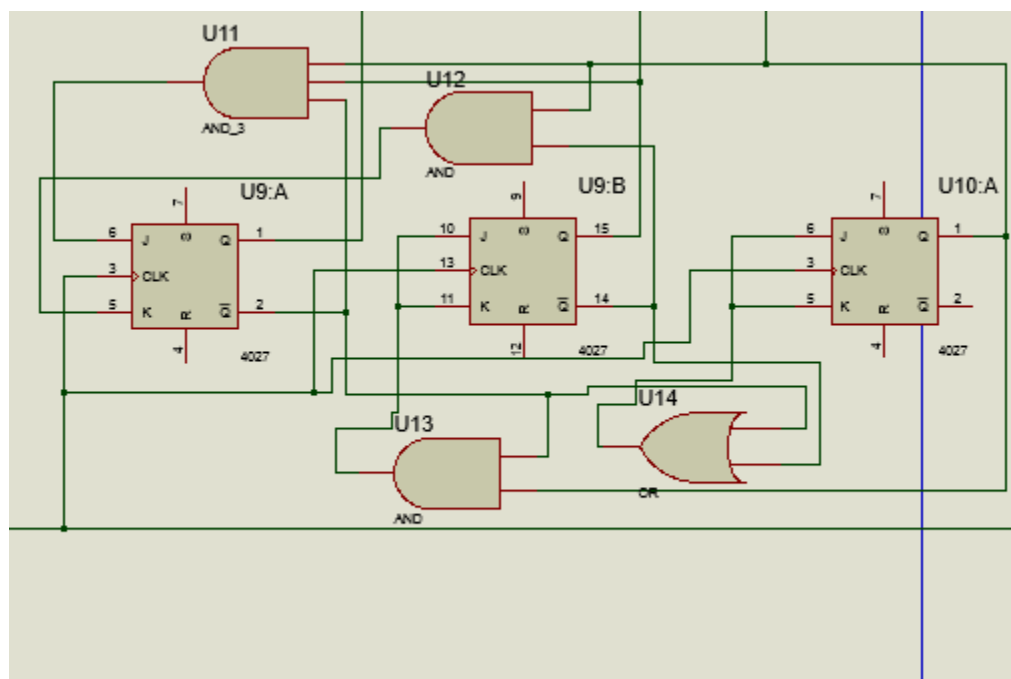
For Jo and Ko



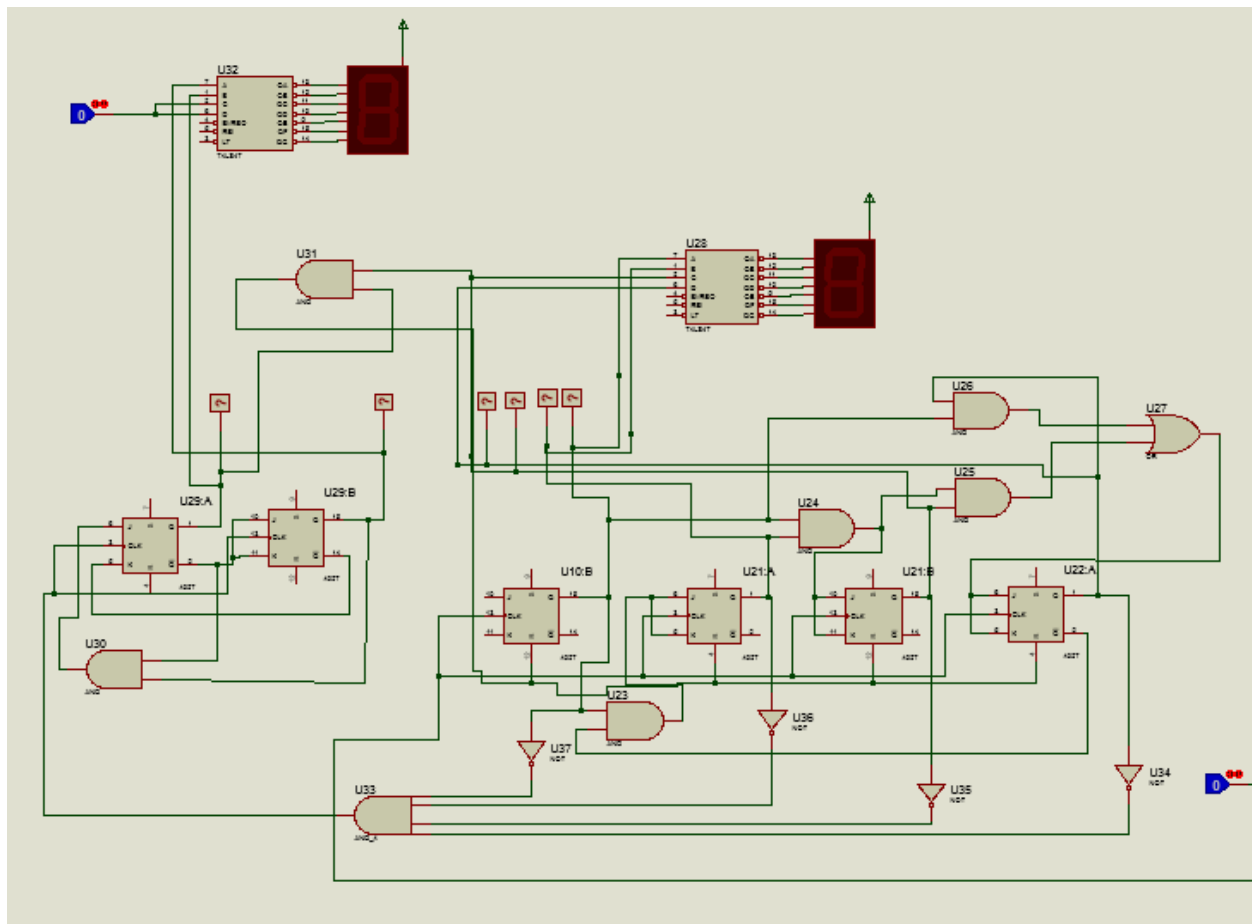
$$y = (\bar{x}_2) \vee (\bar{x}_1)$$

$$y = (\bar{x}_2) \vee (\bar{x}_1)$$

The final diagram will look like the following



6.2 The hour counter



The counter in the hour part of the circuit counts from 0 to 23 full 24 hour. We have achieved this by building two separate counters one that counts 0 to 9 and the other that counts 0 to 2. The decade counter we have used is the exact replication of the counter designed in the previous section.

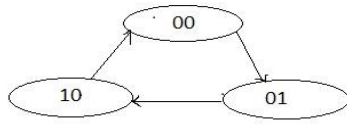
6.2.1 The 0 to 2 counter

Step 1 decide the number of flip flops.

The counter needs 2 bits to count so we have used two jk flip flops for design.

Step 2 state diagram and circuit excitation table.

The state diagram of the 2 bit counter normally consists of 4 states but as we want to count up to 2 so it will have 3 states.

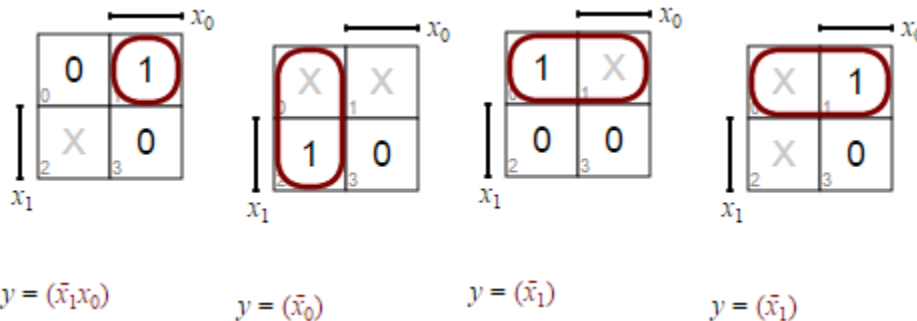


The excitation table will be

Initial state	Final state	J1	K1	Jo	Ko
00	01	0	X	1	X
01	10	1	X	X	1
10	00	x	1	0	X

Resolving k map for the outputs

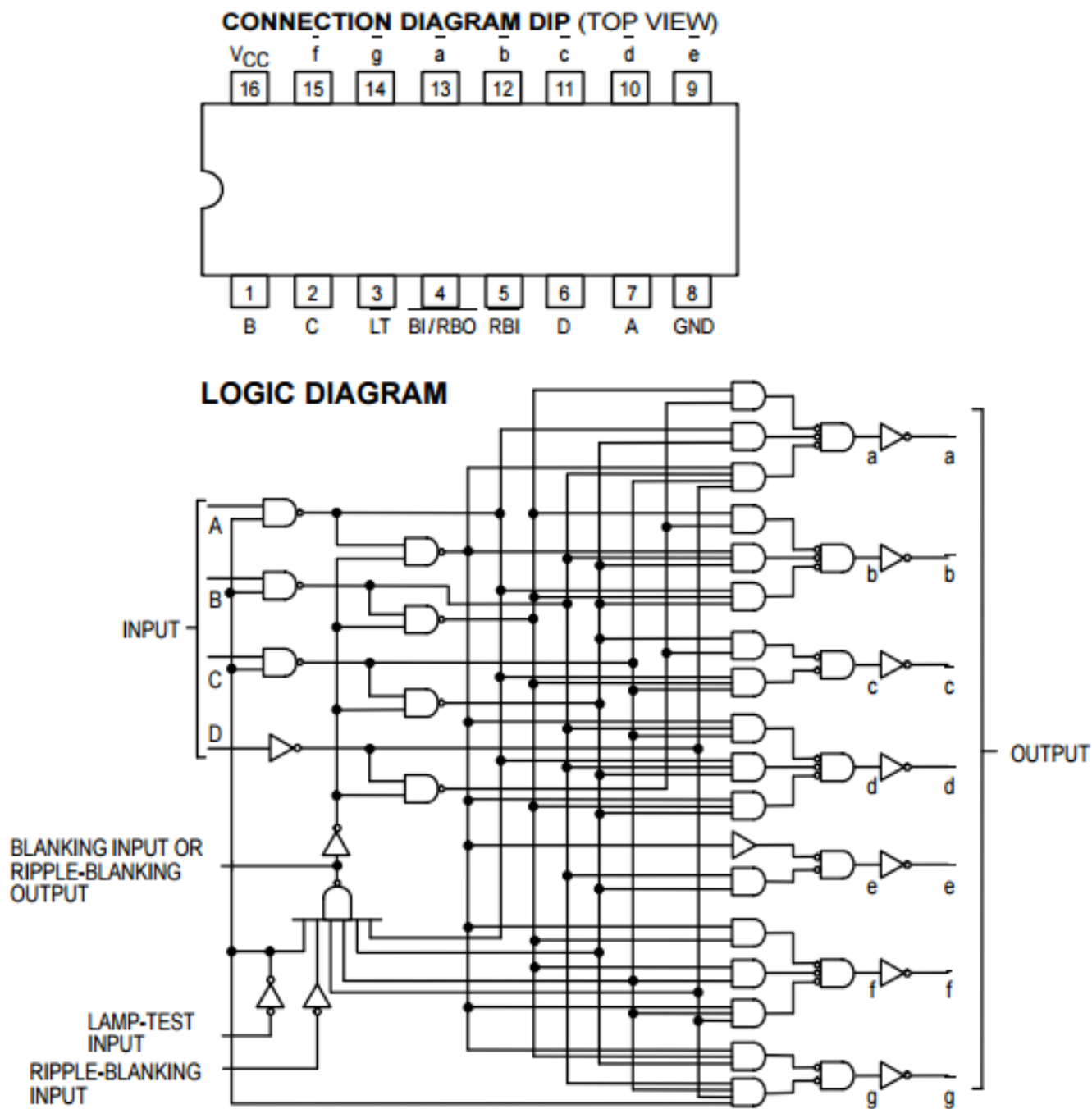
For J1, K1, Jo, Ko respectively



6.3 BCD to 7 segment decoder

In this project we have used what's called the basic 7 segment decoder 74LS47 decoder which can decode the bcd output of the flip flops in to 7 segment display.

74LS47 are Low Power Scotty BCD to 7-Segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input. The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN54/74LS47 are designed to withstand the relatively high voltages required for 7-segment indicators. These outputs will withstand 15 V with a maximum reverse current of 250 μ A. Indicator segments requiring up to 24 mA of current may be driven directly from the SN74LS47 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions



TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS							OUTPUTS							NOTE
	$\overline{\text{LT}}$	$\overline{\text{RBI}}$	D	C	B	A	$\overline{\text{BI/RBO}}$	$\overline{\text{a}}$	$\overline{\text{b}}$	$\overline{\text{c}}$	$\overline{\text{d}}$	$\overline{\text{e}}$	$\overline{\text{f}}$	$\overline{\text{g}}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	A
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	A
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	B
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	C
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	D

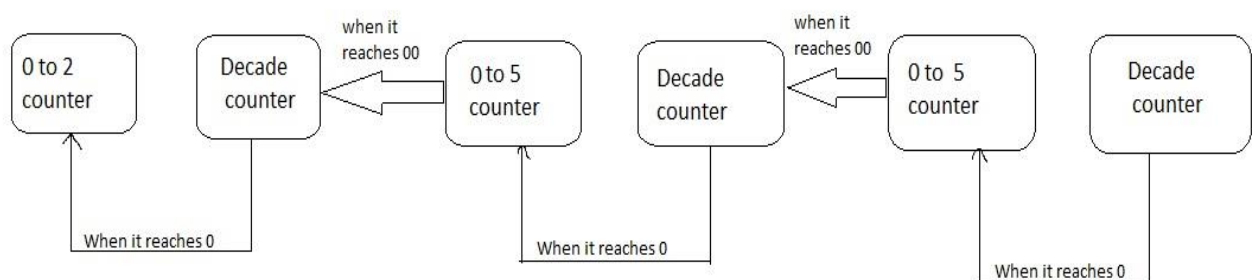
H = HIGH Voltage Level

L = LOW Voltage Level

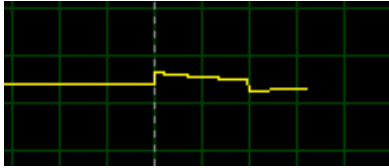
X = Immaterial

6.4 The working principles of the circuit

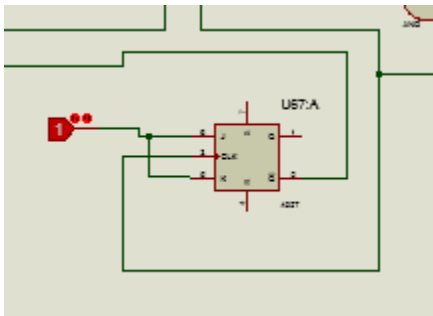
Regarding digital clocks the second and the minute has to count 0 up to 59 this done while the decade counter counts 0 to 9 and restart back to 0 it will give one clock pulse to the left counter so that the display will be 10 and continue like this when the 1 to 5 counter reaches its maximum value it will reset itself and restart from 0 again.



The first 0000 clock also gives a high voltage to the next block also but the voltage is applied simultaneously with the clock so there would be no change in the output means it will stay at 0000. But while simulating the circuit we have encounter one shot in voltage that will happen when the counter starsfer from 9 to 10.



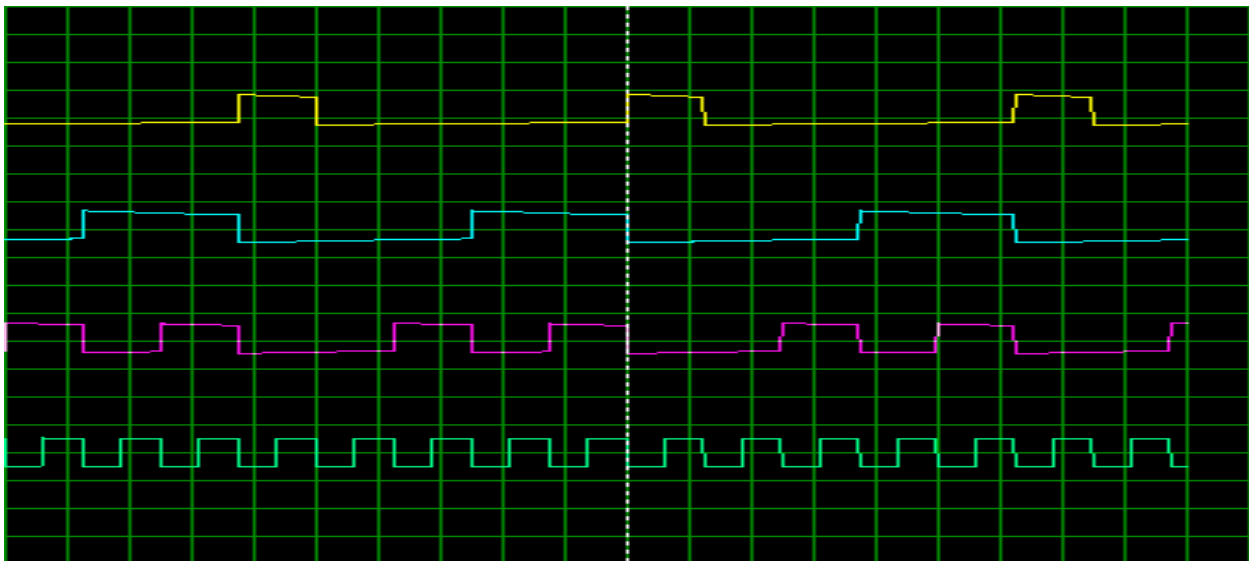
This is caused by the small delay in the flip flops and we have corrected this with another jk flip flop. As this happens at the first it will make the the minut counter to 0001 before the second reaches the second cycle. So the first clock in every cycle has to be eliminated so we have given the clock output of the second to the clock input of the flip flop and give the inverted output of the flip flop to the input of the minute clock.



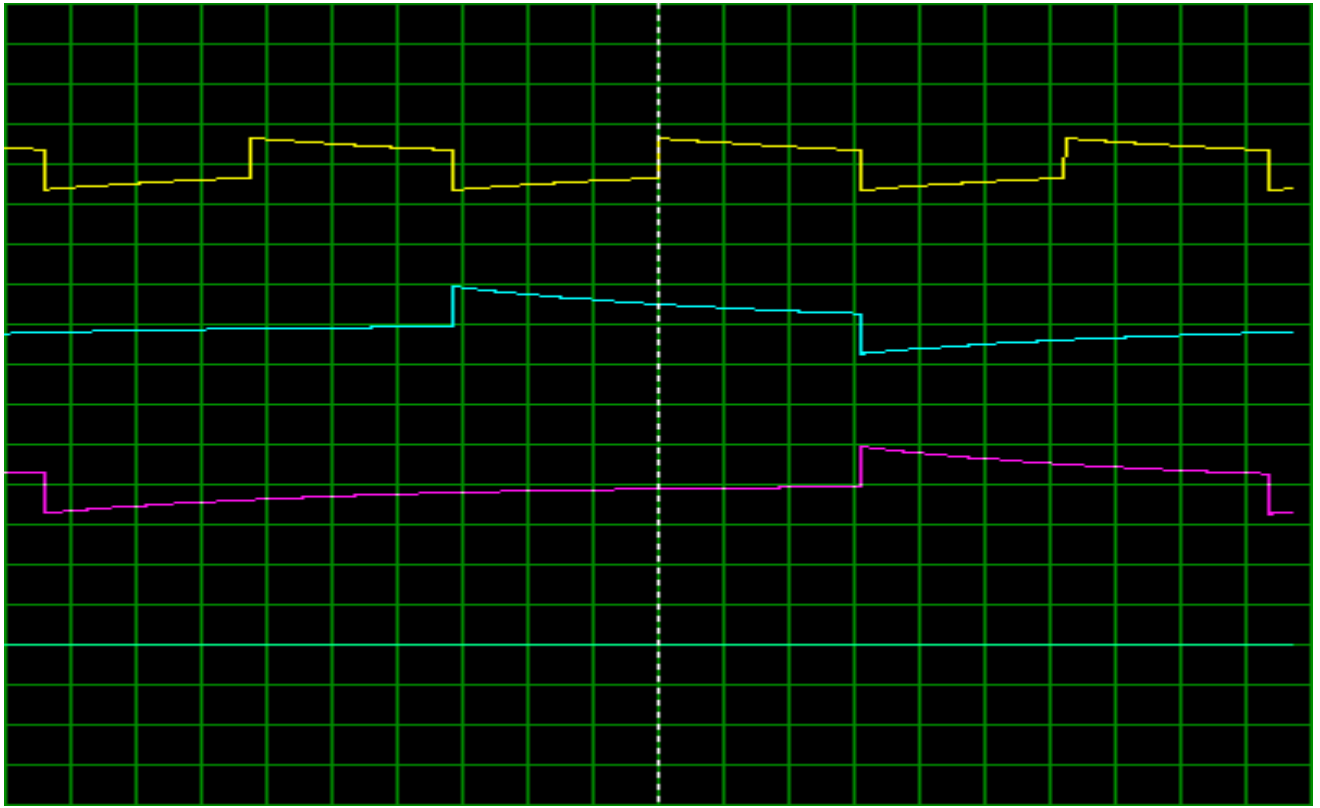
This type of cascading also used for cascading the hour to the minute counter.

6.5 Simulation results

From the decade counter when the outputs are viewed by oscilloscope it will become starting from the list significant bit(yellow) to the most(green).



The output of the 0-5 counter



References

- [1] https://en.wikipedia.org/wiki/Digital_clock
- [2] <http://www.mathematik.uni-marburg.de/~thormae/lectures/ti1/code/karnaughmap/>
- [3] Thomas L. Floyd, "**Digital Fundamentals**", Seventh Edition, Prentice-Hall International, Inc., 2000.
- [4] Donald D. Givone, "**Digital Principles and Designs**", McGraw- Hill 2003.
- [5] Victor P. Nelson, H. Try Nagle, Bill D. Carroll, and J. David Irwin, "**Digital Logic Circuit Analysis & Design**", Prentice-Hall Englewood Cliffs.NJ, 1995.
- [6] HCF4027B datasheet
- [7] 74LS47 datasheet