
STM32
CubeMX

1. Description

1.1. Project

Project Name	movie_pinout_v2 pinout cubemx
Board Name	custom
Generated with:	STM32CubeMX 6.4.0
Date	01/14/2023

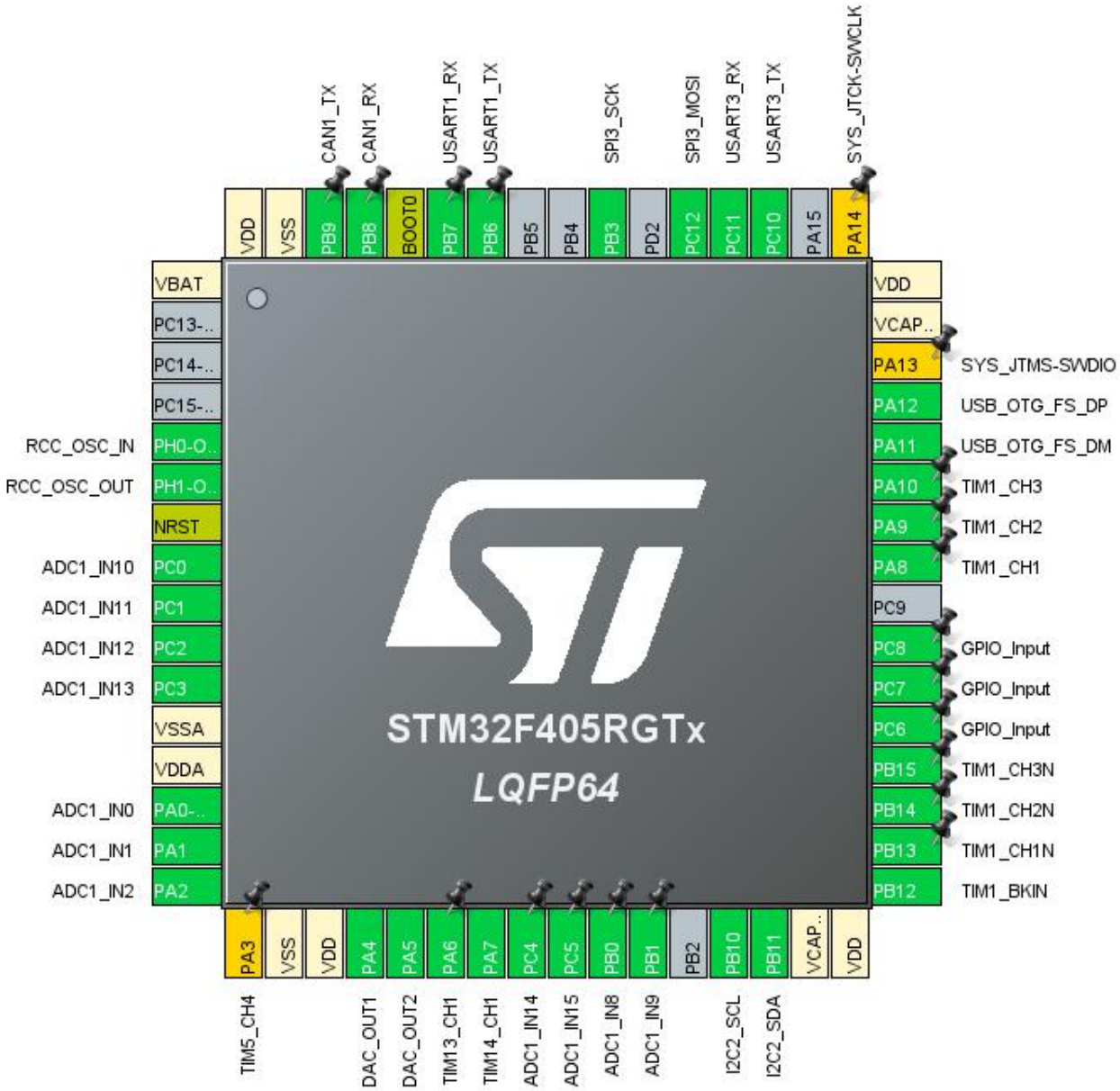
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F405/415
MCU name	STM32F405RGTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



3. Pins Configuration

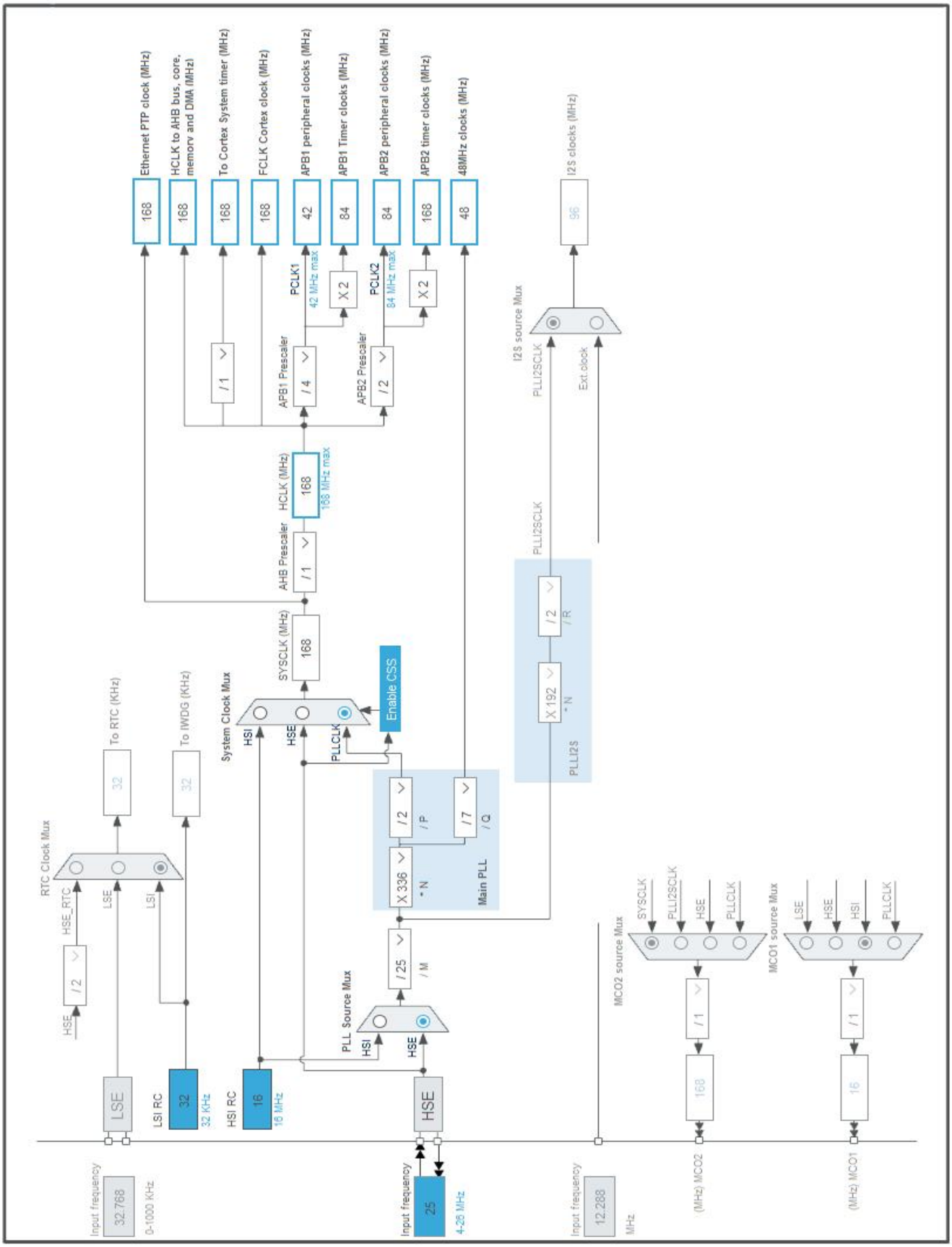
Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	ADC1_IN10	
9	PC1	I/O	ADC1_IN11	
10	PC2	I/O	ADC1_IN12	
11	PC3	I/O	ADC1_IN13	
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	ADC1_IN0	
15	PA1	I/O	ADC1_IN1	
16	PA2	I/O	ADC1_IN2	
17	PA3 *	I/O	TIM5_CH4	
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	DAC_OUT1	
21	PA5	I/O	DAC_OUT2	
22	PA6	I/O	TIM13_CH1	
23	PA7	I/O	TIM14_CH1	
24	PC4	I/O	ADC1_IN14	
25	PC5	I/O	ADC1_IN15	
26	PB0	I/O	ADC1_IN8	
27	PB1	I/O	ADC1_IN9	
29	PB10	I/O	I2C2_SCL	
30	PB11	I/O	I2C2_SDA	
31	VCAP_1	Power		
32	VDD	Power		
33	PB12	I/O	TIM1_BKIN	
34	PB13	I/O	TIM1_CH1N	
35	PB14	I/O	TIM1_CH2N	
36	PB15	I/O	TIM1_CH3N	
37	PC6 **	I/O	GPIO_Input	
38	PC7 **	I/O	GPIO_Input	
39	PC8 **	I/O	GPIO_Input	
41	PA8	I/O	TIM1_CH1	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
42	PA9	I/O	TIM1_CH2	
43	PA10	I/O	TIM1_CH3	
44	PA11	I/O	USB_OTG_FS_DM	
45	PA12	I/O	USB_OTG_FS_DP	
46	PA13 *	I/O	SYS_JTMS-SWDIO	
47	VCAP_2	Power		
48	VDD	Power		
49	PA14 *	I/O	SYS_JTCK-SWCLK	
51	PC10	I/O	USART3_TX	
52	PC11	I/O	USART3_RX	
53	PC12	I/O	SPI3_MOSI	
55	PB3	I/O	SPI3_SCK	
58	PB6	I/O	USART1_TX	
59	PB7	I/O	USART1_RX	
60	BOOT0	Boot		
61	PB8	I/O	CAN1_RX	
62	PB9	I/O	CAN1_TX	
63	VSS	Power		
64	VDD	Power		

** The pin is affected with an I/O function

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	movie_pinout_v2 pinout cubemx
Project Folder	C:\Google Drive\hardware design\motor controller
Toolchain / IDE	EWARM V8.32
Firmware Package Name and Version	STM32Cube FW_F4 V1.26.2
Application Structure	Basic
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ADC1_Init	ADC1
5	MX_CAN1_Init	CAN1
6	MX_DAC_Init	DAC
7	MX_I2C2_Init	I2C2
8	MX_SPI3_Init	SPI3
9	MX_TIM1_Init	TIM1
10	MX_TIM13_Init	TIM13
11	MX_TIM14_Init	TIM14

Rank	Function Name	Peripheral Instance Name
12	MX_USART1_UART_Init	USART1
13	MX_USART3_UART_Init	USART3
14	MX_USB_OTG_FS_PCD_Init	USB_OTG_FS

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F405/415
MCU	STM32F405RGTx
Datasheet	DS8626_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

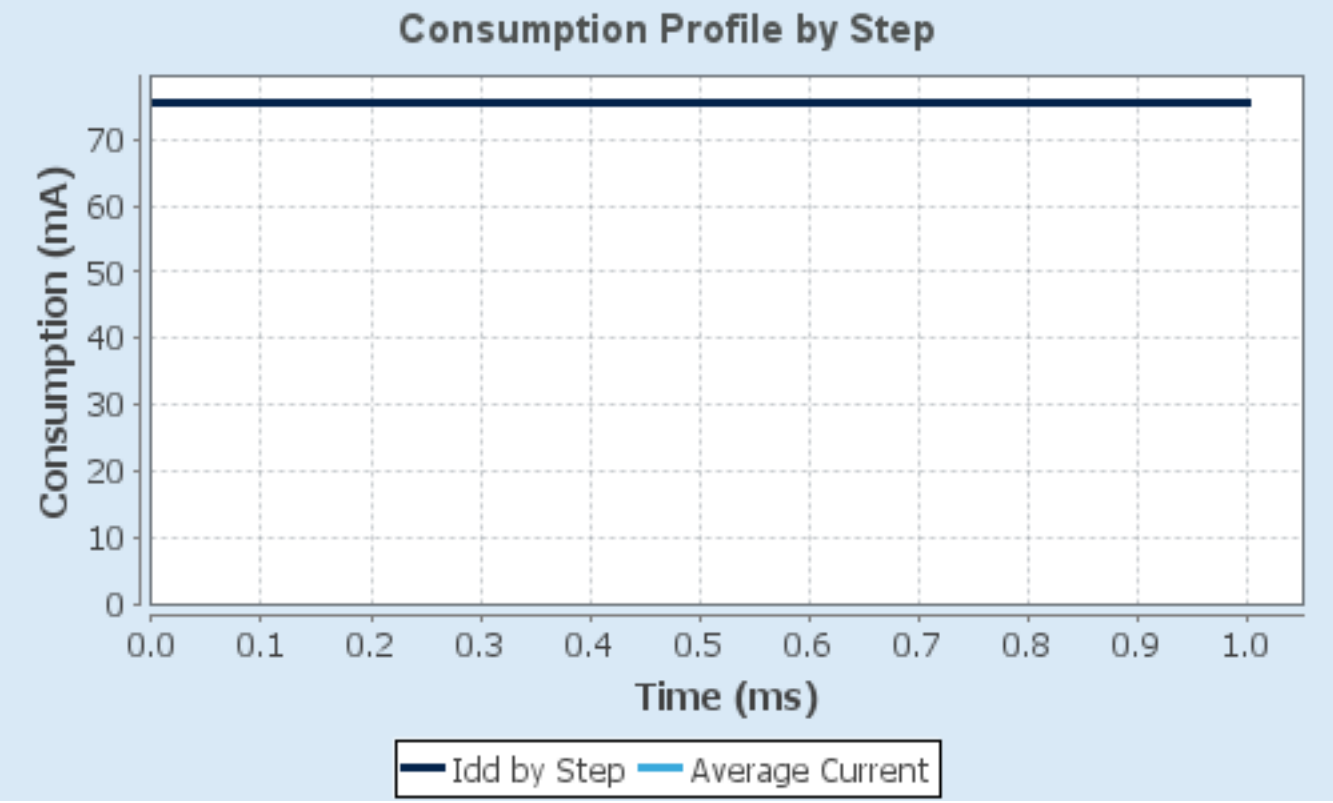
6.4. Sequence

Step	Step1
Mode	RUN
Vdd	3.3
Voltage Source	Vbus
Range	Scale1-High
Fetch Type	FLASH
CPU Frequency	168 MHz
Clock Configuration	HSE PLL
Clock Source Frequency	4 MHz
Peripherals	ADC1 ADC2 ADC3 CAN1 DAC:OUT1 DMA1 DMA2 I2C1 TIM1 TIM2 TIM3 TIM4 TIM5 TIM6 TIM8 TIM14 USART1 USART3 USB_OTG_FS
Additional Cons.	0 mA
Average Current	75.6 mA
Duration	1 ms
DMIPS	210.0
Ta Max	93.52
Category	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	75.6 mA
Battery Life	0	Average DMIPS	210.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
70
60
50
40
30
20
10
0
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN0

mode: IN1

mode: IN2

mode: IN8

mode: IN9

mode: IN10

mode: IN11

mode: IN12

mode: IN13

mode: IN14

mode: IN15

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. CAN1

mode: Activated

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	16
Time Quantum	**380.95238095238096 ***
Time Quanta in Bit Segment 1	1 Time
Time Quanta in Bit Segment 2	1 Time
Time for one Bit	**1142 ***
Baud Rate	**875000 ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

7.3. DAC

mode: OUT1 Configuration

mode: OUT2 Configuration

7.3.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None

7.4. I2C2

I2C: I2C

7.4.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.6. SPI3

Mode: Half-Duplex Master

7.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***
Baud Rate	**2.625 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	**Enabled ***
CRC Polynomial	X1+X3
NSS Signal Type	Software

7.7. SYS

Timebase Source: SysTick

7.8. TIM1

Channel1: Output Compare CH1 CH1N

Channel2: Output Compare CH2 CH2N

Channel3: Output Compare CH3 CH3N

mode: Activate-Break-Input

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Enable

BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	0

Output Compare Channel 1 and 1N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

Output Compare Channel 2 and 2N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

Output Compare Channel 3 and 3N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

7.9. TIM13

mode: Activated

Channel1: PWM Generation CH1

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.10. TIM14

mode: Activated

Channel1: PWM Generation CH1

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.11. USART1

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.12. USART3

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.13. USB_OTG_FS

Mode: Device_Only

7.13.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	
	PC2	ADC1_IN12	Analog mode	No pull-up and no pull-down	n/a	
	PC3	ADC1_IN13	Analog mode	No pull-up and no pull-down	n/a	
	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC1_IN15	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
CAN1	PB8	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB9	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC_OUT2	Analog mode	No pull-up and no pull-down	n/a	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	**Pull-up ***	**Very High ***	
	PB11	I2C2_SDA	Alternate Function Open Drain	**Pull-up ***	**Very High ***	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI3	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB3	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
TIM1	PB12	TIM1_BKIN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	TIM1_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB14	TIM1_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	TIM1_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM13	PA6	TIM13_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM14	PA7	TIM14_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART3	PC10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
Single Mapped Signals	PA3	TIM5_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
GPIO	PC6	GPIO_Input	Input mode	**Pull-up ***	n/a	
	PC7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	**Very High ***

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA2 stream0 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
CAN1 TX interrupts	unused		
CAN1 RX0 interrupts	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
USART1 global interrupt	unused		
USART3 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
SPI3 global interrupt	unused		
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused		
USB On The Go FS global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

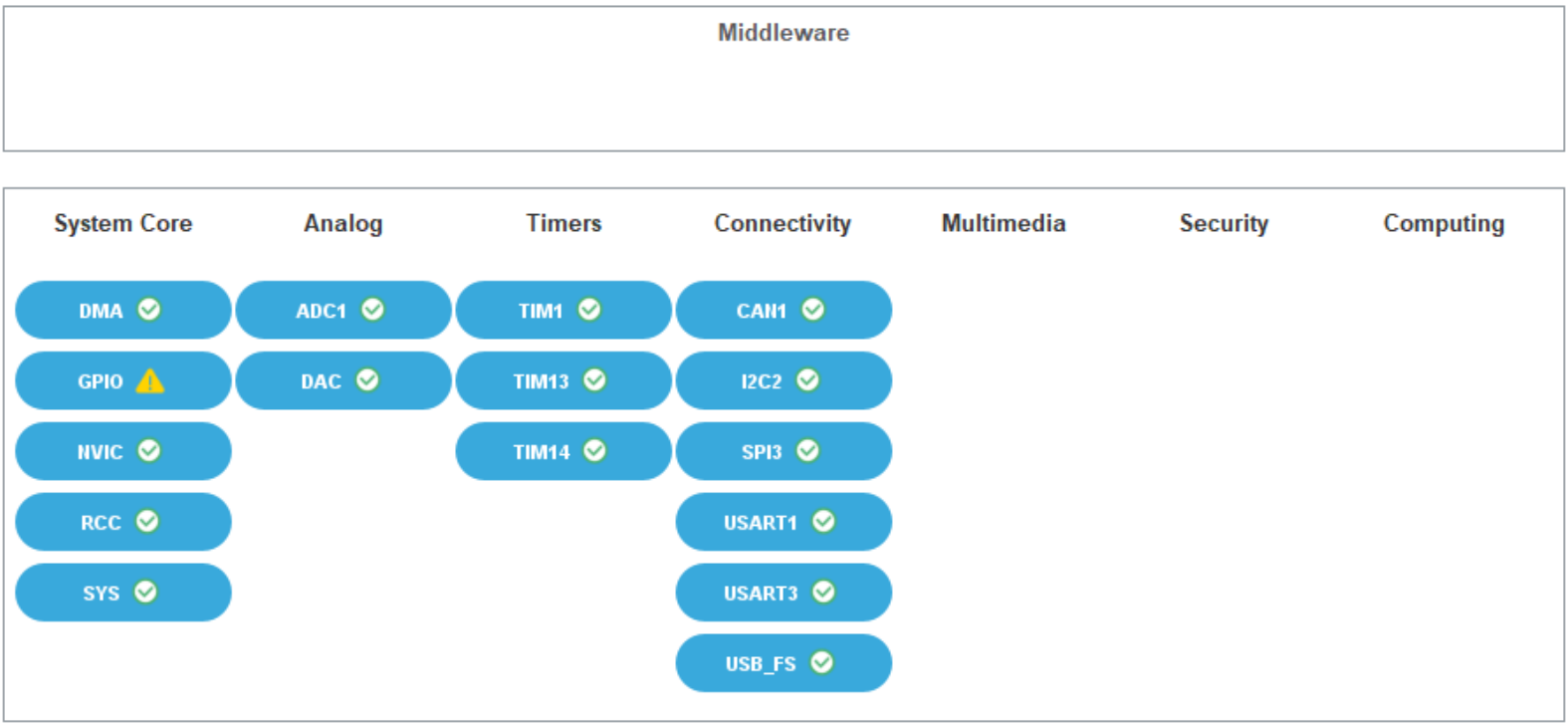
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA2 stream0 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00037051.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00031020.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00037591.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00025071.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00050879.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf

Application note	http://www.st.com/resource/en/application_note/DM00154959.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00213525.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00263732.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf