UNIVERSITEIT•STELLENBOSCH•UNIVERSITY
jou kennisvennoot • your knowledge partner

E344 Assignment 2

Daniel von Eschwege
21785155

Report submitted in partial fulfilment of the requirements of the module Design (E) 344 for the degree Baccalaureus in Engineering in the Department of Electrical and Electronic Engineering at Stellenbosch University.

October 24, 2020

UNIVERSITEIT•STELLENBOSCH•UNIVERSITY
jou kennisvennoot • your knowledge partner

Plagiaatverklaring / *Plagiarism Declaration*

1. Plagiaat is die oorneem en gebruik van die idees, materiaal en ander intellektuele eiendom van ander persone asof dit jou eie werk is.
   Plagiarism is the use of ideas, material and other intellectual property of another's work and to present is as my own.

2. Ek erken dat die pleeg van plagiaat 'n strafbare oortreding is aangesien dit 'n vorm van diefstal is.
   I agree that plagiarism is a punishable offence because it constitutes theft.

3. Ek verstaan ook dat direkte vertalings plagiaat is.
   I also understand that direct translations are plagiarism.

4. Dienooreenkomstig is alle aanhalings en bydraes vanuit enige bron (ingesluit die internet) volledig verwys (erken). Ek erken dat die woordelikse aanhaal van teks sonder aanhalingstekens (selfs al word die bron volledig erken) plagiaat is.
   Accordingly all quotations and contributions from any source whatsoever (including the internet) have been cited fully. I understand that the reproduction of text without quotation marks (even when the source is cited) is plagiarism

5. Ek verklaar dat die werk in hierdie skryfstuk vervat, behalwe waar anders aangedui, my eie oorspronklike werk is en dat ek dit nie vantevore in die geheel of gedeeltelik ingehandig het vir bepunting in hierdie module/werkstuk of 'n ander module/werkstuk nie.
   I declare that the work contained in this assignment, except where otherwise stated, is my original work and that I have not previously (in its entirety or in part) submitted it for grading in this module/assignment or another module/assignment.

21785155	
Studentenommer / *Student number*	Handtekening / *Signature*
D.H. von Eschwege	October 24, 2020
Voorletters en van / *Initials and surname*	Datum / *Date*

Contents

Declaration i

List of Figures iv

List of Tables v

Nomenclature vi

1. System design 1

1.1. System overview 1

2. Voltage regulation 3

2.1. Introduction 3

2.2. Design 3

2.3. Results 4

2.4. Summary 5

3. Temperature sensor conditioning circuit 6

3.1. Intro 6

3.2. Design 6

3.3. Results 8

3.4. Summary 9

4. Heart rate sensor 10

4.1. Introduction 10

4.2. Design 10

4.3. Results 12

4.4. Summary 14

5. Calibration and digitisation 15

5.1. Temperature sensor 15

5.1.1. Analytical Design 15

5.1.2. Empirical Design 15

5.2. Heart rate sensor 15

6. System and conclusion 16

6.1. System 16

6.2. System 16

6.3. Lessons learnt 17

Bibliography 18

A. Social contract 19

B. GitHub Activity Heatmap 20

C. Stuff you want to include 21

D. Stuff you want to include 22

List of Figures

1.1. System Diagram 1

2.1. Linear Voltage Regulator 3
2.2. Switchmode Voltage Regulator 4
2.3. Switchmode Voltage Regulator Noise 4
2.4. Linear Voltage Regulator Output 5
2.5. Switchmode Voltage Regulator Output 5

3.1. Temperature Sensor Circuit 7
3.2. Simulated bode plot of filter 8
3.3. Complete Circuit Output 9

4.1. Complete Circuit 10
4.2. Fast fourier transform of stimulus 11
4.3. Filter input and output 12
4.4. Frequency response of filters 13
4.5. Signal Conditioning 13
4.6. Full input versus output range 13
4.8. Total current usage 14

List of Tables

2.1. Comparison of Voltage Regulators 4

3.1. Temperatures and Corresponding Voltage Levels 6

Nomenclature

Variables and functions

f_c	Cutoff frequency
V_{REF}	Reference voltage
A_v	Gain
β	Feedback fraction
V_{CM}	Common-mode voltage
V_{ID}	Differential-mode voltage
η	Efficiency
ω_n	Natural Frequency
t_r	Rise time (90%)
V_{ref}	Reference Voltage

Acronyms and abbreviations

PWM	Pulse-width modulation
FFT	Fast Fourier transform
DC	Direct Current
Q-factor	Quality factor
BPM	Beats per minute
UTP	Upper trip point
LTP	Lower trip point
AC	Alternating Current
DC	Direct Current
ADC	Analog-to-Digital Converter

Chapter 1

System design

1.1. System overview

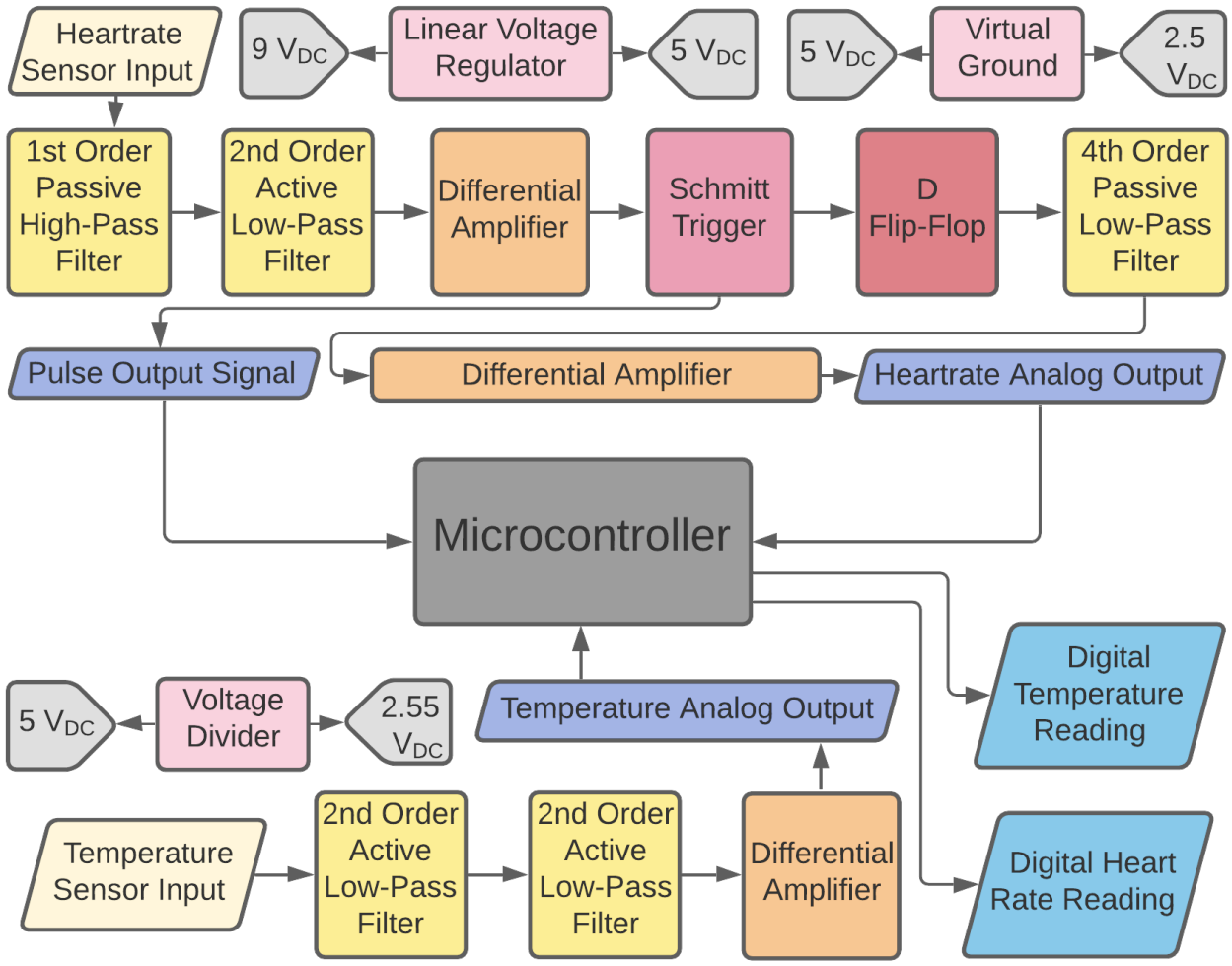


Figure 1.1: System Diagram

A health monitoring system is designed, consisting of a temperature sensor and an optic heart-rate monitor, interacting with a microcontroller. Figure 1.1 provides an overview. Since physical sensor measurements are ill-suited for digital interfacing, the main focus of this report is the conditioning, filtering and amplification of the aforementioned.

The temperature sensor input is subject to noise, has an unwanted DC offset and an amplitude of insufficient magnitude for AD-conversion. Two second-order low-pass filters were cascaded to clear the signal of noise. This may seem excessive at first, but the cascaded setup allows for the use of less costly components (see Section 3.2), as well as producing an

output signal subject to very low noise (see Section 3.3). Following filtering, amplification is required. Since the filtered signal still contains a DC offset, and the differential amplifier requires a virtual ground, the voltage divider connects to the amplifier in such a way as to simultaneously remove the input DC offset and add the virtual ground. The signal is thus amplified to the degree required by a microcontroller ADC.

The heart-rate sensor input is to be converted to a pulse signal and an analogue output, corresponding to heart-beats and the heart-rate respectively. On account of the noise present in the sensor input, signal conditioning is required. Furthermore, the small amplitude of the sensor input necessitates amplification. A first order passive high-pass filter and a second order active low-pass filter attenuate both high- and low-frequency noise. Despite designing with maximal simplicity in mind to reduce cost and complexity, the filters still performing more than adequately. Thereafter, a differential amplifier produces a signal with a large amplitude and little noise. A Schmitt Trigger then outputs a pulse signal with a frequency corresponding to the heart-rate. The Schmitt Trigger was chosen as it provides a noise margin via hysteresis. An analogue voltage output is required for the microcontroller - filtering and peak detection using diodes was considered but discarded, as non-linear diodes result in extremely slow simulation. Rather, the pulse output signal was converted to a pulse-width modulated signal, where the frequency of the former determines the duty cycle of the latter. This was done as PWM signals lend themselves to conversion-to-analogue by simple filtering. The PWM signal was obtained by using a D Flip-Flop and a RC-circuit **(see section 4.2)**. A fourth order passive RC filter is then used - passive components reduce cost, current usage and simulation time. The filter is of high order as to minimize noise while meeting the settling time requirement. Finally, the signal is amplified to achieve the required range.

A microcontroller produces digital readings of the temperature and heart-rate by using the analogue output voltage (representative of the temperature measurement) and the pulse output signal (representing the the heart-rate) in a calibration formula programmed into the microcontroller, where the former is linearly scaled and the latter is converted to a digital reading using the signal frequency. The frequency is detected by measuring the time-interval between rising edges.

A voltage regulator supplies power to all sub-circuits of which the system is comprised. Capable of a maximum current of 100 mA at 5 V, it is more than sufficient to supply the current drawn by Assignments 1, 2 and 3 - 12.8 mA, 13.0 mA and 50 mA respectively, where the current draw for Assignment 3 is estimated based on the typical current draw of a microcontroller of the type that would suffice for analogue-to-digital conversion of the heart-rate and temperature data [**?**]. All circuits were designed with conservative current use in mind as to increase efficiency of the health-monitoring system.

Chapter 2

Voltage regulation

2.1. Introduction

Given a 9 V_{DC} battery, a voltage regulator is required to reduce the voltage level to 5 V_{DC}, as this is the level required by the operational amplifiers used in the rest of the circuit. Two voltage regulators were considered: the LM7805 linear regulator as well as the LM2595 switchmode regulator, which were both analysed with regards to efficiency and noise by means of calculations and simulations. According to the literature, the linear regulator produces insignificant levels of noise, but has low power efficiency of around 50% for input and output of 9 V_{DC} and 5 V_{DC} [1] respectively. The switchmode regulator can provide power efficiency of around 85%, but outputs a considerable amount of noise [2]. With the aforementioned in mind, both of the regulators were simulated (Section 2.2) to determine the best trade-off between low noise and efficiency.

2.2. Design

The LM7805 chip and its required peripheral circuit is shown in Figure 2.1. Component values were obtained from the datasheet [1]. For testing purposes, a 50 Ω load was connected to the regulator, drawing 100 mA.

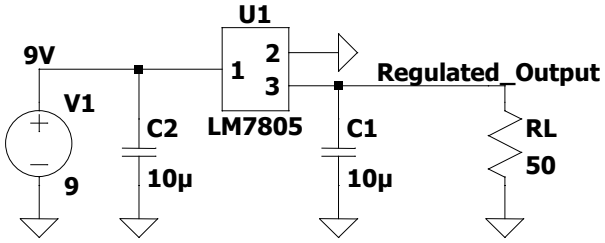


Figure 2.1: Linear Voltage Regulator

The LM2595 chip is shown in figure 2.2, built into the required peripheral circuit. Capacitor and inductor values were obtained from the datasheet [2]. Resistor values were calculated:

$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) \quad \text{where } V_{REF} = 1.23V$$

Selecting R_1 as 1 kΩ, with V_{out} as 5 V gives R_2 as 3065 Ω. For testing purposes, a 50 Ω load was connected to the regulator, drawing 100 mA.

Since the provided circuit includes a resistor (R_{sense}) between the voltage source and the voltage regulator, the voltage drop over the resistor will be $V = IR = (0.01238)(0.01) = 123.8\mu$V. Considering that the power source supplies 9 V, the aforementioned voltage drop is negligible - it is not nearly enough to approach the dropout voltages of the voltage regulators, which are 6.7 V for the LM7805 and 5.8 V for the LM2595 in the case of a 5 V output.

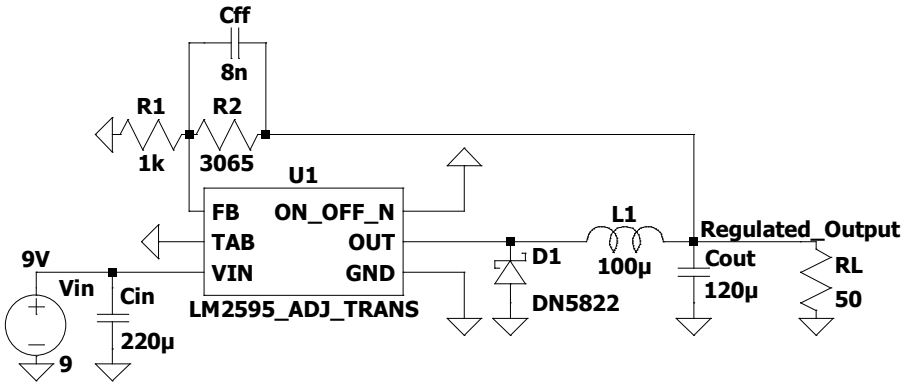


Figure 2.2: Switchmode Voltage Regulator

2.3. Results

The input and output power measurements are displayed in table 2.1. Comparing the efficiency of the respective regulators, it is clear that the switchmode regulator is considerably more efficient. However, simulation results in a settling time of 1.24 ms, which is quite slow. Furthermore, the switchmode regulator creates noise levels of up to 950 μV_{pp} in the output, as can be seen in figure 2.3, whereas the linear regulator produces almost no noise (figure 2.4). Noise is a problem, as the large gain of the differential amplifier will increase the noise levels, which will distort the output.

Table 2.1: Comparison of Voltage Regulators

	I_{in} [mA]	I_{out} [mA]	P_{in} [mW]	P_{out} [mW]	η [%]
LM7805	105.06	100.05	945.54	500.55	52.93
LM2595	57.54	99.65	517.86	496.6	95.89

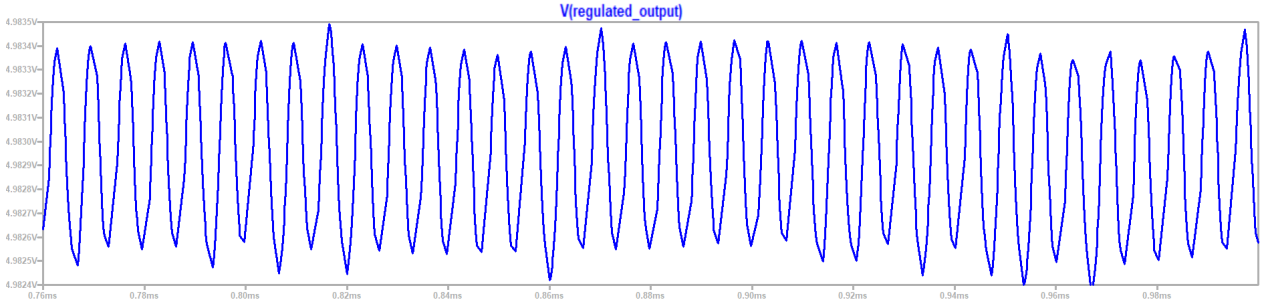


Figure 2.3: Switchmode Voltage Regulator Noise

The output graphs of the voltage regulators are shown in figures 2.4 and 2.5, and clearly demonstrate that both regulators produce the desired output current and voltage. The input current for the switchmode regulator is not shown as it obscures the graph, but it has an

average value of 57.54 mA. All relevant values can be found in table 2.1.

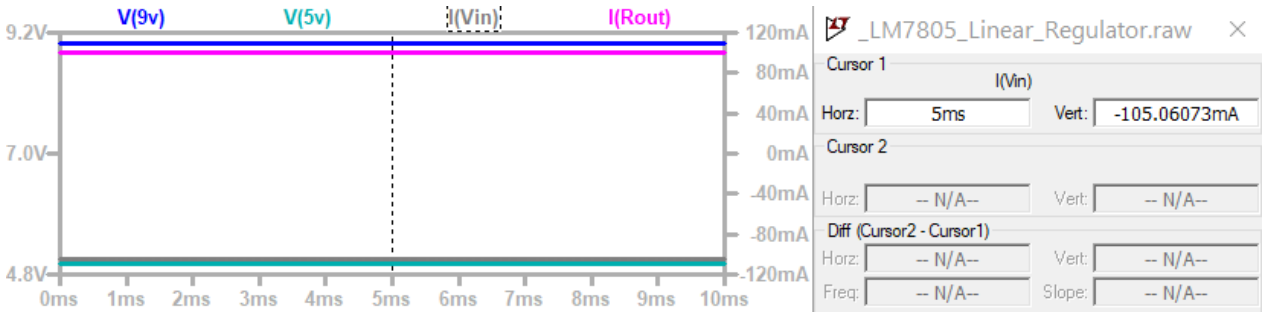


Figure 2.4: Linear Voltage Regulator Output

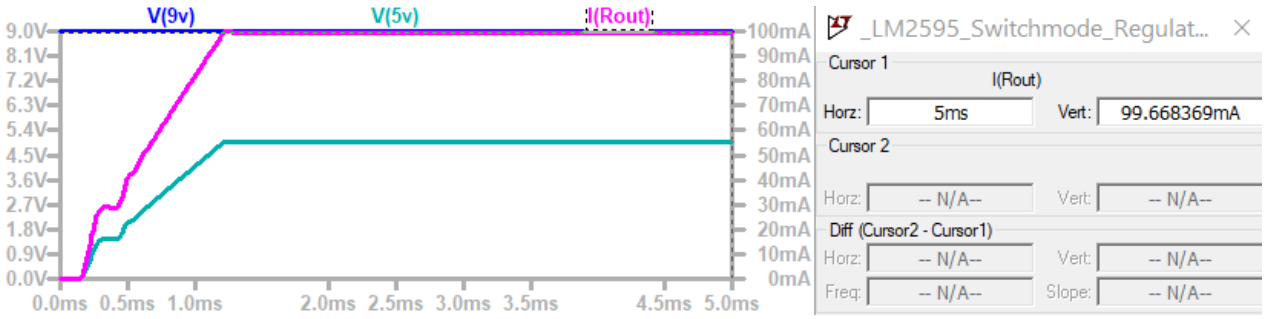


Figure 2.5: Switchmode Voltage Regulator Output

2.4. Summary

Concluding, it has been shown that both regulators behave as expected, but that the levels of noise present in the switchmode regulator make it unsuitable for the design at hand, as input signals, and thus the noise as well, will be amplified to levels of noise in the output signal that are unacceptable for an ADC input. The linear regulator will therefore be used. This choice was made despite the fact that the switchmode regulator is approximately 40% more efficient than the linear regulator. However, since the total current drawn is still very low, efficiency is not of concern.

Chapter 3

Temperature sensor conditioning circuit

3.1. Intro

The temperature sensor signal presents as DC with 50 Hz AC noise superimposed. The sensor output amplitude is too small to act as ADC input and the desired range is only from 34°C to 42°C. The two aforementioned considerations necessitate amplification of the relevant part of the temperature sensor signal to a 0 to 5 V range. Conditioning circuitry is thus required, namely a filter, an offset removing subcircuit, as well as an amplifier. The filter attenuates the AC noise, the offset subcircuit removes enough of the DC offset as to obtain an output signal centered around 2.5 V, ensuring the largest possible output swing. Finally, the amplifier increases the magnitude of the input signal in order to be suitable as input for an ADC.

3.2. Design

The amplifier was designed first, as its gain serves as the determining factor for the amount of noise reduction that is required from the filter. A TLC2272 op-amp was chosen as it allows for an output very close to its rails. Since the output signal has to be centered around 2.5 V, a differential amplifier was decided upon, allowing for adjustment of the negative input in order to determine the output offset. The zero-reference temperature sensor voltage (V_{zero}) is 440 mV, and increases by 35 mV for every 1°C (V_Δ). Therefore $V_{temp} = V_{zero} + V_\Delta \times Temp$. As shown in table 3.1, the maximum input voltage swing equals $1.91 - 1.63 = 0.28$V, and has a DC offset of 1.77 V. Amplification is needed to reach an output voltage swing of 5 V, which, combined with a 2.5 V DC offset, ensures that the circuit uses the input range in accordance to specification, while excluding the lower and upper temperature ranges (i.e. below 34°C and above 42°C). Therefore:

Table 3.1: Temperatures and Corresponding Voltage Levels

Temperature [°C]	32	38	42
Voltage [V]	1.63	1.77	1.91

$$A_v = \frac{V_{out}}{V_{in}} = \frac{5}{0.28} = 17.86$$

Considering the current design requirement of 25 mA maximum, R_{input} is selected as 10 kΩ, which will therefore, at the highest possible voltage level of 5 V, draw 0.5 mA. This gives $R_{feedback} = 178.6\text{k}\Omega$, according to $A_v = \frac{R_{feedback}}{R}$ [3]. R_{input} corresponds to R_1 and R_2, and

$R_{feedback}$ to R_3 and R_4 in the design diagram (figure 3.1), which is shown here already as to aid with explanation of the design process. $R_{feedback}$ required adjustment to 230 kΩ upon simulation due to the non-linear A_v curve characteristic of op-amps.

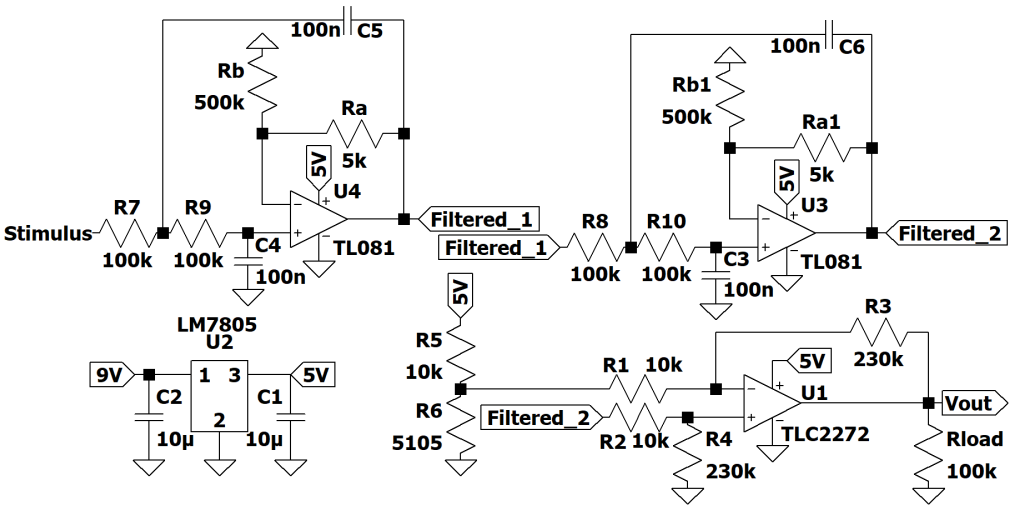


Figure 3.1: Temperature Sensor Circuit

Two points require consideration:

1. The DC offset of the input signal is undesired and has to be removed in order to obtain a zero-mean input signal. This can be achieved by designing another subcircuit that makes use of another op-amp, for example. This adds to the cost and complexity of the circuit.

2. The output signal has to be centered around 2.5 V. This means that a DC offset has to be added in the form of a virtual ground.

When considered in conjunction with each other, the DC offset alteration can be resolved in one step, thereby reducing cost and complexity significantly. The decision was therefore made to use a differential amplifier with the input signal connected to the positive input, after which the voltage required at the negative input can be calculated in such a way as to simultaneously subtract the offset and add the virtual ground in one step, thereby producing an output DC offset of 2.5 V. This approach also simplifies the design procedure, as it renders a separate virtual ground completely superfluous, thereby also removing the need to perform any virtual ground calculations per se. (Lecture Video 2, minute 11 [4] mentions this to be an acceptable approach). For a non-inverting amplifier, the calculation thus reduces to a simple differential amplifier gain formula [3]:

$$V_{out} = \frac{R_{feedback}}{R}\left(V_{in+} - V_{in-}\right) \quad \rightarrow \quad 2.5 = \frac{230000}{10000}\left(1.77 - V_{in-}\right)$$

With V_{out} as 2.5 V, V_{in+} as 1.77 V and the resistor values as calculated previously, $V_{in-} = 1.661$ V. The voltage at V_{in-} can be set by means of a voltage divider circuit, which takes 5 V as input and is calculated as follows (resistor names in formulae are selected to

conform with Figure 3.1): $V_{in-} = 5(\frac{R_6}{R_6 \times R_5})$. Selecting R_5 as 10 kΩ gives $R_6 = 5.0\,\text{k}\Omega$. Here, the common-mode voltage, V_{IC}, needs consideration; the TLC2272 can operate with a common-mode voltage of V_{DD-} to $V_{DD+} - 1.5$ [5]. Since $V_{in+_{max}}$ is 1.91 V and V_{in-} is 1.66 V, the largest possible common mode voltage is $V_{IC} = \frac{1.91+1.66}{2} = 1.79\,\text{V}$, which is well below the maximum limit. Since V_{in-} stays constant, the lower limit will never be reached either.

Simulation was used to select a filter, and has shown the following: a passive low-pass filter is very simple, but produces too much noise and does not meet the settling time requirement. The active low-pass filter meets both the noise and settling time requirements, but requires the TLC2272 op-amp to do so. Since a single TLC2272 op-amp is more expensive than multiple TL081 op-amps, the decision was made to rather use cascaded second order low-pass filters, using the TL081. This is somewhat more complex, but lowers the cost, as the final circuit now only uses three op-amps, two of which are the cheaper TL081 models. Assignment 3 further motivates the decision for increased filter complexity, as the cascaded setup produces an output signal with extremely low noise, which is indispensable for meeting the bonus requirements during calibration and digitisation - see section 5.1.2. Following selection, the filter is designed: A filter gain of close to unity is desired; for $R_A = 500\,\text{k}\Omega$, $R_A = 5\,\text{k}\Omega$, according to the formula: $A_v = 1 + \frac{R_A}{R_B}$ [6]. The settling time requirement of 100 ms means that a cutoff frequency of more than 10 Hz is needed, while the attenuation of noise requires a cutoff frequency below 50 Hz. $f_c = 15\,\text{Hz}$ was chosen - the bandwidth thus also is 15 Hz. Choosing R (R_7 and R_9 in the diagram) as 100 kΩ gives C (C_4 and C_5) as 106.1 nF, according to $f_c = \frac{1}{2\pi RC}$. The given cutoff frequency implies a rise time of 19.1 ms according to $t_r \approx \frac{1.8}{w_n} = \frac{1.8}{2\pi(15)}$ [7]. This meets the requirement of 100 ms, even when cascaded. After design completion, this filter is then duplicated and connected back-to-back in order to form cascaded second-order low-pass filters, as seen in figure 3.1. The simulated frequency response is shown in figure 3.2. While 10.5 Hz is somewhat lower than designed, it still falls within the range determined by the cutoff frequency and settling time requirements, as discussed previously. Assuming that each resistor is subjected to an average voltage of 2.5 V, while op-amps draws 3 mA [5], the calculated current consumption of the temperature sensor circuit is:
$I_{total} = (3)\frac{2.5}{10k} + (2)\frac{2.5}{230k} + (4)\frac{2.5}{100k} + (2)\frac{2.5}{500k} + (3)\frac{2.5}{5k} + (2)\frac{2.5}{230k} + (3)3mA = 11.38mA$
This leaves 88.62 mA for the rest of the health-monitoring system.

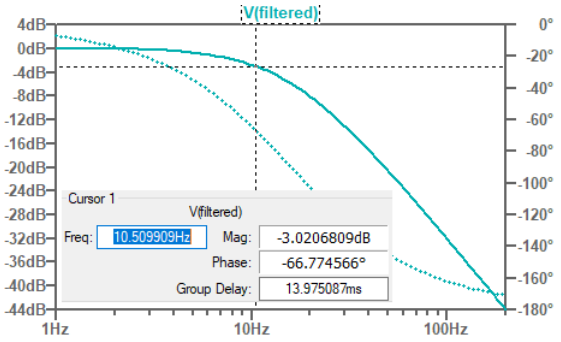
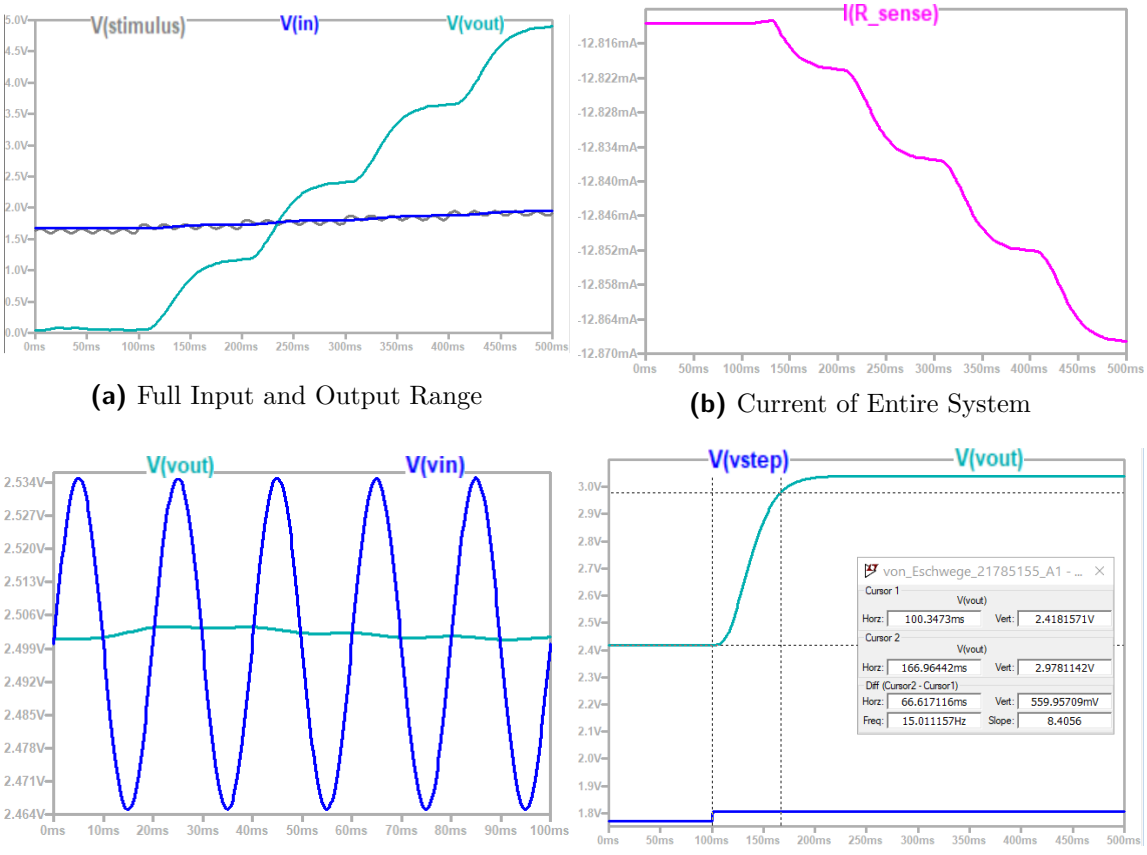


Figure 3.2: Simulated bode plot of filter

3.3. Results

The designed circuit receives an input signal ranging from 1.67 to 1.94 V for V_{in+}, which is somewhat higher than the calculated values of 1.63 to 1.91 V, and is due to the filter adding

some offset. This can easily be overcome by adjusting the voltage divider. V_{in-} receives 1.7 V. Both V_{in-} and V_{in+} thus fall well within the allowable range for the TLC2272, which is from $V_{DD-} - 0.3$ to V_{DD+} [5]. The circuit produces a signal centered at 2.5 V with an output swing of 4.86 V (figure 3.3a), exceeding the required 3.5 V. The absolute maximum amount of noise measured is 25.6 mV (figure 3.3c), and the settling time is 67 ms (figure 3.3d), thereby meeting the requirements of 50 mV and 100 ms respectively. Total current draw is 12.83 mA (figure 3.3b), well below the required 15 mA, and very close to the calculated 11.38 mA. The output signal (light blue) is shown in figure 3.3a.



(a) Full Input and Output Range

(b) Current of Entire System

(c) Simulated Noise Suppresion

(d) Simulated Output Rise Time

Figure 3.3: Complete Circuit Output (a) Output Range: 0.1 to 4.85V. Input Range: 1.63 to 1.94 V. (b) Current draw below requirement. (c) Noise suppressed to negligible levels. (d) Settling time within 100 ms.

3.4. Summary

Concluding, the circuit performs very well and successfully amplifies the temperature sensor output to a level that is readable by the microcontroller ADC, all the while attenuating almost all noise present in the input. The design is somewhat more complex, which however is justified by the requirements of Assignment 3. While being complex, it still is inexpensive, as it uses less of the TLC2272 op-amps. The design meets all base and bonus requirements requirements with a good margin to spare, all the while using only three op-amps, two of which are the cheaper TL081 models.

Chapter 4

Heart rate sensor

4.1. Introduction

Circuits pertaining to signal conditioning, pulse signal and analogue output generation will be discussed. Conditioning is done via filtering and amplification, thereafter thresholding and pulse-width modulation is used to generate outputs. Active filters provide high input and low output impedance, and a large Q-factor [8]. A differential amplifier is suitable for amplification, as the gain is referenced against a customizable voltage [3]. A Schmitt Trigger is well-suited for pulse generation, as it provides a noise margin [9]. PWM signals can be converted to analogue using filtering [10].

4.2. Design

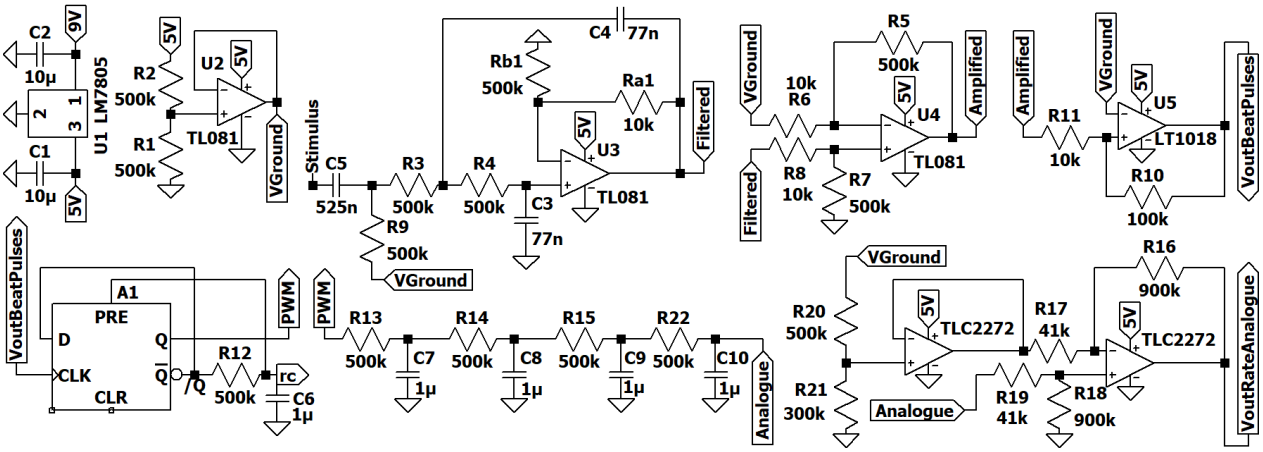


Figure 4.1: Complete Circuit

The complete circuit is shown upfront in figure 4.1 to aid explanation. The largest resistor in sub-circuits is always chosen to be 500 kΩ as to reduce current usage. The TLC2272 op-amp has V_{CM} of −0.3 to 4 V, $V_{ID} = \pm 16\ V$, $V_{in_{max}} = V_{DD+}$ and $V_{in_{min}} = V_{DD-} - 0.3$ [5]. The TL081 has V_{CM} of 1 to 4 V, $V_{ID} = \pm 30\ V$, $V_{in_{max}} = 3.5\ V$ and $V_{in_{min}} = 1.5\ V$ [11]. This information is given here as to avoid repetition - refer here when op-amp characteristics are discussed. The design process now follows. The FFT of the stimulus input in figure 4.2 shows information residing between 0.8 to 2.5 Hz, corresponding to 50 and 150 BPM respectively. The other peaks represent noise at 0.25 Hz, as well as at twice and three times the message signal, and higher. Noise distorts square wave output, necessitating filtering. A first order passive high-pass filter, $f_c = 0.606$ Hz, attenuates the

low-frequency noise at 0.25 Hz. R18 = 500 kΩ, thus C8 = 525 nF according to $f_c = \frac{1}{2\pi RC}$. A virtual ground centres the signal around 2.5 V, ensuring that the LPF input falls within the common-mode range of the TL081, which is used as it inexpensive [12]. A second order active low-pass filter, $f_c = 4.1$ Hz, filters out high frequency noise. R5 = R6 = 500 kΩ, C1 = C2 = 77 nF - see aforementioned formula. Cutoff frequencies were selected to remove noise maximally while minimally affecting heart-rate data. The signal should reside slightly above 2.5 V to facilitate amplification (to be discussed) and to ensure common-mode input range compliance in the next stage. Thus, Rb1 = 500 kΩ and Ra1 = 10 kΩ since $A_v = 1 + \frac{R_A}{R_B}$ [6]. A filter output with DC offset slightly above 2.5 V allows for the use of a differential amplifier with the existing virtual ground connected to the negative input, removing the need for additional circuitry otherwise required. The signal is amplified according to $V_{OUT} = \frac{R_a}{R_b}(V_2 - V_1)$ [3], where R_a corresponds to R7 and R9 and R_b to R8 and R10. The gain of 50 was selected to again provide a DC offset of 2.5 V, as it facilitates implementation of the comparator (to be discussed). Since the amplified signal has an amplitude of only 1.66 V, the inexpensive TL081 was chosen despite having a smaller output range. Next, the signal is fed into a Schmitt Trigger - the LT1018 comparator allows for output very close to 0 and 5V and has a high gain. 5 V is produced if the input exceeds the upper trip point (UTP) and 0 V if the input falls below the lower trip point (LTP) [9]. The hysteresis width (w_h = UTP - LTP) serves as a noise margin around the reference voltage, V_{REF} [9]. The DC offset of 2.5 V of the amplified signal requires $V_{REF} = 2.5$ V, once again allowing for the use of the existing virtual ground. Pulse duration is designed for the highest frequency, as it will then also meet the requirement for lower frequencies. Since 150 BPM corresponds to a period of 0.4 s, w_h is selected to ensure an output pulse width of at least 150 ms; 200 ms selected to account for noise. The amplified signal approximates a sinusoid:

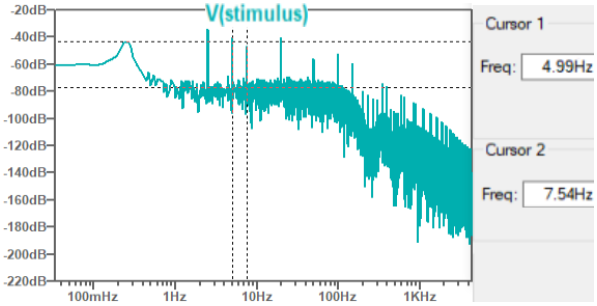


Figure 4.2: Fast fourier transform of stimulus

$$y_1 = 1.66\sin(2\pi(2.5)t_1) + 2.5 \qquad (4.1) \qquad y_2 = 1.66\sin(2\pi(2.5)t_2) + 2.5 \qquad (4.2)$$

Subtracting 4.2 from 4.1 yields $y_1 - y_2 = w_h = 0.52$ V for t_1 =0.01 s and $t_2 = 0.21$ s, resulting in a theoretical pulse width ranging from 0.2 to 0.625 ms, which is sufficient. w_h also is an order of magnitude larger than the highest input signal noise levels, increasing design fidelity. Now, UTP = 2.75 V, LTP = 2.25 V, UTP = $V_{REF} + \beta Vcc$ and LTP = $V_{REF} - \beta Vcc$, thus β = 0.05 [9]. Further, $\beta = \frac{R_{22}}{R_{22}+R_{21}}$. Thus R21 = 190 kΩ and R22 = 10 kΩ. (R21 was adjusted to 100 kΩ to account for loading effects). A one-shot was considered to extend the pulses, but was omitted as it was superfluous. The pulse output frequency thus represents the heart-rate.

Obtaining an output suitable for a microcontroller presents itself as a problem of converting frequency to analogue. The decision was made to obtain a PWM signal from the FM pulse signal, as PWM signals readily lend themselves to conversion-to-analogue using a simple

low-pass RC filter. Pulse-width modulation was achieved by means of a D flip-flop. The essence of the design is to continually keep the output high at first, but to then drive the output low for a fixed time, once per period. Since the period of the clock signal varies against BPM, driving low for a fixed amount of time results in a different ratio of the pulse being low at different frequencies, producing a varying duty cycle. Specifically, the previously generated pulse signal is used as a clock signal for the D flip-flop, and the not-Q output is fed back into the data line. This would normally drive the output high for all time t; thus a RC circuit is added of which the capacitor is charged by the not-Q output, and connected to the SET-line of the flip-flop. Once the capacitor charges to 2.5 V, Q is pulled high and not-Q low until the next rising edge of the clock input inverts Q and not-Q. The result is a slightly delayed PWM signal, with a large duty cycle at high frequencies, and vice-versa. The PWM output is consistent as long as the capacitor charge time is selected to be shorter than the narrowest pulse of the clock signal. See section 4.3, figure 4.7a for output. For the RC circuit, R1 = 500 kΩ gives $C = 1\mu$, according to the capacitor charge/discharge exponential equations - the extended solution (via Matlab scripting) is given in Appendix C for the sake of brevity. Having obtained a PWM signal, a fourth order passive low-pass filter produces analogue values in the range of 0.95 to 1.2 V. A cutoff frequency of 0.3 Hz ensures maximal attenuation of noise while maintaining a 5% settling time of 10 seconds. Therefore R = 500 kΩ and C = 1 μ. Finally, the analogue output is amplified by means of a TLC2272 differential amplifier with a negative input at 0.938 V. A gain of 20 produces a sufficient output range. Resistor values were increased as to minimize loading effects - thus R2 = R12 = 900 kΩ and R11 = R13 = 45 kΩ according to $V_{OUT} = \frac{R_a}{R_b}(V_2 - V_1)$ [3]. Loading effects still had a slight effect, and required adapting R11 and R13 to 41 kΩ. An analogue transducer is thus designed. **For microcontroller integration, a log-linear scale can linearise the analogue output, and the calibration constant is calculated. The slope is $\frac{0.8-2.5}{4.7-0.5} = -0.404$. Thus, for 150 BPM, $f = 2.5 = -0.404V + C = -0.404(0.5) + C \quad \rightarrow \quad C = 2.702$. ADC stuff here?????**

Total current is calculated using 1.4 mA per TL081 [11], 2.2 mA per TLC2272 [5] and 110 μA per LT1018 [13]. Non-trivial resistors are all approximated using 5 V over, as to err on the side of caution: $4(1.4m) + (2.2m) + (110n) + 16\left(\frac{5}{500k}\right) + 3\left(\frac{5}{10k}\right) + 2\left(\frac{5}{41k}\right) + \left(\frac{5}{100k}\right) = 9.75$ mA.

4.3. Results

The frequency response of the high- and low-pass filters gives $-3dB$ at 0.61 Hz and $-6dB$ at 4.3 Hz respectively - see figures 4.4a and 4.4b. This reflects design calculations near perfectly. Comparison of filter input and output in figure 4.3 shows a drastic noise reduction.

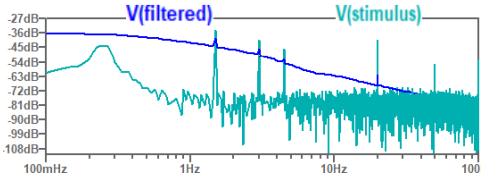
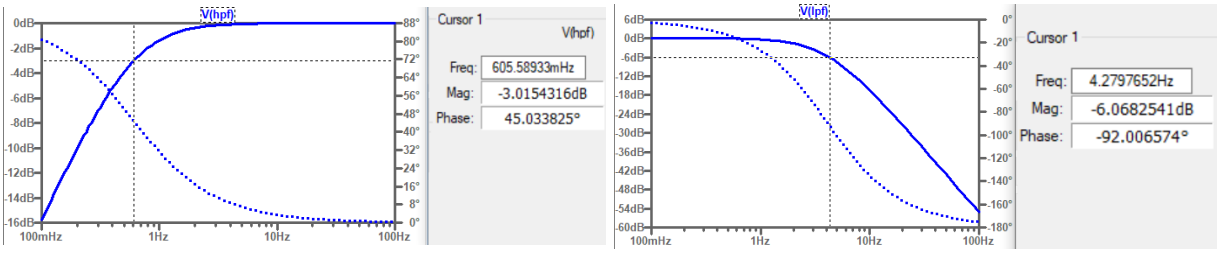


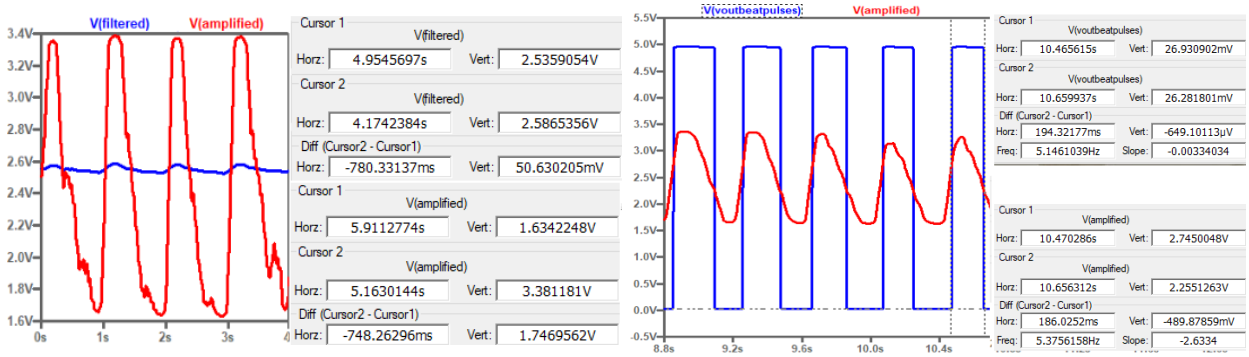
Figure 4.3: Filter input and output



(a) High-pass filter **(b)** Second-order low-pass filter

Figure 4.4: Frequency response of filters

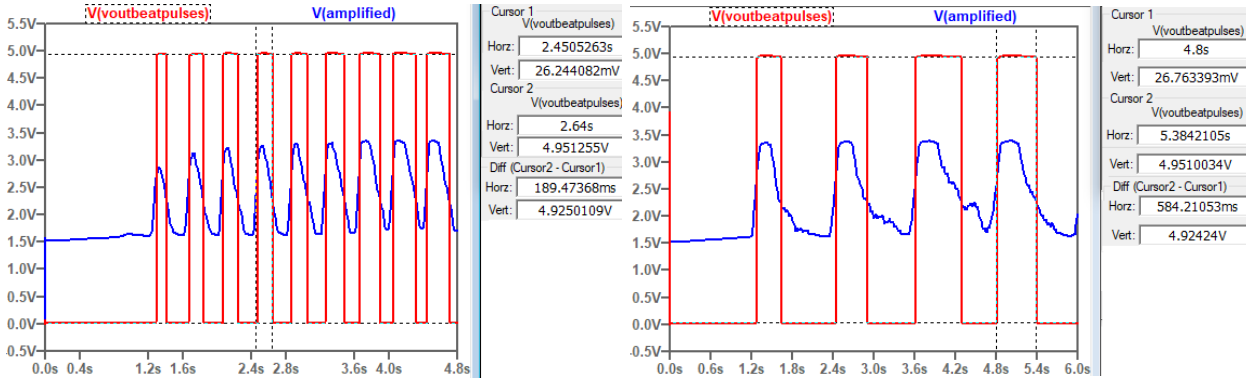
The filtered signal is passed through a differential amplifier; the input is shown in blue and the output in red in figure 4.5a. The filtered signal has a 50 mV amplitude (peak-to-peak), and the output 1.747 V. Therefore $A_v \approx 35$, which, although smaller than calculated, is to be expected due to non-linear behaviour for high amplification factors. Input and output of a LT1018 comparator, used for thresholding, is shown in figure 4.5b. See UTP = 2.75 V and LTP = 2.25V in figure 4.5b, giving a hysteresis width of 0.5 V, exactly as calculated.



(a) Amplification of filtered signal **(b)** Thresholding

Figure 4.5: Signal Conditioning

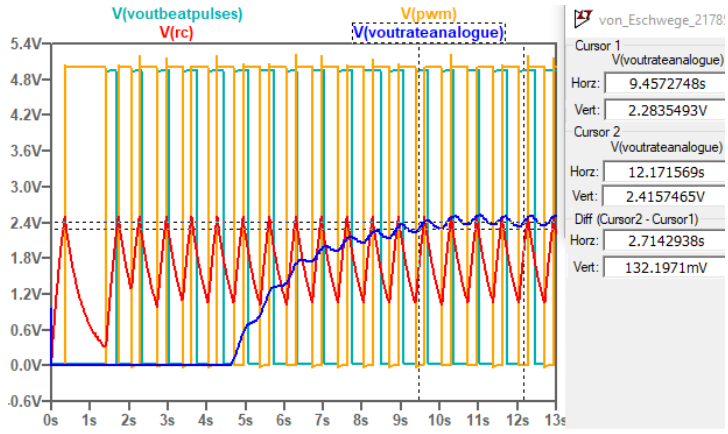
The output ranges from 0.026 to 4.95V, with a pulse duration in range 189 to 584 ms in figures 4.6a and 4.6b, meeting the 150 ms requirement. The design remains consistent for specification deviations of ±10% amplitude and a DC offset variation of ± 0.2 V, as the high-pass filter removes the DC component and the filter has a cutoff frequency low enough to greatly attenuate noise.



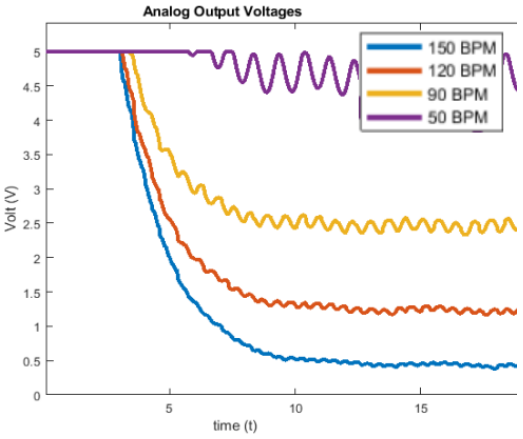
(a) 150 BPM **(b)** 50 BPM

Figure 4.6: Full input versus output range

For the analogue transducer, a PWM signal is obtained. Section 4.2 explains the interrelation, where `voutbeatpulses`, `pwm` and `rc` in figure 4.7a correspond to the clock signal, Q, and the charging capacitor voltage respectively. The 5% settling time is 9.45 s. The duty cycle is 73% at 60 BPM and decreases to 56% at 150 BPM. Finally, amplification and filtering of the PWM signal produces analogue output, range 4.2 V (4.7b).



(a) PWM and settling time



(b) Analogue voltage output

In figure 4.8, total current draw is measured through R_{sense}, averaging 13.0 mA, meeting the bonus requirement of 15 mA. When combined with Assignment 1, the combined current of 25.8 mA still is far less than the maximum current rating of 100 mA for the voltage regulator [**?**].

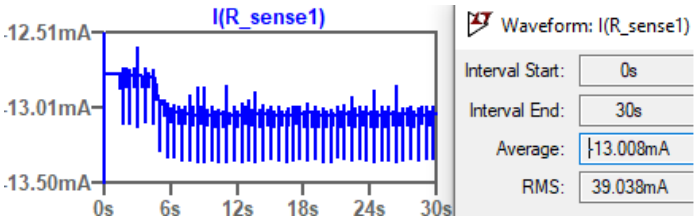


Figure 4.8: Total current usage

4.4. Summary

Concluding, it has been shown that the design performs as expected, meeting the all requirements. Output pulse width is broader than required, analogue output is generated with discrete, non-overlapping values exceeding the required range, while settling to a final value according to specification. Current draw remains sub-15 mA. Upon implementation of the microcontroller, be cognizant of the fact that analogue output values scale in a slightly non-linear fashion. This is not a problem, as it can be easily accounted for in software. By design, the system is limited to the 50 to 150 BPM range, but could be expanded using the existing design as a proof-of-concept.

Chapter 5

Calibration and digitisation

5.1. Temperature sensor

Include flow diagram of code or pseudocode as a list.

5.1.1. Analytical Design

Analytical expectations (calculations of what you expected the calibration to be) Please include a 10-bit make-believe ADC in your calculations

5.1.2. Empirical Design

Based on measurements, calculate calibration (to adapt or replace analytic design. Compare analytic solution to empirical solution (plot?)
Include assessment of your calibration.

5.2. Heart rate sensor

No need to include the 10-bit ADC in this section.

Chapter 6

System and conclusion

6.1. System

Considering the system as a whole, it should be easy to integrate it with the rest of the health monitoring system as the design is modular. This can be done by feeding the output of the temperature sensor into the system designed in this report, and then connecting the output of the system to the microcontroller ADC. This requires relatively few connections, and the only setup needed is to calibrate the ADC, using the following formula [7]:

$$\text{ADC} = (2^{10} - 1)\frac{V_{in}}{V_{ref}} \quad \rightarrow \quad V_{in} = \frac{\text{ADC}(V_{ref})}{2^{10} - 1}$$

The slope of the temperature increase is $\frac{42-34}{5-0} = 1.6$. Thus, for 38°C:

$$T = 38 = 1.6V + C = 1.6(2.5) + C \quad \rightarrow \quad C = 34$$

Therefore, the temperature can finally be calculated by

$$T = (1.6)\frac{\text{ADC}(V_{ref})}{2^{10} - 1} + 34$$

Since the noise is 25 mV at maximum, the quantisation error (due to noise) is $T_{err} = (1.6(0.025) + 34) - (1.6(0) + 34) = 0.04$°C. Therefore, the measurement error is less than 4% per 1°C.

Concluding, it has been shown that the combination of the voltage regulator and the temperature sensing circuitry works very well to achieve the desired result. Since the cascaded filters ensure extremely low noise levels, the ADC should be capable of distinguishing the measured temperature to a very high degree of accuracy. The system uses more of the less costly components, and is very power efficient, all the while meeting all of the bonus requirements. It is thus safe to say that the objective of the design has been met successfully.

6.2. System

The design of the heart-rate sensor goes to show that a noisy input signal could effectively be converted to a square wave output as well as an analogue output, enabling reliable interfacing of real-world measurements with digital systems. The heart-rate sensing circuit can now be

integrated with the remainder of the health monitoring system by connecting the analogue output to the microcontroller input, to which the temperature sensor will also be connected - see E344 Assignment 1 [**?**]. The modular design of different parts of the health-monitoring system simplifies both design and debugging. Due to the second order low-pass filter, the heart-rate sensor is remarkably robust with respect to variations in noise, attenuating noise levels to below 6% of the signal amplitude before creating a pulse output. The design also performs well on a variety of the normalised input data sets. Calibration for microcontroller integration is done according to $f = -0.404V + 2.702$ (section 4.2, and the quantisation error is $f_{err} = \frac{2.5-0.8}{2^{10}}/(2.5-0.8) \times 100 = 0.1\%$. Noise is filtered to the extent that it has a negligible effect on the digitalized reading. The system utilizes less costly components where possible, is very power efficient, and adheres to all of the bonus requirements. The design objective has been met successfully.

6.3. Lessons learnt

1. LTSpice is a blessing, but can be an absolute nightmare with simulations. I've created a rough metric; it goes to show that 30% of my time was spent on circuit design, 10% on report writing, and 60% on debugging LTSpice simulation problems. I entered E-Design with the belief that simulation would greatly accelerate the pace of the subject, as soldering was eliminated, but I stand firm in my belief that I could have built a practical circuit much faster, as 'timestep too small' does not apply in the beauty of real-world continuity. However, maybe I just stand firm in this belief because I have not dealt with the problems arising from burnt-out components, messy soldering, melted PCB tracks and exploding diodes.
2. I believe to have greatly improved with regards to modularising and debugging not only circuits, but systems in general. Treating everything as a small problem to be solved furthered my conceptual understanding of component interaction.
3. I shouldn't have gone surfing for the entirety of the first week of the term. I said this in Assignment 1 as well, and lost marks for it, but it is still applicable, so I'll say it again.
4. If I could have it all over again, I wouldn't have texted my circuit; she did not reply.

Bibliography

[1] *LM78LXXA 3-Terminal 0.1 A Positive Voltage Regulator*, LM7805 Datasheet, Fairchild Semiconductor Corporation, 2013.

[2] *LM2595 SIMPLE SWITCHER® Power Converter 150-kHz 1-A Step-Down Voltage Regulator*, LM2595 Datasheet, Texas Instruments, May 2016.

[3] W. Storr, "Operational amplifiers," 2018. [Online]. Available: https://www.electronics-tutorials.ws/opamp

[4] M. J. Booysen, "E344 - lecture 2," 2020. [Online]. Available: https://www.youtube.com/watch?v=5bzHyeFQCPo&feature=youtu.be

[5] *TLC227x: Advanced LinCMOS Rail-to-Rail Operational Amplifiers*, TL2272 Datasheet, Texas Instruments, 2016.

[6] W. Storr, "Filters," 2018. [Online]. Available: https://www.electronics-tutorials.ws/filter

[7] H. Jordaan, "Control systems - 314," 2020. [Online]. Available: https://learn.sun.ac.za/course/view.php?id=53481

[8] "Difference between active and passive filter." [Online]. Available: https://circuitglobe.com/difference-between-active-and-passive-filter.html#ComparisonChart

[9] W. Storr, "Op-amp comparator," 2018. [Online]. Available: https://www.electronics-tutorials.ws/opamp/op-amp-comparator.html

[10] "Analog output - convert pwm to voltage." [Online]. Available: https://www.instructables.com/id/Analog-Output-Convert-PWM-to-Voltage/

[11] *TL08xx: JFET-Input Operational Amplifiers*, TL081 Datasheet, Texas Instruments, May 2015.

[12] "Octopart," Octopart, 2020. [Online]. Available: https://octopart.com/

[13] *LT1018 Micropower Dual Comparator*, LT1018 Datasheet, Linear Technology.

Appendix A

Social contract

UNIVERSITEIT•STELLENBOSCH•UNIVERSITY
jou kennisvennoot • your knowledge partner

E-design 344 Social Contract

2020

The purpose of this document is to establish commitment between the student and the organisers of E344. Beyond the commitment made here, it is not binding.

In the months preceeding the term, the lecturer (Thinus Booysen) and the Teaching Assistant (Michael Ritchie) spent countless hours to prepare for E344 to ensure that you get your money's worth and that you are enabled to learn from the module and demonstrate and be assessed on your skills. We commit to prepare for the module, to set the tests and assessments fairly, to be reasonably available, and to provide feedback and support as best and fast we can. We will work hard to give you the best opportunity to learn from and pass analogue electronic design E344.

Signature: ..... Date: 13 July 2020

.....

I, Daniel Heinrich von Eschwege have registered for E344 of my own volition with the intention to learn of and be assessed on the principals of analogue electronic design. Despite the potential publication of supplementary videos on specific topics, I acknowledge that I am expected to attend the lectures and lab sessions to make the most of these appointments and learning opportunities. Moreover, I realise I am expected to spend the additional requisite number of hours on E344 as specified in the yearbook.

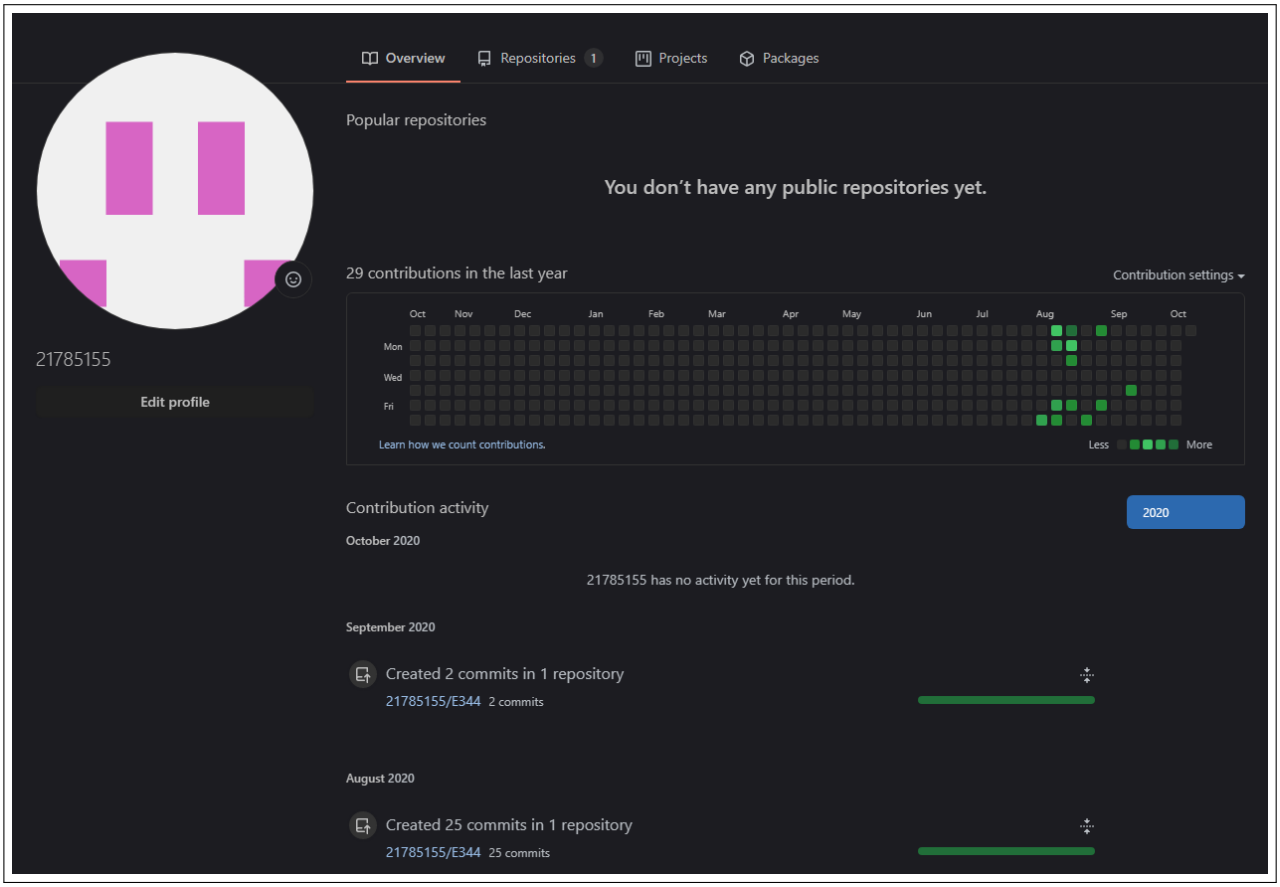
I acknowledge that E344 is an important part of my journey to becoming a professional engineer, and that my conduct should be reflective thereof. This includes doing and submitting my own work, working hard, starting on time, and assimilating as much information as possible. It also includes showing respect towards the University's equipment, staff, and their time.

Signature: ..... Date: 24/09/2020

1

Appendix B

GitHub Activity Heatmap



Appendix C

Stuff you want to include

R1 = 500 kΩ. $\tau = RC$. The capacitor charge oscillates between V_L and V_H. $V_H = 2.5\,\text{V}$. V_L is reached for the first time at t_{L_1} and V_H at t_{H_1}. V_L is then reached at t_{L_2}. For 150 BPM (or 2.5 Hz), the pulse drives high for 0.2 ms. Since the capacitor has to charge faster than 0.2 ms, a charge time of 0.16 ms was selected to add a 20% margin, accounting for noise. Thus $t_{H_1} - t_{L_1} = 0.16$ and $t_{L_2} - t_{H_1} = 0.4 - 0.16 = 0.24$ for the 150 BPM signal. Finally,

$$V_L = 5\left(1 - e^{\frac{t_{L_1}}{\tau}}\right)$$

$$V_H = 5\left(1 - e^{\frac{-t_{H_1}}{\tau}}\right)$$

$$V_L = V_H\left(e^{\frac{t_{L_1}}{\tau}}\right)$$

giving $C = 1\mu$, when solving using the following MatLab script:

```
syms t
syms tl1
syms th1
syms tl2
syms Vl
Vh = 2.5
R = 500000
A = Vl==5*(1-exp(-tl1/t))
B = Vh==5*(1-exp(-th1/t))
C = Vl==Vh*(exp(-(tl2-tl1)/t))
D = th1 - tl1 == 0.16
E = tl2 - th1 == 0.24
S = solve([A, B, C, D, E],[t, tl1, th1, tl2, Vl])
S.t
S.tl1
S.th1
S.tl2
Vl
C = R/t
```

Appendix D

Stuff you want to include

It is a good design practice to include a unity gain op-amp to acts as a voltage buffer by clamping V_{in-} against fluctuations. This design practice was considered, but ultimately rejected, as tests with and without the buffer provided outputs of equal quality. This is the case as the signal conditioning circuit already has a very high input resistance. The only notable differences resulting from the inclusion of a buffer were an increase in current drawn, as well as an increase in cost for the circuit components, as another op-amp is required. Therefore, in order to keep the current consumption below 15 mA, as well as to use reduce cost by only using three op-amps, the voltage buffer was omitted in the final design.