Microprocessors Module 1 Questions

Part A

1. List Features of 8085 Microprocessor

- 8-bit general purpose microprocessor(μp)
- Capable of addressing 64 kb of memory
- Has 40 pins
- Requires +5 v power supply

2. Value of Code Segment(CS) Register is 3054H and value of different registers is as follows BX: 4025H, IP: 1580H, 5467H, Calculate the physical address of next instruction to be fetched

- The offset of the CS Register is the IP register.
- Therefore, the effective address of the memory location pointed by the CS register is
  - Effective address= Base address of CS register X 10H + Address of IP

$$
\begin{aligned}
&= 3054_H \text{ X } 10_H + 1580_H \\
&= (30540 + 1580)_H \\
&= 31AC0_H
\end{aligned}
$$

3. What is pipelined architecture? How is it implemented in 8086?

- To speed up the execution of program, the instruction fetching and execution of instructions are overlapped with each other.
- This process of fetching the next instruction when the present instruction is being executed is called as pipelining
- In pipelining, when the nth instruction is executed, the (n+1) th instruction is fetched and thus the processing speed is increased
- Pipelining has become possible due to the use of queue.
- BIU (Bus Interfacing Unit) fills in the queue until the entire queue is full.
- When EU is busy in decoding and executing an instruction, the BIU fetches up to six instruction bytes for the next instructions

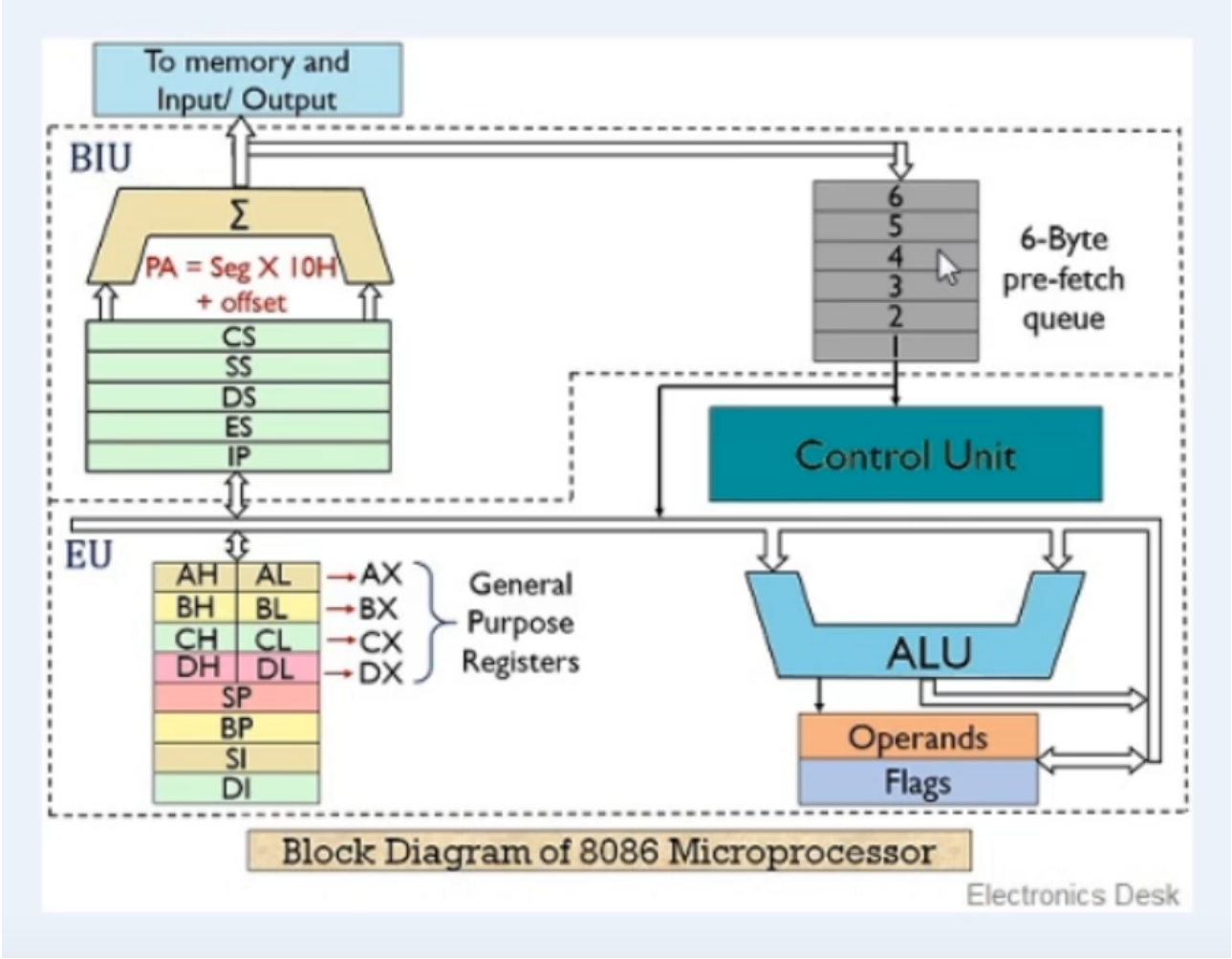
- BIU restarts filling in the queue when at least two locations of queue are vacant

4. Compare the architectural and signal difference between 8086 and 8088

S. NO.	8086 MICROPROCESSOR	8088 MICROPROCESSOR
1	The data bus is of 16 bits.	The data bus is of 8 bits.
2	It has 3 available clock speeds (5 MHz, 8 MHz (8086-2) and 10 MHz (8086-1)).	It has 3 available clock speeds (5 MHz, 8 MHz)
3	The memory capacity is 512 kB.	The memory capacity is implemented as a single 1MX 8 memory banks.
4	It has memory control pin (M/IO) signal.	It has complemented memory control pin (IO/M) signal of 8086.
5	It has Bank High Enable (BHE) signal.	It has Status Signal (SSO).
6	It can read or write either 8-bit or 16-bit word at the same time.	It can read only 8-bit word at the same time.
7	Input/Output voltage level is measured at 2.5 mA.	Input/Output voltage level is measured at 2.0 mA
8	It has 6 byte instruction queue.	It has 4 byte instruction queue as it can fetch only 1 byte at a time.
9	It draws a maximum supply current of 360 mA.	It draws a maximum supply current of 340 mA.

Part B

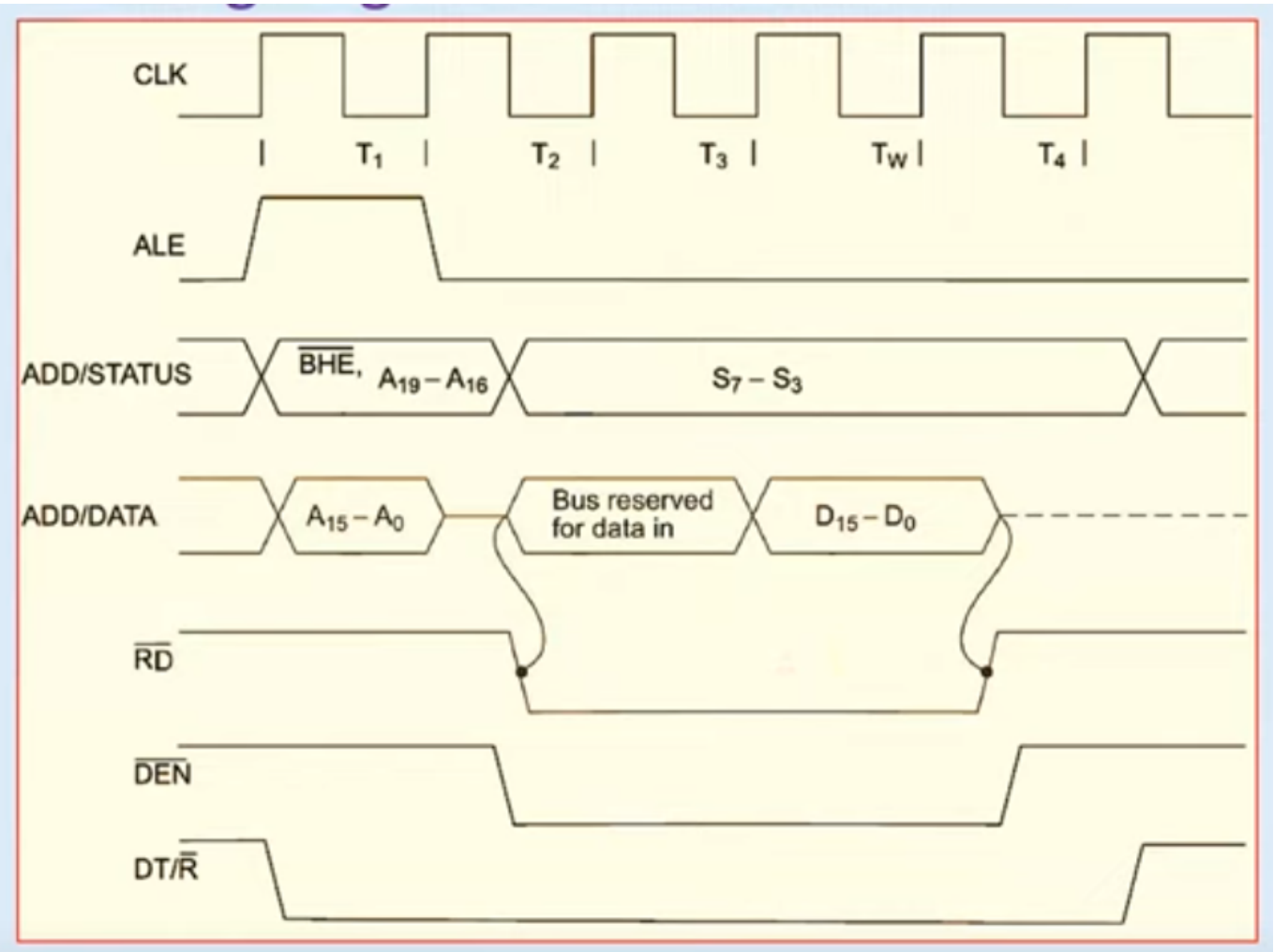
1. Draw and explain internal architecture of 8086



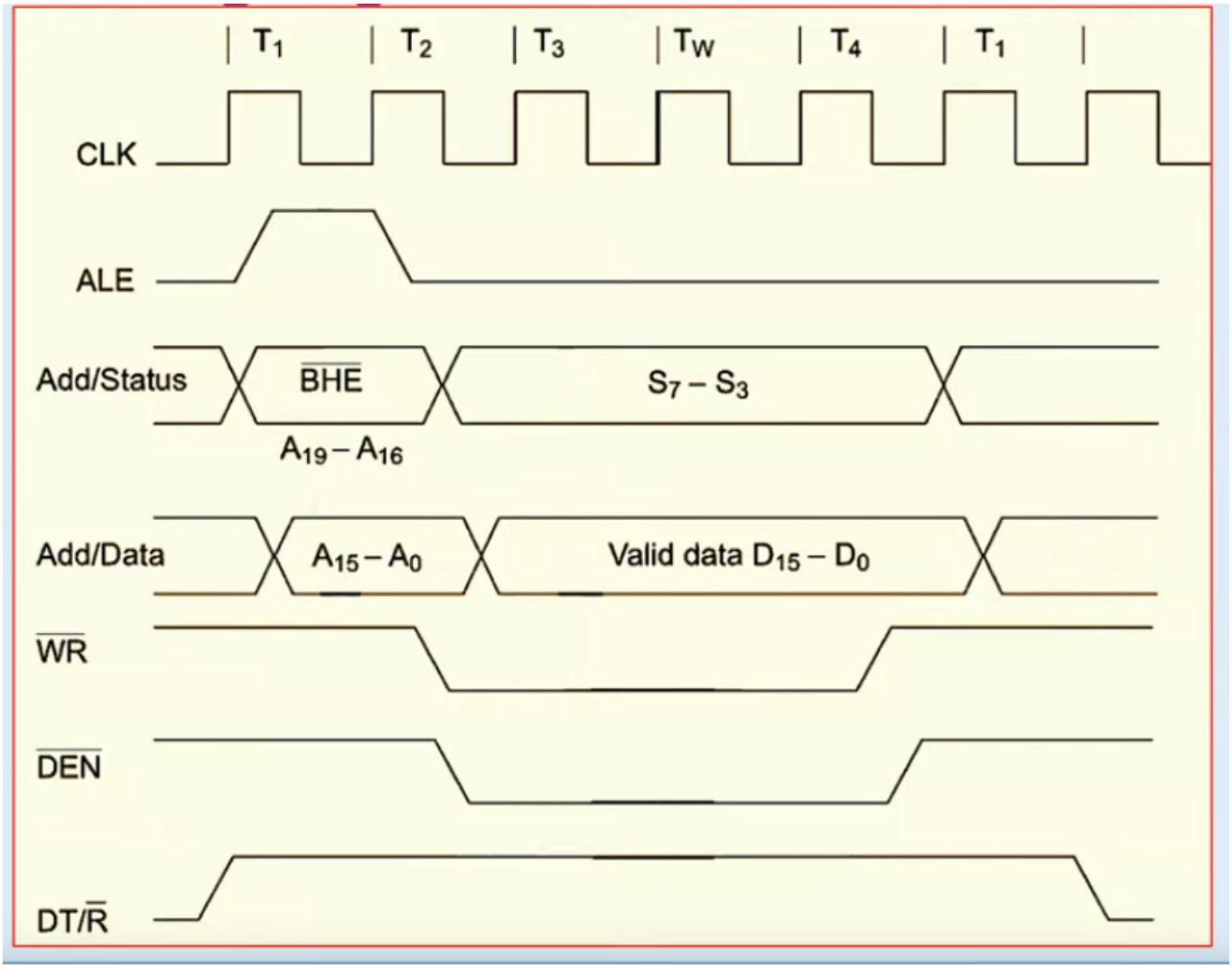
- General purpose registers
- Segment registers
- flag register
- Execution unit
- Bus interface unit
- instruction queue
- address bus
- data bus
- control bus

2. Draw the memory read and write diagrams of 8086 in minimum mode

Read Diagram



Write Diagram



3. Draw the structure of 8086 flag register and mention purpose of each flag

Flag Register

- A flag is a flip-flop used to store the information about the status of the processor and the status of the instruction executed most recently. 8086 has 9 flags.

Acronym (ODIT SZ CAP)

- Overflow Flag
  - Set if overflow occurs
- Direction Flag
  - Flag= 0
    - String processed lowest -> highest
  - Flag = 1
    - String processed highest -> lowest

- Interrupt flag
- - Flag = 1 when maskable interrupt is recognised by CPU
- Trap Flag
  - Flag = 1 when trap interrupt is generated after execution of each instruction
- Sign Flag
  - Flag = 1 when result of computation is negative
- Zero Flag
  - Flag = 1 when result of computation is 0
- Ac Auxiliary carry flag
  - Flag = 1 if there's a carry from the lowest nibble
- P - Parity Flag
  - Flag = 1 when result has even parity
  - Flag = 0, when odd parity
- Cy - Carry Flag
  - Set when there's a carry from addition or borrow from subtraction

Bits	**D_{15}**	**D_{14}**	**D_{13}**	**D_{12}**	**D_{11}**	**D_{10}**	**D_9**	**D_8**	**D_7**	**D_6**	**D_5**	**D_4**	**D_3**	**D_2**	**D_1**	**D_0**
Flags					O	D	I	T	S	Z		AC		P		CY