

**Queen's University Belfast**

**School of Electronics, Electrical Engineering and  
Computer Science**

**ELE8095 Individual Research Project**

**Project Title: *Implementation and Analysis of  
Applications for CHERI Enabled SIMT based SOC***

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**22nd September 2023**

## **Abstract**

This project investigates the implementation and analysis of programmes designed for a System-on-Chip (SoC) architecture enabled by Capability Hardware Enhanced RISC Instructions (CHERI) and the Single Instruction, Multiple Threads (SIMT) execution paradigm. CHERI, known for its security innovations, offers to the SoC area a unique mix of hardware-based capabilities and fine-grained memory protection, providing greater security and adaptability. Through actual application development and in-depth research, the major goal of this study is to evaluate the capabilities and possibilities of CHERI-enabled SIMT-based SoCs. This project will help in the solving of many crucial issues by developing and optimising apps for this unique architecture, crucial issues like the performance and security of applications with data parallel workload. The discoveries and contributions of this research are intended to increase the understanding of CHERI-enabled SIMT-based SoCs, with implications for both academia and industry. Furthermore, this research aims to give practical assistance for developers and engineers working with future hardware security technologies and parallel computing architectures, therefore encouraging innovation in the ever-changing computing system landscape.


## **Acknowledgements**

This project would never have been possible without the excellent guidance, assistance and patience of my supervisor, Dr. Arnab Kumar Biswas. I also thank the Queen's University Belfast for being able to provide me with a lab space, a laptop and all the necessary materials that I needed for this project. Finally, I would like to thank those who supported me in any way especially those who were able to support me emotionally.

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# 1.INTRODUCTION

SIMTight is a synthesisable General Purpose Graphics Processing Unit (GPGPU) that utilises the Single Instruction Multiple Threads (SIMT) model. SIMT hardware, such as Graphics Processing Units (GPUs), has been adopted widely in numerous domains, including graphics, machine learning and High-Performance Computing [1]. Along with the advent of CUDA, the SIMT programming approach was introduced and popularised for GPUs [2]. SIMT are similar to GPGPUs and has its advantages over a CPU due to its multithreading and control flow to avoid deadlock, the CPU also has its advantages over SIMT like its precise prediction for branch and its lower latency. SIMT hardware has built-in effective performance because it amortises the front end of a pipeline overhead by acquiring and deciphering each of the instructions just one time for every one of the threads in the same warp and a warp is a group of threads, and it generates a smaller amount of traffic to the system's memory by combining accesses from threads in the same warp [1]. SIMT may lead to a deadlock without a control flow graph and a thread block compaction is one of the methods for an efficient SIMT flow [3]. Applications that reap the advantages from GPU execution often have a high level of data parallelism along with frequent memory access behaviours that enable optimal utilisation of off-chip memory bandwidth [4]. There is a problem of the security of a system in hardware that the Capability Enhanced Risc Instructions (CHERI) will cover because of not enough emphasis is placed on the hardware's security. CHERI can be seen as a software or hardware collaborative project. Setting up a simulator for SIMTight is one of the goals for the project and another one of the goals of the project will be to enable CHERI on the simulator, a more detailed explanation of the various goals and the results will be discussed extensively across all the sections but the main goal for this project is to use the enabled CHERI SIMTight simulator to successfully test the effectiveness and performance of the CHERI enabled Simulator with different algorithms and codes so that it can be confirmed that the simulator can work for different algorithms or codes and not just the original sample codes while utilizing the library of NoCL to achieve the desired result. The SIMTight project also talks about the scalar synchronization of SIMT but this will not be a point of focus in this dissertation. In this dissertation, applications are also referred to as sample codes or original sample codes and modified applications are referred to as modified codes. There will be a total of six sections in this dissertation, the first section is the introduction section, the second section is the literature review section,

the third section is the test methodology section, the fourth section is the experiment result and analysis section where the results from the code implementation will be discussed along with future plans on the direction to take, the fifth section is the conclusion section, the sixth and final section is the references section.

## **1.1 Problem Statement**

The project is about the Implementation and Analysis of Applications for CHERI Enabled SIMT based SOC (System on Chip). Various problems will be encountered along the process of reaching the project's objectives. The first challenge that will be encountered is the setting up of the simulator because although there are instructions that can be followed, there are errors that can be encountered due to version issues or library issues. The second challenge that will be stumbled upon, is the enabling of CHERI and scalarization to provide a way for compartmentalization for blocks and threads in a block which exist in the memory. The second challenge also has the same problem as the first challenge whereby errors can occur due to dependency problem for the cheribuild that will be installed. The third and final problem which is the modification of application codes that utilize NoCL library, the challenges that will be the trial and error of various algorithms and data structures to find one which can enhance the performance of the applications when they are run on the CHERI enabled simulator.

## **1.2 Motivation**

Since the inception of SIMT based SOC, there have been several research that have contributed to its advancement, but the pace of its improvement is a bit slow because there are not a lot of articles that can be found when it comes to SIMT based SOC especially CHERI enabled SIMT based SOC. CHERI provides security enhancements which helps in the development of computing systems that are secure. Cyberthreats continue to plague the cybersecurity industry, so CHERI contributes to the reduction of successful cyberthreat attacks in computing systems. A CHERI enabled SIMT based SOC is a cutting-edge technology and the architectural structure of SIMT is suitable for certain sorts of applications which are good with data parallel workload. There are several applications which exist for a CHERI enabled SIMT based SOC which utilize a library called NoCL. NoCL is a library that is designed for the suitability for a CHERI enabled SOC, the goal of the project is the modification of a couple of these applications. Table 1



below displays the codes that will be modified in this project so as to improve their performance which enhances the security to protect data that are sensitive.

Application Name	Description
Reduce	Performs the summation of vectors.
Histogram	Computes 256-bin histogram.
VecAdd	Performs the addition of vectors.
MatMul	Performs the multiplication of a matrix.
Scan	Computes a parallel prefix sum (inclusive scan).
BitonicSortLarge	Performs the sorting of arrays while using Bitonic Sort algorithm.

**Table 1. Application names and their description.**

## 2. LITERATURE REVIEW

SIMTight is a project that uses the SIMT model of execution, it also utilizes CHERI for the security of the hardware, so a survey based on SIMT, CHERI, and GPU implementation of the three cryptographic algorithms was conducted. There were a couple of helpful articles about SIMT and CHERI which led to the discovery of a couple of projects that were also based off SIMT execution model. A. Alawneh et al. [1], discussed about the two major side effects that were noticed from a GPU SIMT hardware, the two side effects are the control flow for threads that exist in a block and the divergence of memory in the SIMT hardware because they are important when it comes to SIMT and the acceleration of the GPU so the authors proposed a tool which was called SIMTec, the proposed tool is used for the calculation of the control-flow and the divergence of memory which are the two side effects that affect an SIMT hardware. To compute the predicted SIMT efficiency, the tool is used to generate and analyse the dynamic control flow graph of the application, which the threads in a block are then grouped into warps (32 threads = 1 warp), and the functionality of a SIMT stack for each and every warp are replicated. Memory coalescing is computed using the locations accessible by memory instructions from parallel threads and the execution mask of each warp, memory coalescing is the merging or combining of requests to the memory into one so as to increase the performance of the memory. The SIMTec tool gives information on the efficiency of SIMT and the divergence of memory in order to provide more information for the programmer about the issues that exist in SIMT, especially the responsiveness of SIMT when it comes to CPU applications that are multithreaded. The authors in [2], recognized that there existed constraints when it came to the adaptation of algorithms where synchronization is employed for the hardware implementation of SIMT so they made 3 propositions, their first proposition was that by analysing the application control flow graph (CFG), they presented a static analysis approach for which could be used for the detection of deadlocks in SIMT. Their second proposition was that, wherever synchronisation is local to a function, where it becomes probable that a Control Flow Graph's transformation could be used for the elimination of SIMT deadlocks. The transformation and analysis methods of the Control Flow Graph are both carried out by the compiler passes of an LLVM. Their last and final proposition was that they offered an adaptive hardware reconvergence approach that allows the synchronisation of Multiple Instruction Multiple Data without the modification of the application's Control Flow Graph but can also benefit from the analysis

of their compiler. W. W. Fung and T. M. Aamodt [3], were more engrossed in the compaction of the thread block (Compaction can be seen as when the fragmented memory that is available is collected into a large memory so that other processes can be carried out) which helped for effective control flow for SIMT because they noticed that warps run without any issues until a divergent branch where the synchronization of warps is encountered, which causes a slow performance in multi-threaded systems, so they proposed the evaluation of the potential advantages of the expansion of the sharing of resources in a block of warps which could help to speedup or improve its performance because a lot of divergent branches lead to complications and inefficiency in the sharing of resources, and the proposed evaluation is also currently utilised for scratchpad memory, to leverage control flow locality across threads. Warps inside a thread block share a shared block-wide stack for divergence management. Threads are condensed into new warps in hardware at a diverging branch, their propositions were able to achieve a good result because they were able to achieve a significant performance to the speed of the per-warp reconvergence stack baseline. A. Ramamurthy [5], suggested that applications that are designed through the use of Gpu synchronisation have a problem that exists, and the problem was between the scalar programming approach and vector technology. How the stack of a hardware is used to handle the divergence of the control flow that exists among scalar threads was the cause of the problem. In order to solve the issue, the author made a proposition of an instruction set and hardware improvements to make mutual exclusion easier to implement when porting multiple-instruction, multiple data (MIMD) programmes with synchronisation to accelerators that use the SIMT hardware. In comparison to a more complicated software-only methods, the instructions provided comparable results, the queue based mutual exclusion on SIMT were also executed and assessed, but the set of instructions seemed to work in common cases but not all. W. Zhu and J. Curry [6], discussed that GPUs are used for scientific calculations that happen on a large scale due to its ability to break down tasks and run them in parallel, so they attempted to test the limits of the ACO Pattern Search Algorithm and how efficient it was, on a set of constrained functions that are bound. GPU are the typical graphics which are present in the hardware of personal computers that exist currently, it can also be used for the computing of parallel data that are on a computer's desktop. The traditional Ant Colony Optimisation (ACO) is converted in this proposition for the data-parallel GPU computing platform with SIMT and the research can be considered as a success because there was significant reduction to the time that was needed to perform a global

and local search. According to X. Gong et al. [7], the SIMT architecture used by existing GPU computation frameworks could not properly leverage the tolerance with memory resources because of the divergence of branch that exists in the memory. GPU applications, with the assumption of a SIMT execution architecture, usually tends to issue surges of requests to the memory which battles for GPU memory resources and such requests are managed by hardware units such as the wavefront scheduler but when the number of computing activities is very low to mask the lengthy latency of accesses into the memory, then the scheduler is affected. So, they came up with the solution of utilizing a Twin Kernel Multiple Thread (TKMT) execution paradigm which is a central compiler method that enhances the scheduling of hardware throughout the compilation process. By means of static instruction scheduling, TKMT spreads the surges of memory demands in a couple of wavefronts and there was about a 12% of average performance improvement compared to the model of SIMT when it came to hardware scheduling. A. Habermaier and A. Knapp [8] were concentrated on how correct the SIMT model was due to the various execution models that were being released continuously so the SIMT execution model was normalised in an operational semantics for a stack-based reconvergence mechanism and demonstrate its validity by building a simulation that bridges the SIMT semantics and a typical interspersed multi-thread semantics. The authors also displayed that the SIMT execution paradigm produces inequitable schedules in various situations, the objective of numerous papers on SIMT is usually to improve the performance and the efficiency of the SIMT execution model, but they don't focus on the unfairness of the SIMT execution model. M. Steffen and J. Zambreno [9], worked on increasing the SIMT effective performance of global rendering algorithms through the utilization of architectural assistance for dynamic micro-kernels and they were able to accomplish that by providing a SIMT architecture that allows threads to be formed dynamically during runtime to increase the utilisation of the CPU for rendering algorithms that are global, they replaced branching statements which led to the efficiency of the processor to be poor with new threads, but the idea was a good one but the final results that were achieved were not good because the time taken for a new thread to be spawn also reduces the efficiency and the performance of the processor. K. Wang and C. Lin [10], presented an approach for decoupling affine computations from the main execution stream which is a group of expressions which gives rise to systematic values that are extreme across SIMT threads, because the affine computations could be carried out with independence and a vast productivity from the main execution stream. This approach of

decoupling has two pros: (1) the dynamic warp instruction count is decreased considerably for compute-bound programmes; (2) the memory latency is lowered considerably when it comes to memory workloads that are bound by acting as a prefetcher which is non speculative for the data specified by the many affine calculations for memory address. J. C. Huthmann [11], proposed a new execution mechanism which allows various threads to run concurrently in a single accelerator because of the slow growth of the performance for typical processors. Furthermore, the paradigm allows for dynamic thread reordering at key places in the shared accelerator pipeline. This particular feature allowed for the threads which are not in the waiting line to be overrun by a thread that is waiting to access the memory because they have a higher priority, and it improves the performance of the processor by closing the gap to the interruption of memory accesses. To close the gap in the delay of accesses into the memory, these other threads can conduct their computations unaccompanied by the thread that is waiting. The new execution model resulted to a better resource usage by utilising resources more effectively. In addition, the concurrent execution of several threads can provide the same performance as numerous copies of an accelerator that has a single thread. The objective of this model was to achieve temporal switching, simultaneous execution and resource sharing so as to hide the latency in memory, improve performance and the improvement of efficiency respectively which were later accomplished. The authors Z. Lin et al. [12], discussed that context switching is a critical method which is used to enable CPU preemption and the multiplexing of time. Yet, because of the number of threads which are a lot in SIMT processors, it is difficult to handle context switching which in turn results in many architectural states to be exchanged during context switching. They proposed three distinct approaches to reducing and compressing architectural characteristics to accomplish lightweight context switching on SIMT processors which are selective pre-emption, context format and pre-emption pipeline. The authors B. Tine et al. [13], explained that the significance of hardware and software which are open-sourced are growing. Even though GPUs are among the most often used accelerators there is relatively little open-source GPU infrastructure which is available in a domain which is public which was also confirmed during the process of sourcing materials related to FPGA, Hardware, CHERI and the implementation of GPU, there was contention about the complexity of GPU ISAs and software stacks being one of the probable causes for the absence of open-source infrastructure, so they made a proposition of a RISC-V Instruction Set Architecture (ISA) modification that enables GPGPUs and graphics. The

primary purpose for the proposal of the ISA extension is to minimise ISA modifications in order to minimise equivalent changes to the open-source ecosystem, resulting in a sustainable development ecology. They developed the whole Vortex software and hardware stacks on FPGA to illustrate the practicality of the RISC-V ISA. To address some issues of the memory bandwidth wall, the authors X. Xie et al. [14] proposed the Memory-centric Processing Unit (MPU), the first-generation SIMT processor which was based on a 3D-stacking near-bank computing architecture was used to overcome these difficulties. To realise varied data pathways with low overheads, MPU employs a hybrid pipeline capable of loading commands to near-bank compute-logic. A pair of architectural aids was also investigated for the SIMT programming model, a near-bank shared memory architecture and an improvement with considerable number of active buffers in row. Finally, a complete compilation flow for MPU was given to enable CUDA programmes which are products of Nvidia. A backend optimisation was also created for the decision to offload instruction so that the MPU's hybrid pipeline can be properly utilized. F. Elsabbagh et al. [15], presented a Vortex, a RISC-V General-Purpose GPU that's compatible with OpenCL which is a framework that is utilized to perform heterogeneous tasks on GPUs that are powered by CUDA, it is also as a result of the current issues that were being tackled in the scaling industry. Vortex offers a SIMT architecture with a modest ISA extension to RISC-V that supports OpenCL programme execution. They also modified the OpenCL runtime framework to take use of the new ISA. V. Agrawal et al. [16], explained that existing SIMT processors especially GPUs, are unsuitable for applications of a server since they especially are intended to maximise throughput at the price of latency, making them incapable of achieving server QoS standards. In their research, they suggested a new approach to SIMT server processors known as Massively Parallel Server Processors (MPSPs). They evaluated the magnitude of control-flow and access to the memory's divergence experienced while running unaltered server programmes on MPSP-style CPUs to begin to understand their architectural requirements and why they worked the way they did. The first results showed that the scheduler of a software that groups comparable requests together can reduce control-flow divergence, which allows for the execution of SIMT for unmodified server code. It was also discovered that, while memory-access divergence is considerable, it is manageable through adjustments in stack and heap architectures. A. Tino et al. [17], presented Single Instruction Multi-Thread Express (SIMT-X) which is a CPU microarchitecture that allows for the execution of SIMT across a considerable

number of threads of the same programme for a high throughput. The maintenance of the benefits of latency of out-of-order operation and programming ease of uniform multithreaded processors. SIMT-X takes advantage of the backend of SIMD to deliver a CPU or GPU type of functionality on a single core with a minimum overhead. Despite using a limited form of Out-of-Order (OoO), SIMT-X successfully captured the majority of the benefits of an aggressive OoO execution which utilized not more than two register mappings that are concurrent according to each architectural register, while the partial dependencies are addressed and supported an ISA which is all-purpose, this research resulted in a better performance for throughput. Caroline.C [18], presented Simty to solve the issue of the execution for generalized SIMT on RISC-V. SIMTY is a vastly multithreaded RISC-V processor core which served as some form of evidence for the vectorization of dynamic interthread. SIMTY operates groups of scalar threads that execute SPMD code in lockstep (the running of two processors concurrently, with the same set of instructions in parallel) and dynamically gathers SIMD instructions across threads in a block. SIMTY vectorizes scalar universal binaries, as opposed to current SIMD or SIMT processors such as GPUs or vector processors. There is no instruction set expansion or compiler update required. SIMTY is written in RTL (Register Transfer Level) that can be synthesised. S. Damani and V. Sarkar [19], had their paper revised and selected from papers from the 32<sup>nd</sup> international workshop LCPC, the papers were mainly about the languages and compilers for parallel computing. Their revised paper was about the separation of threads in a warp located in a branch on SIMT processors, the hardware scheduler serialises how they run which resulted in a reduced SIMT performance. They proposed a Common Subexpression Convergence (CSC), which is a new compiler optimisation which utilizes the scheduling in a cross-block to guarantee expression trees which are prevalent across paths that are separated and are moved to connecting regions and carried out by additional threads or every thread in parallel, enhancing the productivity and the time of execution of SIMT. The optimisation system in this research is built on a dynamic programming method that seeks out the most lucrative common expression subgraphs. They also provide a generic technique based on the programme dependence graph for testing the legality of our optimisation, as well as a heuristic-based cost model for determining when the optimisation should be implemented. The SIMTight project also has an aspect of hardware security, and I was able to find a useful paper. R. N. M. Watson et al. [20], made a report about an overview of CHERI. The study discusses their architectural strategy, the major microarchitectural consequences of CHERI,

their formal modelling and proof technique, the CHERI software model, their software-stack prototypes, further reading, and prospective future research fields. CHERI adds architectural features to the usual Instruction-Set Architectures (ISAs) for processors which allows smooth protection of the memory and a highly scalable software compartmentalization which increases its software performance for the various software isolated spaces so as to restrict access. CHERI's hybrid capability-system concept enables architectural characteristics to be seamlessly combined with conventional RISC architectures and microarchitectures. CHERI's capabilities are unforgeable authority tokens that may be used in C and C++ to implement both explicit pointers and implied pointers. CHERI directly eliminates an extensive variety of previously identified vulnerability types and exploit methodologies when utilised for memory protection. Aid for further scalable software categorization enables software prevention approaches such as sandboxing, this is also some form of protection against future or unknown vulnerability classes and attack methodologies. The final aspect of this project is GPU implementation of cryptographic algorithm which the next couple of papers will address. M. Bobrov [21], performed a comparative study of GPU implementation of cryptographic encryption algorithms (AES, SHA-2 and KECCAK) while utilizing CUDA library of Nvidia to get an idea of the behaviour of the three encryption algorithm in the environment of a GPU. Two types of test methodology were utilized for the experiment, the first one is total throughput and the second one is GPU throughput. The results of the experiment were categorized into the performance on a single kernel, the performance on a multi kernel and the effects of the encryption on GPU performance in a normal GPU and CPU environment. When it came to the single kernel, the AES was the better performer compared to the other 2 and it even performed better than in the case of a CPU. When it came to the performance of the multi kernel, the AES was still the better performer and it even performed better than when it was run on a single kernel, the author did not perform an experiment on SHA-2 and KECCAK for the multi kernel performance. When it came running the three algorithms in a typical environment, SHA-2 and KECCAK had a slight increase in the total time taken to run the algorithm, but AES had a significant increase in the total time taken. X. Fei et al. [22], were more focused on how the energy consumption of a GPU with parallel AES algorithm could be reduced and it could be more energy efficient so for CPU-GPU hybrid systems, an Energy-Efficient Concurrent AES encryption method was proposed to solve the issue of energy efficiency which the result of the proposal was also a great success with the utilized test methodology. Since this this project is about applications for CHERI



enabled SIMT the papers on SIMT, SIMTight and CHERI had to be reviewed because the knowledge of SIMT and CHERI are crucial because the Cheri enabled Simulator is the product of a group of people and can be found in [23], while the papers on GPU implementation had to be reviewed because of the implementation of encryption algorithms on a single kernel of the GPU and the papers on encryption algorithm are also important because of the conversion process of CUDA to NoCL would be difficult without first understanding the nature of AES, SHA-2 and KECCAK. The following papers [24], [25], [26], [27], [28] and [29], also contributed to the understanding of AES, SHA-2 and KECCAK.

### 3. TEST METHODOLOGY

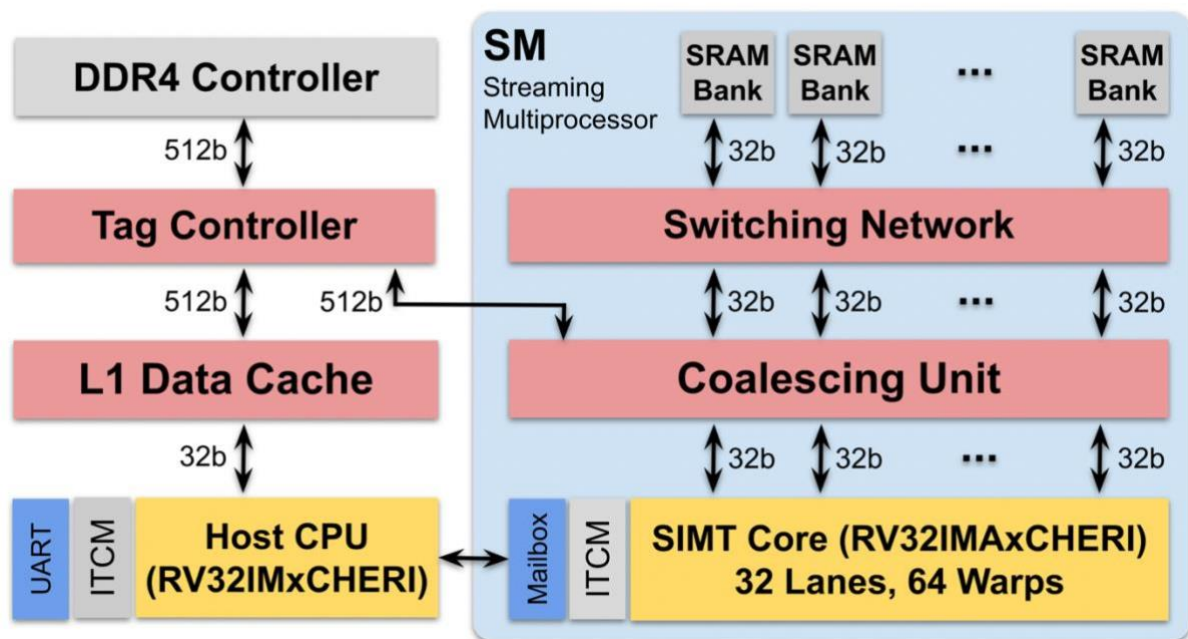
This section will discuss the test methodology that was utilized to run tests on the modified algorithms that utilize NoCL library. The methodology for testing for NoCL library algorithm which utilizes SIMTight simulator can be summarized as follows:

1. **Definition of the test objectives:** The definition of the test objectives is the most important step because in the testing methodology, it determines the next steps after it. The test objectives need to be clear, concise, measurable and specific. The goals of the project are setting up a CHERI enabled simulator successfully, modifications of some applications that utilize NoCL library and the final goal is the successful testing of the applications that utilize NoCL library with the provided benchmarks in [23].
2. **Selection of the appropriate benchmarks:** The features to test for or the appropriate benchmarks in the applications are in the test script. The benchmarks for the test were developed by the project creators in [23].
3. **Configuration of the SIMTight simulator:** The configuration of the SIMTight simulator has a couple system requirements. The below are the system requirements for the SIMTight to run smoothly and efficiently:
  - Ubuntu 20.04.
  - RISC-V Compiler.
  - Ghcup or ghc 9.2.1.

The SIMTight project also has the following features:

- i) RV32IMAXCHERI instruction set (RISC-V).
- ii) On conventional GPGPU workloads, a low-area architecture with good IPC is used.
- iii) Strong CHERI memory separation and safety.
- iv) Dynamic scalarisation (automated scalar behaviour identification in hardware).
- v) Parallel vector or scalar pipelines that take advantage of scalarisation to boost throughput.
- vi) Compression of register files and store buffers using scalarisation for decreased on-chip storage and energy.

- vii) CHERI's register size and spill overhead are significantly reduced.
- viii) In pure capability mode, it runs a CUDA-like C++ library and a benchmark suite.
- ix) Haskell implementation utilising the Blarney hardware description library.
- x) The Pebbles architecture allows for the modular separation of instruction sets and pipelines.



**Figure 1. Diagram of SIMTight.**

The diagram of figure 1 above was gotten from [23] and it displays the individual components on the SIMTight project. NoCL is a library that is very lightweight, and it is used for developing CUDA-like compute kernels in plain C++ (there is no need for a specific compute language, which is the reason for the name). NoCL was created to make it possible for CUDA kernels to be transferred to the SIMTight GPGPU SoC that is CHERI-enabled without the requirement for additional compiler effort. Alternative implementations should be viable because the NoCL API attempts to abstract over the target architecture [23]. The implementation of NoCL is defined in a single header file which needs to be included into any code

that wants to utilise NoCL library. The benchmarks to be utilized were already made available in [23]. Since a simulated hardware platform will be used.

4. **Running of the benchmarks:** The running of the benchmarks can be done automatically or manually but the SIMTight simulator will need to be started before the benchmarks can be run automatically or manually. If the running of the benchmark is done automatically then there will be the usage of a script to do so, this will be seen in section 4. If the benchmarks are run manually then it will need to be run one at a time on an SIMT kernel, this will also be seen in section 4.
5. **Analysis of the results:** The analysis of the results is the comparison between the various benchmarks so that areas for improvement can be identified.

By using this testing process, the applications that use the NoCL library can be verified to be properly evaluated and that the results are accurate and dependable.

## 4.EXPERIMENT RESULT AND ANALYSIS

This section will have an in-depth analysis of the experiment and the result that was conducted. Based off the testing methodology that was utilized the first step was the definition of the test objectives which has already been summarized in section 3. The focus of this section will be the process that was taken in the configuration of the SIMTight simulator and the challenges that were encountered in the Simulator setup and how they were overcome, the benchmarks that were utilized and the process of modification of some of the benchmarks and how they differ from the original benchmark and test on one SIMT kernel. How the original benchmarks and tests were run both manually and automatically, how the modified benchmarks and tests were able to run manually on one SIMT kernel and automatically when the test script is utilized,

### 4.1 Configuration of the SIMTight simulator

The Simulator setup was achieved by installing Oracle Virtualbox and downloading Ubuntu 20.04. The next step was the installation of the necessary libraries and then the cloning of the github repository in [23] to the local user's system because if the necessary libraries aren't installed then there will be errors and the commands to start the simulator will not be functional, an example was an error that occurred due to GHC or GHcup not being installed, so the steps needs to be followed accordingly for the configuration to be successful. Once the necessary configurations have been made then the simulator can be started by opening the terminal, changing to the sim (simulator) directory and running a make command, the simulator can then be started by running the ". /sim" command on the terminal. The CPU and SIMT cores were also checked, and they were able to run smoothly which can be seen in figures 3 to 7. Figures 2 to 14 are the evidence to display the results that were gotten after starting the simulator and the utilization of the provided testbench.

```
tevofrost@tevofrost-VirtualBox:~$ ls
cheri      Desktop  Downloads  Music      Pictures  sambashare  snap      Videos
cheribuild Documents intelFPGA_lite  old_sources_list_d  Public    SIMTight    Templates
tevofrost@tevofrost-VirtualBox:~$ cd SIMTight
tevofrost@tevofrost-VirtualBox:~/SIMTight$ cd sim
tevofrost@tevofrost-VirtualBox:~/SIMTight/sim$ make
make: 'sim' is up to date.
tevofrost@tevofrost-VirtualBox:~/SIMTight/sim$ ./sim
```

Figure 2. Starting of the Simulator.

```

tevofrost@tevofrost-VirtualBox:~/SIMTight$ cd apps/TestSuite
tevofrost@tevofrost-VirtualBox:~/SIMTight/apps/TestSuite$ make test-cpu-sim
I/add          ok
I/addi         ok
I/and          ok
I/andi         ok
I/beq          ok
I/bge          ok
I/bgeu         ok
I/blt          ok
I/bltu         ok
I/bne          ok
I/lui          ok
I/or           ok
I/ori          ok
I/simple       ok
I/sll          ok
I/slli         ok
I/slt          ok
I/slti         ok
I/sltiu        ok
I/sltu         ok
I/sra          ok

```

Figure 3. Utilizing the Simulator to test the CPU.

```

I/sra          ok
I/srai         ok
I/srl          ok
I/srli         ok
I/sub          ok
I/xor          ok
I/xori         ok
I/NoCap/auipc ok
I/NoCap/jal    ok
I/NoCap/jalr   ok
I/NoCap/lb     ok
I/NoCap/lbu    ok
I/NoCap/lh     ok
I/NoCap/lhu    ok
I/NoCap/lw     ok
I/NoCap/sb     ok
I/NoCap/sh     ok
I/NoCap/sw     ok
M/div          ok
M/divu         ok
M/mul          ok
M/mulh         ok
M/mulhsu       ok
M/mulhu        ok

```

Figure 4. Continuation of the utilization of the simulator to test the CPU.

```

tevofrost@tevofrost-VirtualBox:~/SIMTight/apps/TestSuite$ make test-simt-sim
I/add      ok
I/addi     ok
I/and      ok
I/andi     ok
I/beq      ok
I/bge      ok
I/bgeu     ok
I/blt      ok
I/bltu     ok
I/bne      ok
I/lui      ok
I/or       ok
I/ori      ok
I/simple   ok
I/sll      ok
I/slli     ok
I/slt      ok
I/slti     ok
I/sltiu    ok
I/sltu     ok
I/sra      ok
I/srai     ok
I/srl      ok

```

Figure 5. Utilizing the Simulator to test the SIMT Core.

```

I/srli     ok
I/sub      ok
I/xor      ok
I/xori     ok
I/NoCap/auipc ok
I/NoCap/jal ok
I/NoCap/jalr ok
I/NoCap/lb ok
I/NoCap/lbu ok
I/NoCap/lh ok
I/NoCap/lhu ok
I/NoCap/lw ok
I/NoCap/sb ok
I/NoCap/sh ok
I/NoCap/sw ok
M/div      ok
M/divu     ok
M/mul      ok
M/mulh     ok
M/mulhsu   ok
M/mulhu    ok
M/rem      ok
M/remu     ok

```

Figure 6. 2<sup>nd</sup> Continuation of the utilization of the Simulator to test the SIMT Core.

```

M/rem      ok
M/remu     ok
A/amoadd_w ok
A/amoand_w ok
A/amomax_w ok
A/amomaxu_w ok
A/amomin_w ok
A/amominu_w ok
A/amoor_w  ok
A/amoswap_w ok
A/amoxor_w ok

```

Figure 7. 3<sup>rd</sup> Continuation of the utilization of the Simulator to test the SIMT Core.

```

tevofrost@tevofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ killall sim
tevofrost@tevofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ cd ../
tevofrost@tevofrost-VirtualBox:~/SIMTight/apps/Samples$ cd ../
tevofrost@tevofrost-VirtualBox:~/SIMTight/apps$ cd ../
tevofrost@tevofrost-VirtualBox:~/SIMTight$ cd test
tevofrost@tevofrost-VirtualBox:~/SIMTight/test$ ./test.sh
SIMTight build: ok
Simulator build: ok
Starting simulator: ok

Test Suite (CPU, Simulation)
=====

I/add          ok
I/addi         ok
I/and          ok
I/andi         ok
I/beq          ok
I/bge          ok
I/bgeu         ok
I/blt          ok
I/bltu         ok

```

Figure 8. Shows the killing of the Simulator and the running of the benchmarks with a test shell script command.

```

I/NoCap/auipc  ok
I/NoCap/jal    ok
I/NoCap/jalr   ok
I/NoCap/lb     ok
I/NoCap/lbu    ok
I/NoCap/lh     ok
I/NoCap/lhu    ok
I/NoCap/lw     ok
I/NoCap/sb     ok
I/NoCap/sh     ok
I/NoCap/sw     ok
M/div          ok
M/divu         ok
M/mul          ok
M/mulh         ok
M/mulhsu       ok
M/mulhu        ok
M/rem          ok
M/remu         ok
Summary: ok

```

Figure 9. Continuation of the ./test.sh command in figure 8.



```
Test Suite (SIMT Core, Simulation)
=====
```

I/add	ok
I/addi	ok
I/and	ok
I/andi	ok
I/beq	ok
I/bge	ok
I/bgeu	ok
I/blt	ok
I/bltu	ok
I/bne	ok
I/lui	ok
I/or	ok
I/ori	ok
I/simple	ok
I/sll	ok
I/slli	ok
I/slt	ok
I/slti	ok
I/sltiu	ok
I/sltu	ok

Figure 10. Continuation of the `./test.sh` command in figure 8.

I/NoCap/sb	ok
I/NoCap/sh	ok
I/NoCap/sw	ok
M/div	ok
M/divu	ok
M/mul	ok
M/mulh	ok
M/mulhsu	ok
M/mulhu	ok
M/rem	ok
M/remu	ok
A/amoadd_w	ok
A/amoand_w	ok
A/amomax_w	ok
A/amomaxu_w	ok
A/amomin_w	ok
A/amominu_w	ok
A/amoor_w	ok
A/amoswap_w	ok
A/amoxor_w	ok

Summary: **ok**

Figure 11. Continuation of the `./test.sh` command in figure 8.

```

Apps (Simulation)
=====

Samples/VecAdd (build): ok
Samples/VecAdd (run): ok
Samples/Histogram (build): ok
Samples/Histogram (run): ok
Samples/Reduce (build): ok
Samples/Reduce (run): ok
Samples/Scan (build): ok
Samples/Scan (run): ok
Samples/Transpose (build): ok
Samples/Transpose (run): ok
Samples/MatVecMul (build): ok
Samples/MatVecMul (run): ok
Samples/MatMul (build): ok
Samples/MatMul (run): ok
Samples/BitonicSortSmall (build): ok
Samples/BitonicSortSmall (run): ok
Samples/BitonicSortLarge (build): ok
Samples/BitonicSortLarge (run): ok
Samples/SparseMatVecMul (build): ok

```

Figure 12. Continuation of the `./test.sh` command in figure 8.

```

Samples/Scan (run): ok
Samples/Transpose (build): ok
Samples/Transpose (run): ok
Samples/MatVecMul (build): ok
Samples/MatVecMul (run): ok
Samples/MatMul (build): ok
Samples/MatMul (run): ok
Samples/BitonicSortSmall (build): ok
Samples/BitonicSortSmall (run): ok
Samples/BitonicSortLarge (build): ok
Samples/BitonicSortLarge (run): ok
Samples/SparseMatVecMul (build): ok
Samples/SparseMatVecMul (run): ok
InHouse/BlockedStencil (build): ok
InHouse/BlockedStencil (run): ok
InHouse/StripedStencil (build): ok
InHouse/StripedStencil (run): ok
InHouse/VecGCD (build): ok
InHouse/VecGCD (run): ok
InHouse/MotionEst (build): ok
InHouse/MotionEst (run): ok

All tests passed
tevofrost@tevofrost-VirtualBox:~/SIMTight/test$

```

Figure 13. Continuation of the `./test.sh` command in figure 8.

```

tevofrost@tevofrost-VirtualBox:~/SIMTight$ cd apps/Samples/Histogram
tevofrost@tevofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ make RunSim
make: 'RunSim' is up to date.
tevofrost@tevofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ ./RunSim
Cycles: 00001b39
Instrs: 0002a8a8
Susps: 00000000
Retries: 000004af
DRAMAccs: 0000072e
Self test: PASSED

```

Figure 14. Displays the running of one of the SIMT kernel.

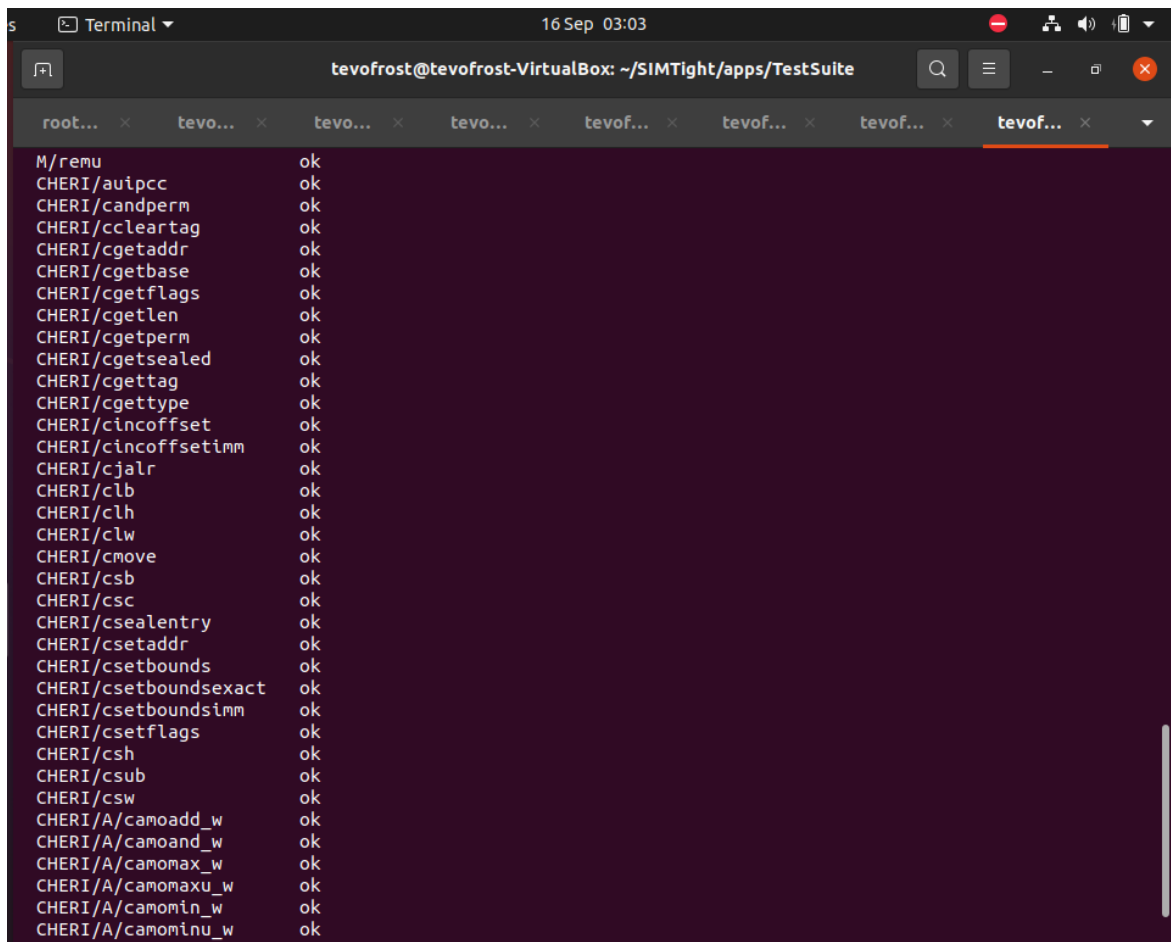
The next stage which is the process of enabling CHERI and Scalar Scalarization so that the block and threads in the block can undergo compartmentalization so as a create some

form of security to the memory and there is also an increase to the performance of the GPU. The enabling process of CHERI also needs to be done accordingly or errors will be encountered. The dependencies required by CHERI need to be met before it can be cloned from the github page in [23], if the cloning is done without meeting the dependency criteria or if the cloning is done first and the meeting of the dependency criteria is put as the second step then errors will be encountered. Once CHERI has been enabled then the results displayed on the Ubuntu terminal from the CHERI enabled simulator when it is used to test the CPU and the SIMT cores will differ slightly to when CHERI has not been enabled, the displayed results can be seen in figure 15 and figure 16. The last part is the enabling of scalarization which is an optimization technique that identifies uniform and affine vectors and processes them more effectively as scalars, thereby lowering on-chip storage and enhancing performance density. An affine vector has a constant stride between each element, whereas a uniform vector has a zero stride, implying that all elements are equal. SIMTight supports dynamic scalarisation in the hardware, at runtime, which can be activated individually for the integer register file and the register file carrying capability meta-data. The enabling of scalarization can be done by the editing of inc/Config.h (Config.h is where the configuration of the SIMTight project is done) by changing some defined values in the header file. [23]

```
Terminal 16 Sep 02:54
tevofrost@tevofrost-VirtualBox: ~/SIMTight/apps/TestSuite

root... x tevo... x tevo... x tevo... x tevo... x tevo... x tevo... x tevo... x
M/mul ok
M/mulh ok
M/mulhsu ok
M/mulhu ok
M/rem ok
M/remu ok
CHERI/auipcc ok
CHERI/candperm ok
CHERI/ccleartag ok
CHERI/cgetaddr ok
CHERI/cgetbase ok
CHERI/cgetflags ok
CHERI/cgetlen ok
CHERI/cgetperm ok
CHERI/cgetsealed ok
CHERI/cgettag ok
CHERI/cgettype ok
CHERI/cincoffset ok
CHERI/cincoffsetimm ok
CHERI/cjalr ok
CHERI/clb ok
CHERI/clh ok
CHERI/clw ok
CHERI/cmove ok
CHERI/csb ok
CHERI/csc ok
CHERI/csealentry ok
CHERI/csetaddr ok
CHERI/csetbounds ok
CHERI/csetboundsexact ok
CHERI/csetboundsimm ok
CHERI/csetflags ok
CHERI/csh ok
CHERI/csub ok
CHERI/csw ok
tevofrost@tevofrost-VirtualBox:~/SIMTight/apps/TestSuite$
```

Figure 15. Utilizing the CHERI enabled Simulator to test the CPU.



```
tevofrost@tevofrost-VirtualBox: ~/SIMTight/apps/TestSuite
root... x  tevo... x  tevo... x  tevo... x  tevof... x  tevof... x  tevof... x  tevof... x
M/remu ok
CHERI/auipcc ok
CHERI/candperm ok
CHERI/ccleartag ok
CHERI/cgetaddr ok
CHERI/cgetbase ok
CHERI/cgetflags ok
CHERI/cgetlen ok
CHERI/cgetperm ok
CHERI/cgetsealed ok
CHERI/cgettag ok
CHERI/cgettype ok
CHERI/cincoffset ok
CHERI/cincoffsetimm ok
CHERI/cjalr ok
CHERI/clb ok
CHERI/clh ok
CHERI/clw ok
CHERI/cmove ok
CHERI/csb ok
CHERI/csc ok
CHERI/csealentry ok
CHERI/csetaddr ok
CHERI/csetbounds ok
CHERI/csetboundsexact ok
CHERI/csetboundsimmm ok
CHERI/csetflags ok
CHERI/csh ok
CHERI/csub ok
CHERI/csw ok
CHERI/A/camoadd_w ok
CHERI/A/camoand_w ok
CHERI/A/camonax_w ok
CHERI/A/camonaxu_w ok
CHERI/A/camin_w ok
CHERI/A/caminu_w ok
```

**Figure 16. Utilizing the CHERI enabled Simulator to test the SIMT core.**

## 4.2 Analysis of the modified codes and the benchmark

The following codes that will be discussed are sample codes that were developed the authors in [23] to be tested on the simulator and CHERI enabled simulator and the codes utilize a library called NoCL instead of the usual CUDA libraries that GPU codes utilize, so the modified codes in this context are referring to the sample codes. Modifications to the algorithms or operators utilized in some of the sample codes were done to achieve a similar result but in a different way. One of the main goals which was to test the effectiveness and performance of the CHERI enabled Simulator with different algorithms and codes so that it can be confirmed that the simulator can work for different algorithms or codes and not just the original sample codes. A total of six of the codes were modified but one of them was modified twice, hence the reason for seven modified codes. The seven codes are as follows:

### 4.2.1 ModifiedReduce

The reduce sample code, which is the original code, first defined a kernel called reduce. The number of threads in a block is specified by a single parameter called BlockSize, in this template. Following that, the kernel defines three parameters:

- len: The vector to be summed's length.
- in: A reference to the input vector.
- sum: A pointer to an output variable containing the sum of all the elements in the input vector.

The kernel function then does the following:

- i) It creates a shared memory array with the size BlockSize.
- ii) It adds the input vector items in global memory that are assigned to each thread.
- iii) All threads in the block are synchronised.
- iv) In two steps, it adds up the components in the shared memory array:
  - Each thread adds the shared memory array elements assigned to it and the next l elements.
  - The threads then synchronise and total the preceding step's results.
- v) This operation is repeated until the shared memory array contains only one element, which is the sum of all the items in the original vector.
- vi) After that, this element is written to global memory.

The main function then creates a Reduce kernel instance and sets the len, in, and sum parameters. The `noclRunKernelAndDumpStats()` function is then used to invoke the kernel. This function executes the kernel and outputs some statistics about its execution. Finally, the main function validates the kernel's output by comparing the sum variable's value to the sum of all the components in the input vector. The kernel has passed the self-test if the two values are equivalent.

The modifiedReduce code is similar to the reduce code but the only difference is that it uses the halving recursive algorithm to sum the elements of the shared memory array in the kernel which is because the halving recursive algorithm does not have a need to access any global accesses. It is more efficient than the reduce code, but it is also more

complex. It is a better choice than the reduce code if the array is larger and the array is stored in the shared memory but the reduce code maybe a better option if the array is stored in the global memory. Figure 17 shows when the ModifiedReduce code runs on one SIMT kernel and the code can be found in appendix A.

```

12 Sep 23:15
tevofofrost@tevofofrost-VirtualBox: ~/SIMTight/apps/Samples/Histogram

MaxVecRegs: 00000080
TotalVecRegs: 00002ed5
ScalarisableInstrs: 00d26921
MaxCapVecRegs: 00000000
TotalCapVecRegs: 00000000
DRAMAccs: 0000fe65
Self test: FAILED

tevofofrost@tevofofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ make clean
rm -f *.o *.elf link.ld code.v data.v Run RunSim

tevofofrost@tevofofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ make RunSim
cpp -P -I /home/tevofofrost/SIMTight/inc /home/tevofofrost/SIMTight/apps/Common/link.ld.h > link.ld
riscv64-unknown-freebsd-clang -fuse-ld=lld -g -mabi=il32pc64 -march=rv32imxcheri -O2 -I /home/tevofofrost/SIMTight/pebbles/inc -I /home/tevofofrost/SIMTight/inc -static -mmodel=medany -fvisibility=hidden -nos
lib -fno-builtin-printf -ffp-contract=off -fno-builtin -ffreestanding -ffunction-sections -T link.ld -
app.elf /home/tevofofrost/SIMTight/apps/Common/Start.cpp sortlarge.cpp /home/tevofofrost/SIMTight/pebbles/
b/UART/IO.cpp /home/tevofofrost/SIMTight/pebbles/lib/memcpy.c
riscv64-unknown-elf-objcopy -O verilog --only-section=.text app.elf code.v
riscv64-unknown-elf-objcopy -O verilog --remove-section=.text \
--set-section-flags .bss=alloc,load,contents \
--set-section-flags .sbss=alloc,load,contents \
app.elf data.v
g++ -DSIMULATE -O2 -I /home/tevofofrost/SIMTight/pebbles/inc \
-I /home/tevofofrost/SIMTight/inc -o RunSim Run.cpp

tevofofrost@tevofofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ ./RunSim
Cycles: 000039b5
Instrs: 00058183
Susps: 00000000
Retries: 00000739
MaxVecRegs: 00000082
TotalVecRegs: 000001bb
ScalarisableInstrs: 0002f0a8
MaxCapVecRegs: 00000001
TotalCapVecRegs: 00000003
DRAMAccs: 000009fd
Self test: PASSED

tevofofrost@tevofofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$

```

**Figure 17. ModifiedReduce code result running on one SIMT Kernel.**

#### 4.2.2 Histogram128bins

The histogram sample code works by firstly using the shared memory to store the bins. This enables the kernel to update the bins in parallel in an effective manner. The kernel writes the bins to global memory when they have been changed. The code's main function initialises the input and output vectors, instantiates the kernel, and calls the kernel. It then checks the kernel's output and displays the result. The kernel function does the following in a step-by-step format:

- It saves histogram bins to shared memory.

- It sets all the bins to zero.
- It brings all the threads in the block into sync.
- It loops through the input vector, which it then updates the associated bins in the shared memory.
- It brings all the threads in the block into sync.
- It copies the shared memory bins to global memory.

To update the bins in shared memory, the kernel code calls the `atomicAdd()` function. This function ensures that the bins are updated in an atomic manner, preventing race situations. To invoke the kernel, the main function calls the `noclRunKernelAndDumpStats()` method. This function executes the kernel and outputs some statistics about its execution. The main function then validates the kernel's output by comparing the output vector's bins to the bins in a golden vector. Iterating over the input vector and counting the number of times each value appears yields the golden vector. If the bins in the output vector match those in the golden vector, the kernel passes the self-test.

The Histogram128bins which is the modified code of the Histogram sample code doesn't have a significant difference. The only difference is that the size of the histogram bins reduced from 256 to 128. Table 2 shows a comparison between histogram 256 and histogram 128. Figure 18 displays the results from when Histogram128bins code runs on one SIMT kernel and the code can be found in appendix B.

HISTOGRAM BINS ARRAY SIZE	RESOLUTION	SPEED
256	High	Slow
128	Low	Fast

**Table 2. Comparison between Histogram 256 bins and Histogram 128 bins.**





noclRunKernelAndDumpStats() function runs the kernel on the GPU and outputs statistics about kernel execution, such as execution time and thread count. The main() function initialises the input and output vectors, creates the kernel object, calls the kernel, and examines the kernel's output.

The VecSub code is the modified code of the sample code VecAdd which has a little modification that was made, as compared to the original code. The only difference is that the addition operation that was performed in the kernel function and the addition operation that was used in checking the result in the main() function was changed to subtraction so that two vectors can be subtracted. Figure 19 shows the results of when VecSub code runs on one SIMT kernel and the code can be found in appendix C.

```

aes.cpp:88:16: error: C++ requires a type specifier for all declarations
    state[1] = xor(state[1], roundkey[Nb*round_num+1]);
               ^
fatal error: too many errors emitted, stopping now [-ferror-limit=]
3 warnings and 20 errors generated.
make: *** [/home/tevofofrost/SIMTight/apps/Common/app.mk:72: app.elf] Error 1
tevofofrost@tevofofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ make clean
rm -f *.o *.elf link.ld code.v data.v Run RunSim
tevofofrost@tevofofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ make RunSim
cpp -P -I /home/tevofofrost/SIMTight/inc /home/tevofofrost/SIMTight/apps/Common/link.ld.h > link.ld
riscv64-unknown-freebsd-clang -fuse-ld=lld -g -mabi=il32pc64 -march=rv32imaxcheri -O2 -I /home/tevofofrost/
SIMTight/pebbles/inc -I /home/tevofofrost/SIMTight/inc -static -mcmodel=medany -fvisibility=hidden -nostd
lib -fno-builtin-printf -ffp-contract=off -fno-builtin -ffreestanding -ffunction-sections -T link.ld -o
app.elf /home/tevofofrost/SIMTight/apps/Common/Start.cpp VecSub.cpp /home/tevofofrost/SIMTight/pebbles/lib/U
ART/IO.cpp /home/tevofofrost/SIMTight/pebbles/lib/memcpy.c
riscv64-unknown-elf-objcopy -O verilog --only-section=.text app.elf code.v
riscv64-unknown-elf-objcopy -O verilog --remove-section=.text \
--set-section-flags .bss=alloc,load,contents \
--set-section-flags .sbss=alloc,load,contents \
app.elf data.v
g++ -DSIMULATE -O2 -I /home/tevofofrost/SIMTight/pebbles/inc \
-I /home/tevofofrost/SIMTight/inc -o RunSim Run.cpp
tevofofrost@tevofofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ ./RunSim
Cycles: 00001810
Instrs: 000264b0
Susps: 00000000
Retries: 0000043d
MaxVecRegs: 00000049
TotalVecRegs: 0000005e
ScalarisableInstrs: 0000f630
MaxCapVecRegs: 00000002
TotalCapVecRegs: 00000004
DRAMaccs: 000008b4
Self test: PASSED
tevofofrost@tevofofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$

```

Figure 19. VecSub code result running on one SIMT Kernel.

#### 4.2.4 ModifiedMatrixMultiplication and MatDiv

This subsection will consist of two modified codes of the MatMul Sample. The MatMul sample code is an NoCL kernel code that is used for the multiplication of matrices. It parallelizes the computation using a block-based technique. The kernel is created using the following parameters of which the size of the blocks is specified by BlockSize.

- A: The initial matrix's pointer.
- B: The second matrix's pointer.
- C: The output matrix pointer.
- wA: The initial matrix's width.
- wB: The second matrix's width.

The kernel begins by partitioning the input matrices into BlockSize blocks. Each thread in the kernel then computes a single member of the output matrix, which is the product of the two input blocks' corresponding elements. The outcomes are then saved to global memory. The kernel function is explained in detail in the following steps:

- i) It gets the indices of the block and thread.
- ii) It calculates the start and end indices of the A and B submatrices that the block will process.
- iii) It iterates through the A and B submatrices.
- iv) It multiplies the corresponding elements from the two submatrices and add the result to the Csub variable.
- v) It adds the variable Csub to the output matrix.

The main function initialises the input and output matrices, instantiates the kernel, calls it, and validates the results.

The ModifiedMatrixMultiplication code is one of the modified codes for MatMul sample code. The only difference between the two codes is that the ModifiedMatrixMultiplication code utilizes the `noclRunKernel()` function instead of the `noclRunKernelAndDumpStats()` function which means that the ModifiedMatrixMultiplication code will not dump any statistics about the kernel execution. Figure 20 shows the results of when

ModifiedMatrixMultiplication code runs on one SIMT kernel and the code can be found in appendix D.

The MatDiv code is the 2nd modified code for MatMul that was discussed earlier in this subsection. The main purpose of the MatDiv modified code is for the code to be able to perform the division of matrices. An error that was encountered here was the error handling for when the denominator is zero, the MatDiv code skips the division process, and it sets the associated output matrix element to zero. Table 3 shows a comparison between MatMul and MatDiv. Figure 21 displays the results from when MatDiv code runs on one SIMT kernel and the code can be found in appendix E.

Feature	Matrix Division	Matrix Multiplication
Purpose	Matrix Division ( $C = A / B$ )	Matrix Multiplication ( $C = A * B$ )
Kernel Type	MatDiv	MatMul
Computation	Element-wise Division	Matrix Multiplication
Shared Memory Usage	It is not used	It is used for efficient data access
Kernel Configuration	Based on SIMTLanes	Based on Matrix size and SIMTLanes
Matrix Initialization	Random Values for A and B	Random Values for A and B
Kernel Invocation	noclRunKernelAndDumpStats	noclRunKernelAndDumpStats
Result Verification	CPU computed division results comparison	CPU computed multiplication results comparison
Matrix Operation	Division is elementwise	Multiplication is matrix-level
Kernel Code	Division-specific operations	Multiplication specific operations

**Table 3. Comparison between Matrix Division and Matrix Multiplication.**

```
Terminal 10 Sep 13:15
tevoofrost@tevoofrost-VirtualBox: ~/SIMTight/apps/Samples/Histogram

state[0] = xor(state[0], roundkey[Nb*round_num+0]);
^
aes.cpp:88:20: error: type-id cannot have a name
state[1] = xor(state[1], roundkey[Nb*round_num+1]);
^~~~~~
aes.cpp:88:28: error: expected ')'
state[1] = xor(state[1], roundkey[Nb*round_num+1]);
^
aes.cpp:88:19: note: to match this '('
state[1] = xor(state[1], roundkey[Nb*round_num+1]);
^
aes.cpp:88:16: error: C++ requires a type specifier for all declarations
state[1] = xor(state[1], roundkey[Nb*round_num+1]);
^
fatal error: too many errors emitted, stopping now [-ferror-limit=]
3 warnings and 20 errors generated.
make: *** [/home/tevoofrost/SIMTight/apps/Common/app.mk:72: app.elf] Error 1
tevoofrost@tevoofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ make clean
rm -f *.o *.elf link.ld code.v data.v Run RunSim
tevoofrost@tevoofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ make RunSim
cpp -P -I /home/tevoofrost/SIMTight/inc /home/tevoofrost/SIMTight/apps/Common/link.ld.h > link.ld
riscv64-unknown-freebsd-clang -fuse-ld=lld -g -mabi=il32pc64 -march=rv32imaxcheri -O2 -I /home/tevoofrost/SIMTight/pebbles/inc -I /home/tevoofrost/SIMTight/inc -static -mcmodel=medany -fvisibility=hidden -nostdlib -fno-builtin-printf -ffp-contract=off -fno-builtin -ffreestanding -ffunction-sections -T link.ld -o app.elf /home/tevoofrost/SIMTight/apps/Common/Start.cpp sortlarge.cpp /home/tevoofrost/SIMTight/pebbles/lib/UART/IO.cpp /home/tevoofrost/SIMTight/pebbles/lib/memcpy.c
riscv64-unknown-elf-objcopy -O verilog --only-section=.text app.elf code.v
riscv64-unknown-elf-objcopy -O verilog --remove-section=.text \
--set-section-flags .bss=alloc,load,contents \
--set-section-flags .sbss=alloc,load,contents \
app.elf data.v
g++ -DSIMULATE -O2 -I /home/tevoofrost/SIMTight/pebbles/inc \
-I /home/tevoofrost/SIMTight/inc -o RunSim Run.cpp
tevoofrost@tevoofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ ./RunSim
Self test: PASSED
tevoofrost@tevoofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$
```

Figure 20. ModifiedMatrixMultiplication code result running on one SIMT Kernel.

```

s Terminal 12 Sep 11:30
tevoFrost@tevoFrost-VirtualBox: ~/SIMTight/apps/Samples/Histogram
root@t... x tevofro... x tevofro... x tevofro... x tevofro... x tevofro... x tevofro... x
MaxVecRegs: 000000a9
TotalVecRegs: 00004964
ScalarisableInstrs: 00096b38
MaxCapVecRegs: 0000002d
TotalCapVecRegs: 000003e7
DRAMAccs: 00007900
Self test: FAILED
tevoFrost@tevoFrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ make clean
rm -f *.o *.elf link.ld code.v data.v Run RunSim
tevoFrost@tevoFrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ make RunSim
cpp -P -I /home/tevoFrost/SIMTight/inc /home/tevoFrost/SIMTight/apps/Common/link.ld.h > link.ld
riscv64-unknown-freebsd-clang -fuse-ld=lld -g -mabi=il32pc64 -march=rv32imaxcheri -O2 -I /home/tevoFrost
/SIMTight/pebbles/inc -I /home/tevoFrost/SIMTight/inc -static -mcmodel=medany -fvisibility=hidden -nostd
lib -fno-builtin-printf -ffp-contract=off -fno-builtin -ffreestanding -ffunction-sections -T link.ld -o
app.elf /home/tevoFrost/SIMTight/apps/Common/Start.cpp sortlarge.cpp /home/tevoFrost/SIMTight/pebbles/li
b/UART/IO.cpp /home/tevoFrost/SIMTight/pebbles/lib/memcpy.c
riscv64-unknown-elf-objcopy -O verilog --only-section=.text app.elf code.v
riscv64-unknown-elf-objcopy -O verilog --remove-section=.text \
--set-section-flags .bss=alloc,load,contents \
--set-section-flags .sbss=alloc,load,contents \
app.elf data.v
g++ -DSIMULATE -O2 -I /home/tevoFrost/SIMTight/pebbles/inc \
-I /home/tevoFrost/SIMTight/inc -o RunSim Run.cpp
tevoFrost@tevoFrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ ./RunSim
Cycles: 0004bcfe
Instrs: 003d49e0
Susps: 00000000
Retries: 0002cd96
MaxVecRegs: 000000a9
TotalVecRegs: 0000495f
ScalarisableInstrs: 00096b38
MaxCapVecRegs: 0000002d
TotalCapVecRegs: 000003e8
DRAMAccs: 00007900
Self test: PASSED
tevoFrost@tevoFrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$

```

**Figure 21. MatDiv code result running on one SIMT Kernel.**

#### 4.2.5 ModifiedScan

The scan sample code, which is the original code, first defined a kernel called Scan. The kernel is based on a fundamental version from GPU Gems 3. The kernel begins by loading the input data into a shared array. The shared array is then scanned locally using a prefix sum technique. Finally, it returns the results to the output vector. The main function initialises the input and output vectors, instantiates the kernel, calls the kernel, and verifies the outcome. The following is a sequential explanation description of the kernel function:

- i) Declare two shared arrays to store the interim results, tempIn and tempOut.
- ii) Obtain the thread index t.
- iii) Iterate through the input vector as follows:
  - Fill the shared array tempOut with the supplied data.
  - A synchronisation of all threads should be done.

- Use a prefix sum technique to do a local scan on the shared array tempOut.
- A synchronisation of all threads should be done.
- Return the results to the output vector.

The main() function follows the following procedures to achieve the final result:

- i) Checks if the programme is in simulation mode.
- ii) For benchmarking, this function specifies the vector size N.
- iii) The input and output vectors are initialised.
- iv) Creates the kernel called Scan using a SIMTWarps \* SIMTLanes block size.
- v) The parameters are assigned to the kernel.
- vi) The kernel is invoked.
- vii) Checks the result that is achieved.
- viii) Displays the outcome of the result that was obtained.

The ModifiedScan code is the slightly modified version of the scan sample code. The slight difference lies in the local scan which directly loops through “offset” values that halve on every iteration (blockDim.x/2, blockDim.x/4, ...). It operates on a single shared memory array “tempOut” without swapping unlike the original code that makes use of two shared memory arrays “tempIn” and “tempOut” and swaps them in each iteration. Although both approaches result in the same goal of performing a parallel prefix sum algorithm, they slightly use algorithms that are different and memory access patterns that are different. There is a probability that the choice of implementation may affect the characteristics of its performance but the operation of computing the prefix remains the same in both codes. Table 3 shows a comparison between the advantages and the disadvantages of the local Scan of both the Scan sample code and the ModifiedScan code. Figure 22 displays the results from when ModifiedScan code runs on one SIMT kernel and the code can be found in appendix F.

Aspect	Local Scan in Scan	Local Scan in ModifiedScan
Advantages		

Parallel Prefix Sum Algorithm	It utilises a common parallel prefix sum algorithm.	It is a basic form of “Hillis-Steele Scan Algorithm” which is also a type of parallel prefix sum algorithm.
Thread Coordination	By explicitly swapping between the two memory arrays that are shared, it can help in the management of thread coordination and the efficient dependency of data.	It has a simpler implementation with a reduction in the sharing of the usage of the memory.
<b>Disadvantages</b>		
Shared Memory Usage	It utilizes two shared memory arrays which are “tempIn” and “tempOut” which doubles the usage of the shared memory in comparison to a single-array approach.	A single shared memory array “tempOut” is used which potentially reduces the shared memory overhead.
Extra Memory Traffic	An additional memory traffic can be introduced by swapping the data between “tempIn” and “tempOut”, which has a possibility of affecting the performance.	It is not applicable because there is no explicit swapping of data.
Applicability	It provides flexibility and it can also be used for various scan variants such as an inclusive or exclusive scan.	It is especially made for an inclusive scan, and it cannot be applied directly to an exclusive scan or a scan that is more complex.



Parallelism	It can provide additional parallelism due to the swapping of data that happens between the two arrays.	It can lead to less parallelism in a few cases.
-------------	--	---

**Table 3. comparison between the local Scan of both the Scan sample code and the ModifiedScan code.**

```

s Terminal 13 Sep 01:54
tevofro@tevofro-VirtualBox: ~/SIMTight/apps/Samples/Histogram

root@t... x tevofro... x tevofro... x tevofro... x tevofro... x tevofro... x tevofro... x
MaxVecRegs: 00000100
TotalVecRegs: 0001cfac
ScalarisableInstrs: 00472581
MaxCapVecRegs: 00000080
TotalCapVecRegs: 00009164
DRAMAccs: 00000afd
Self test: FAILED
tevofro@tevofro-VirtualBox:~/SIMTight/apps/Samples/Histogram$ make clean
rm -f *.o *.elf link.ld code.v data.v Run RunSim
tevofro@tevofro-VirtualBox:~/SIMTight/apps/Samples/Histogram$ make RunSim
cpp -P -I /home/tevofro/SIMTight/inc /home/tevofro/SIMTight/apps/Common/link.ld.h > link.ld
riscv64-unknown-freebsd-clang -fuse-ld=lld -g -mabi=il32pc64 -march=rv32imxcheri -O2 -I /home/tevofro/
SIMTight/pebbles/inc -I /home/tevofro/SIMTight/inc -static -mcmodel=medany -fvisibility=hidden -nostd
lib -fno-builtin-printf -ffp-contract=off -fno-builtin -ffreestanding -ffunction-sections -T link.ld -o
app.elf /home/tevofro/SIMTight/apps/Common/Start.cpp sortlarge.cpp /home/tevofro/SIMTight/pebbles/li
b/UART/IO.cpp /home/tevofro/SIMTight/pebbles/lib/memcpy.c
riscv64-unknown-elf-objcopy -O verilog --only-section=.text app.elf code.v
riscv64-unknown-elf-objcopy -O verilog --remove-section=.text \
--set-section-flags .bss=alloc,load,contents \
--set-section-flags .sbss=alloc,load,contents \
app.elf data.v
g++ -DSIMULATE -O2 -I /home/tevofro/SIMTight/pebbles/inc \
-I /home/tevofro/SIMTight/inc -o RunSim Run.cpp
tevofro@tevofro-VirtualBox:~/SIMTight/apps/Samples/Histogram$ ./RunSim
Cycles: 00008220
Instrs: 000d87b0
Susps: 00000000
Retries: 00000e67
MaxVecRegs: 00000080
TotalVecRegs: 000004f6
ScalarisableInstrs: 0005efa4
MaxCapVecRegs: 00000001
TotalCapVecRegs: 00000005
DRAMAccs: 00000e80
Self test: PASSED
tevofro@tevofro-VirtualBox:~/SIMTight/apps/Samples/Histogram$

```

**Figure 22. ModifiedScan code result running on one SIMT Kernel.**

#### 4.2.6 ModifiedBitonicSortLarge

The BitonicSort algorithm of the BitonicSortLarge sample code is a GPU-friendly parallel sorting technique. It divides the input array recursively into smaller subarrays, sorts each subarray, and then merges the sorted subarrays back together. The BitonicSort algorithm is implemented utilizing NoCL library which also uses three kernels:

- i) BitonicSortLocal: This kernel uses a bitonic merging method to sort subarrays of size LOCAL\_SIZE\_LIMIT.
- ii) BitonicMergeLocal: This kernel combines sorted subarrays with sizes equal to or less than LOCAL\_SIZE\_LIMIT.
- iii) BitonicMergeGlobal: This kernel merges sorted subarrays with sizes bigger than LOCAL\_SIZE\_LIMIT.

The sequential process of the main() function is as follows:

- i) The input and output arrays are initialised.
- ii) The BitonicSortLocal kernel is launched to sort subarrays of size LOCAL\_SIZE\_LIMIT.
- iii) For each subarray larger than LOCAL\_SIZE\_LIMIT:
  - If the subarray size is higher than or equal to twice the block size, the BitonicMergeGlobal kernel is launched to merge the sorted subarrays.
  - Otherwise, the BitonicMergeLocal kernel is launched to combine the sorted subarrays.
- iv) The sort result is checked.
- v) Displays the outcome of the result.

The ModifiedBitonicSortLarge code implements the parallel quicksort algorithm in NoCL. Parallel quicksort is a parallel sorting algorithm that works well with GPUs. It divides the input array recursively into smaller subarrays, sorts each subarray in parallel, and then merges the sorted subarrays back together. The parallel quicksort algorithm is implemented in NoCL using a single kernel called "ParallelQuicksort", on the input array, this kernel executes a parallel quicksort. The main() function is as follows:

- i) The input and output arrays are initialised.
- ii) The ParallelQuicksort kernel is instantiated.
- iii) Based on the GPU's restrictions, this function determines the valid blockDim.x and gridDim.x values.
- iv) The ParallelQuicksort kernel is executed.
- v) The sort result is checked.
- vi) Displays the result that was obtained.

The parallel quicksort algorithm implementation in NoCL is a nice example of how to utilise the NoCL library to construct a parallel sorting algorithm. It is effective and simple to grasp. Table 4 shows a comparison between the advantages and the disadvantages of both algorithms utilized in the codes. Figure 23 shows the results from when ModifiedBitonicSortLarge code runs on one SIMT kernel and the code can be found in appendix G.

FEATURE	BITONICSORTLARGE	MODIFIEDBITONICSORTLARGE
Algorithm	Bitonic Sort	Parallel Quicksort
Advantages	It is easy to comprehend, and it is efficient.	The implementation is easy and it is also efficient.
Disadvantages	It can be complicated to implement.	The analysis can be complicated.

**Table 4. comparison between the Bitonic Sort and Parallel quicksort algorithms.**

```

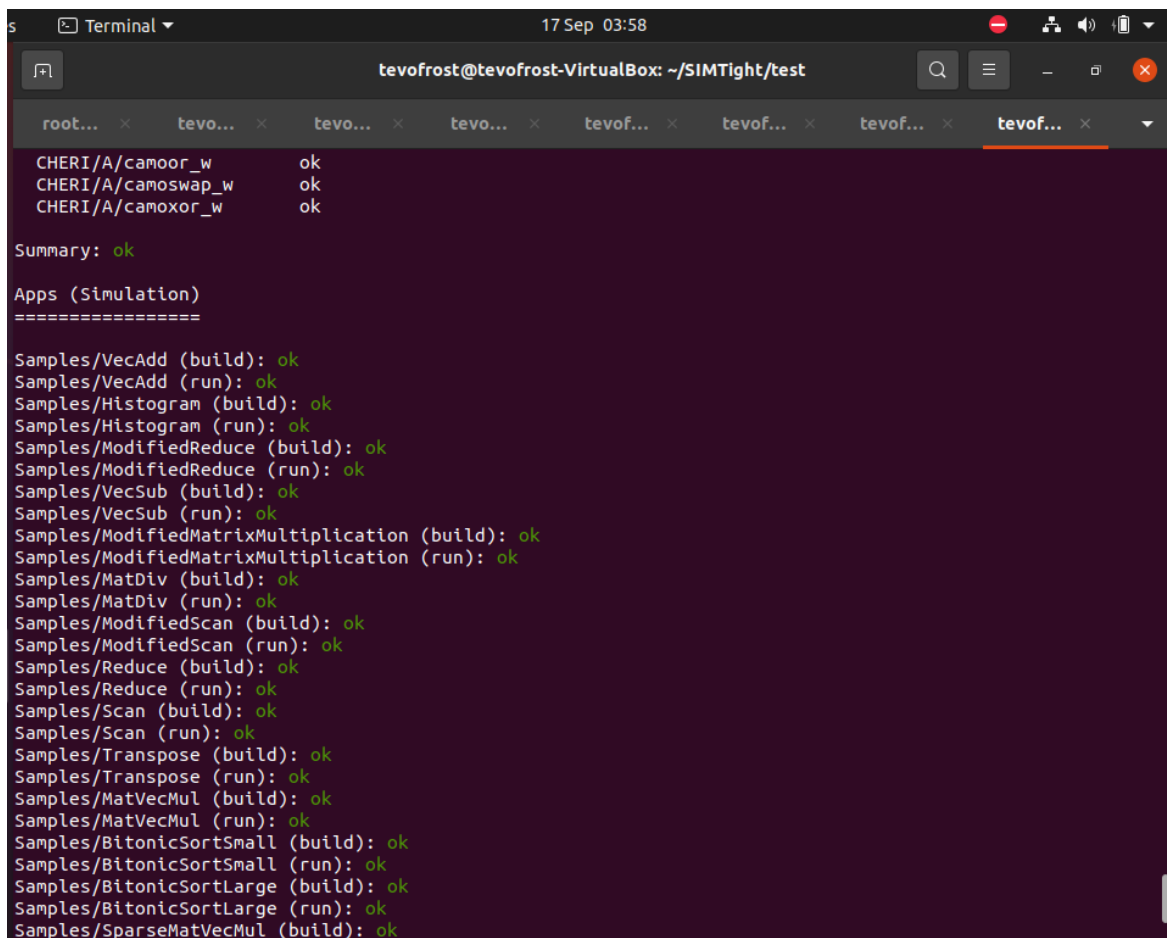
10 Sep 07:50
tevofofrost@tevofofrost-VirtualBox: ~/SIMTight/apps/Samples/Histogram

root@t... x tevofofrost@tevofofrost-VirtualBox: ~/SIMTight/apps/Samples/Histogram
b/UART/IO.cpp /home/tevofofrost/SIMTight/pebbles/lib/memcpy.c
sortlarge.cpp:116:21: error: use of undeclared identifier 'std'
    int blockSize = std::min(nextPowerOfTwo(maxThreadsPerBlock), LOCAL_SIZE_LIMIT);
                      ^
1 error generated.
make: *** [/home/tevofofrost/SIMTight/apps/Common/app.mk:72: app.elf] Error 1
tevofofrost@tevofofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ make clean
rm -f *.o *.elf link.ld code.v data.v Run RunSim
tevofofrost@tevofofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ make RunSim
cpp -P -I /home/tevofofrost/SIMTight/inc /home/tevofofrost/SIMTight/apps/Common/link.ld.h > link.ld
riscv64-unknown-freebsd-clang -fuse-ld=lld -g -mabi=il32pc64 -march=rv32imacxcheri -O2 -I /home/tevofofrost/
SIMTight/pebbles/inc -I /home/tevofofrost/SIMTight/inc -static -mcmodel=medany -fvisibility=hidden -nostd
lib -fno-builtin-printf -ffp-contract=off -fno-builtin -ffreestanding -ffunction-sections -T link.ld -o
app.elf /home/tevofofrost/SIMTight/apps/Common/Start.cpp sortlarge.cpp /home/tevofofrost/SIMTight/pebbles/li
b/UART/IO.cpp /home/tevofofrost/SIMTight/pebbles/lib/memcpy.c
riscv64-unknown-elf-objcopy -O verilog --only-section=.text app.elf code.v
riscv64-unknown-elf-objcopy -O verilog --remove-section=.text \
--set-section-flags .bss=alloc,load,contents \
--set-section-flags .sbss=alloc,load,contents \
app.elf data.v
g++ -DSIMULATE -O2 -I /home/tevofofrost/SIMTight/pebbles/inc \
-I /home/tevofofrost/SIMTight/inc -o RunSim Run.cpp
tevofofrost@tevofofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$ ./RunSim
Kernel failed due to exception
Cycles: 00005fb9
Instrs: 00074900
Susps: 00000000
Retries: 00002526
MaxVecRegs: 00000000
TotalVecRegs: 00000000
ScalarisableInstrs: 0003c340
MaxCapVecRegs: 00000000
TotalCapVecRegs: 00000000
DRAMAccs: 00002dcc
Self test: PASSED
tevofofrost@tevofofrost-VirtualBox:~/SIMTight/apps/Samples/Histogram$

```

**Figure 23. ModifiedBitonicSortLarge code result running on one SIMT Kernel.**

The above figures display the results from when the testbench is run manually on one SIMT kernel. Figures 24 and 25 below show the results of the automatic running of the benchmarks with the utilization of the “./test.sh” shell script command. As can be seen from the results in figures 24 and 25, the modified codes have been included in the benchmarks so that they can also be tested automatically, and the test was successful as all tests were able to pass.

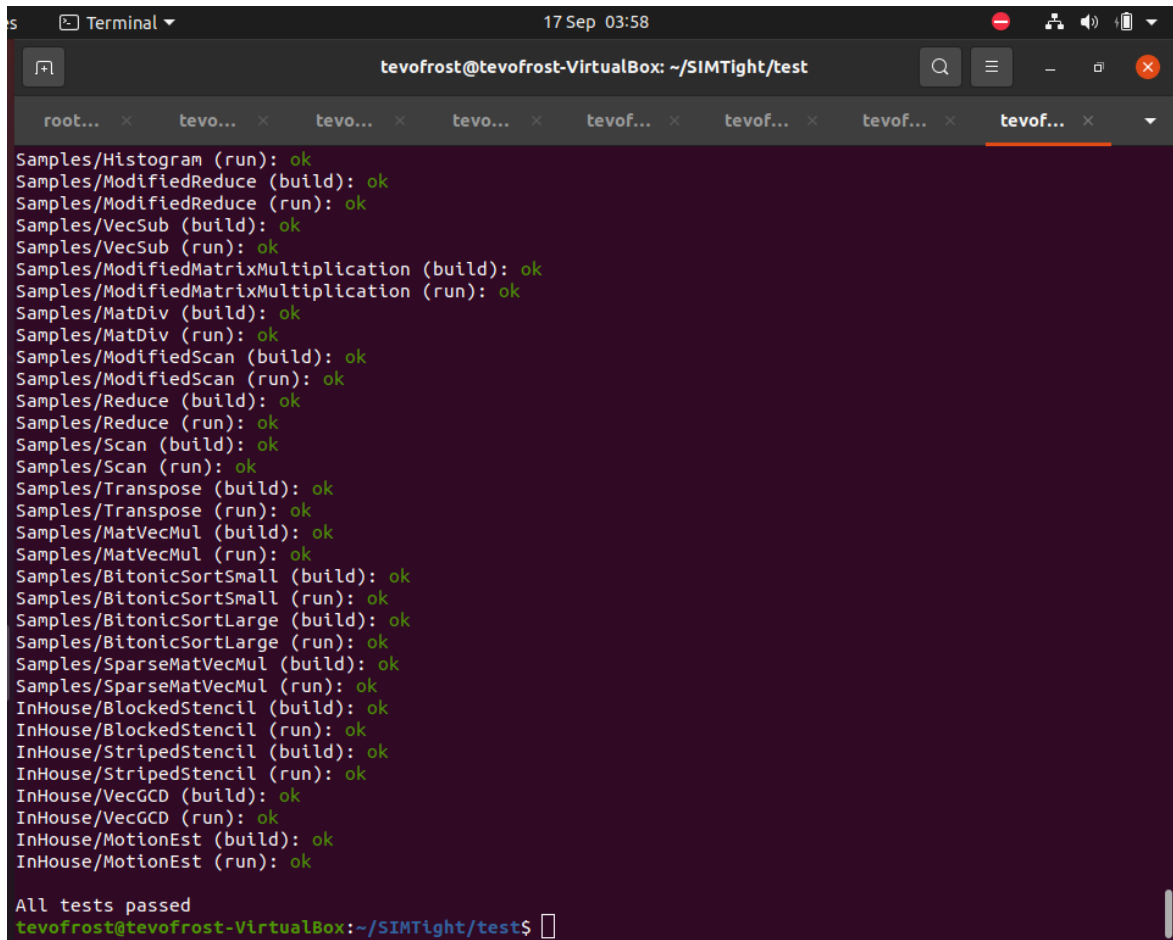


```
tevofrost@tevofrost-VirtualBox: ~/SIMTight/test
CHERI/A/camoor_w      ok
CHERI/A/camoswap_w    ok
CHERI/A/camoxor_w     ok
Summary: ok

Apps (Simulation)
=====

Samples/VecAdd (build): ok
Samples/VecAdd (run): ok
Samples/Histogram (build): ok
Samples/Histogram (run): ok
Samples/ModifiedReduce (build): ok
Samples/ModifiedReduce (run): ok
Samples/VecSub (build): ok
Samples/VecSub (run): ok
Samples/ModifiedMatrixMultiplication (build): ok
Samples/ModifiedMatrixMultiplication (run): ok
Samples/MatDiv (build): ok
Samples/MatDiv (run): ok
Samples/ModifiedScan (build): ok
Samples/ModifiedScan (run): ok
Samples/Reduce (build): ok
Samples/Reduce (run): ok
Samples/Scan (build): ok
Samples/Scan (run): ok
Samples/Transpose (build): ok
Samples/Transpose (run): ok
Samples/MatVecMul (build): ok
Samples/MatVecMul (run): ok
Samples/BitonicSortSmall (build): ok
Samples/BitonicSortSmall (run): ok
Samples/BitonicSortLarge (build): ok
Samples/BitonicSortLarge (run): ok
Samples/SparseMatVecMul (build): ok
```

**Figure 24. Automatic running of benchmarks utilizing ‘./test.sh’ shell script command.**



```
tevofrost@tevofrost-VirtualBox: ~/SIMTight/test
Samples/Histogram (run): ok
Samples/ModifiedReduce (build): ok
Samples/ModifiedReduce (run): ok
Samples/VecSub (build): ok
Samples/VecSub (run): ok
Samples/ModifiedMatrixMultiplication (build): ok
Samples/ModifiedMatrixMultiplication (run): ok
Samples/MatDiv (build): ok
Samples/MatDiv (run): ok
Samples/ModifiedScan (build): ok
Samples/ModifiedScan (run): ok
Samples/Reduce (build): ok
Samples/Reduce (run): ok
Samples/Scan (build): ok
Samples/Scan (run): ok
Samples/Transpose (build): ok
Samples/Transpose (run): ok
Samples/MatVecMul (build): ok
Samples/MatVecMul (run): ok
Samples/BitonicSortSmall (build): ok
Samples/BitonicSortSmall (run): ok
Samples/BitonicSortLarge (build): ok
Samples/BitonicSortLarge (run): ok
Samples/SparseMatVecMul (build): ok
Samples/SparseMatVecMul (run): ok
InHouse/BlockedStencil (build): ok
InHouse/BlockedStencil (run): ok
InHouse/StripedStencil (build): ok
InHouse/StripedStencil (run): ok
InHouse/VecGCD (build): ok
InHouse/VecGCD (run): ok
InHouse/MotionEst (build): ok
InHouse/MotionEst (run): ok
All tests passed
tevofrost@tevofrost-VirtualBox:~/SIMTight/test$
```

**Figure 25. Continuation of the automatic running of benchmarks utilizing ‘./test.sh’ shell script command.**

### 4.3 Comparative Analysis

This subsection will be used for the comparative analysis of the performance timewise of the original application and the modified application. Table 5 below shows the differences in the timewise performance and other features of the original application and the modified application. The application name as the name implies, is the name of the application. The original/modified column clarifies if it is an original application or a modified application. The execution time is the time taken to run the application. The performance column will specify if the performance is poor, average or good. The complexity column will indicate the complexity of the implementation. The error handling column will indicate if the implementation has an error handling that has been put in place.

Application Name	Original/Modified	Execution Time	Performance	Complexity	Error handling
Reduce	Original	1m19.537s	Good	Not Complex	N/A
ModifiedReduce	Modified from Reduce	1m2.646s	Good	Complex	N/A
Histogram	Original	1m13.137s	Good	Not Complex	N/A
Histogram128bins	Modified from Histogram	1m11.876s	Good	Not Complex	N/A
VecAdd	Original	1m48.101s	Average	Not Complex	N/A
VecSub	Modified from VecAdd	1m46.790s	Good	Not Complex	N/A
MatMul	Original	40m32.698s	Poor	Complex	N/A
ModifiedMatrixMultiplication	Modified from MatMul	38m14.982s	Poor	Complex	N/A
MatDiv	Modified from MatMul	70m10.494s	Poor	Complex	Yes
Scan	Original	1m47.920s	Average	Not Complex	N/A
ModifiedScan	Modified from Scan	1m47.810s	Average	Not Complex	N/A
BitonicSortLarge	Original	8m11.907s	Poor	Complex	N/A
ModifiedBitonicSortLarge	Modified from BitonicSortLarge	7m21.490s	Poor	Slightly Complex	N/A

**Table 5. Feature differences between the original application and the modified application.**

There were some challenges when it came with the modification of the codes because the modification of the data structure led to errors due to the libraries for the c++ functions

couldn't be found and when it was installed, the errors still occurred because the changes needed to be made to the makefile "app.mk" but these led to more errors so the course of action that was decided was to modify the algorithms which led to the success of the result outcome. It can be seen from table 5 that most of the modified codes had an improvement in terms of the execution time which was signified an improvement in performance compared to their original implementations. The time was gotten by running the "time ./RunSim" command. The performance column was determined by its execution time, compared to the overall execution time of all the codes. The complexity column was determined by using cognitive complexity and the lines of code.

## 5.FUTURE DIRECTION

This project still has room for lots of improvements like the porting of the project successfully to a Xilinx environment and being able to make it run on a low-end board like the PYNQ Z2 board, but the knowledge of hardware should be very crucial. The porting and the generation of the Verilog files was also achieved to an extent. This project can also be further improved when it comes to the modifications of the sample codes for the CHERI enabled simulator. The current modifications are limited to changing the algorithm but when the data structure is changed then new functions like malloc() need to be introduced but those require C++ libraries, so the configuration of the makefile "app.mk" in the project needs to be done. There is also the development of more codes that utilize NoCL library such as cryptographic algorithms like AES, SHA 2 and Keccak. AES was worked on, but it is incomplete, but a majority of the code has been completed and is provided in appendix H because that was also worked on but couldn't be completed due to the time being insufficient.



## **6.CONCLUSION**

The project can be considered successful because a lot of things were learned, and this project has laid a good foundation for future research into CHERI enabled SIMT because the discoveries and contributions of this research are intended to increase the understanding of CHERI-enabled SIMT-based SoCs. The setting up of the simulator, enabling CHERI and the modification of a couple of codes can be considered a success which can be seen from the figures. More research needs to be done in the SIMTight project, CHERI and NoCL library especially CHERI so that more papers can be made available for future research because there is currently a lack of materials on these which also increases the difficulty level for people who are interested in taking this research to the next level so as to contribute to the security of the Cyber industry when it comes to computing systems.

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## APPENDIX A MODIFIEDREDUCED CODE

The NoCL cpp implementation of ModifiedReduced Code is presented below. The code references implemented codes in [23].

```
#include <NoCL.h>
#include <Rand.h>

// Kernel for vector summation
template <int BlockSize> struct ModifiedReduce : Kernel {
    int len;
    int *in, *sum;

    void kernel() {
        int* block = shared.array<int, BlockSize>();

        // Sum global memory
        block[threadIdx.x] = 0;
        for (int i = threadIdx.x; i < len; i += blockDim.x)
            block[threadIdx.x] += in[i];

        __syncthreads();

        // Sum shared local memory using halving recursive algorithm
        for (int i = blockDim.x / 2; i > 0; i >>= 1) {
            if (threadIdx.x < i) {
                block[threadIdx.x] += block[threadIdx.x + i];
            }
            __syncthreads();
        }

        // Write sum to global memory
        if (threadIdx.x == 0) *sum = block[0];
    }
};

int main()
{
    // Are we in simulation?
    bool isSim = getchar();
```

```

// Vector size for benchmarking
int N = isSim ? 3000 : 1000000;

// Input and outputs
simt_aligned int in[N];
int sum;

// Initialise inputs
uint32_t seed = 1;
int acc = 0;
for (int i = 0; i < N; i++) {
    int r = rand15(&seed);
    in[i] = r;
    acc += r;
}

// Instantiate kernel
ModifiedReduce<SIMTWarps * SIMTLanes> k;

// Use a single block of threads
k.blockDim.x = SIMTWarps * SIMTLanes;

// Assign parameters
k.len = N;
k.in = in;
k.sum = &sum;

// Invoke kernel
noclRunKernelAndDumpStats(&k);

// Check result
bool ok = sum == acc;

// Display result
puts("Self test: ");
puts(ok ? "PASSED" : "FAILED");
putchar('\n');

return 0;
}

```

## APPENDIX B HISTOGRAM128BINS CODE

The NoCL cpp implementation of Histogram128bins Code is presented below. The code references implemented codes in [23].

```
#include <NoCL.h>
#include <Rand.h>

// Kernel for computing 128-bin histograms
struct Histogram128bins : Kernel {
    int len;
    unsigned char* input;
    int* bins; // Modified this to int*

    void kernel() {
        // Store histogram bins in shared local memory
        int* histo = shared.array<int, 128>(); // Changed the size to 128

        // Initialize bins
        for (int i = threadIdx.x; i < 128; i += blockDim.x)
            histo[i] = 0;

        __syncthreads();
    }
};
```

```

// Update bins
for (int i = threadIdx.x; i < len; i += blockDim.x)
    atomicAdd(&histo[input[i]], 1);

__syncthreads();

// Write bins to global memory
for (int i = threadIdx.x; i < 128; i += blockDim.x)
    bins[i] = histo[i];
}
};

int main() {
    // Are we in simulation?
    bool isSim = getchar();

    // Vector size for benchmarking
    int N = isSim ? 3000 : 1000000;

    // Input and output vectors
    nocl_aligned unsigned char input[N];
    nocl_aligned int bins[128]; // Modified the size to 128

    // ...

    // Instantiate kernel
    Histogram128bins k;

    // Use a single block of threads
    k.blockDim.x = SIMTLanes * SIMTWarps;

    // Assign parameters
    k.len = N;
    k.input = input;
    k.bins = bins; // Assign the modified bins array

    // Invoke kernel
    noclRunKernelAndDumpStats(&k);

    // Check result

```



```

bool ok = true;
int goldenBins[128]; // Modified the size to 128
for (int i = 0; i < 128; i++) goldenBins[i] = 0;
for (int i = 0; i < N; i++) goldenBins[input[i]]++;
for (int i = 0; i < 128; i++) // Modified the size to 128
    ok = ok && bins[i] == goldenBins[i];

// Display result
puts("Self test: ");
puts(ok ? "PASSED" : "FAILED");
putchar('\n');

return 0;
}

```

## APPENDIX C VEC SUB CODE

The NoCL cpp implementation of VecSub Code is presented below. The code references implemented codes in [23].

```

#include <NoCL.h>
#include <Rand.h>

```

```

// Kernel for subtracting vectors
struct VecSub : Kernel {
    int len;
    int *a, *b, *result;

    void kernel() {
        for (int i = threadIdx.x; i < len; i += blockDim.x)
            result[i] = a[i] - b[i]; //changed this to a minus operator
    }
};

int main()
{
    // Are we in simulation?
    bool isSim = getchar();

    // Vector size for benchmarking
    int N = isSim ? 3000 : 1000000;

    // Input and output vectors
    simt_aligned int a[N], b[N], result[N];

    // Initialise inputs
    uint32_t seed = 1;
    for (int i = 0; i < N; i++) {
        a[i] = rand15(&seed);
        b[i] = rand15(&seed);
    }

    // Instantiate kernel
    VecSub k;

    // Use a single block of threads
    k.blockDim.x = SIMTWarps * SIMTLanes;

    // Assign parameters
    k.len = N;
    k.a = a;
    k.b = b;
    k.result = result;

```

```
// Invoke kernel
noclRunKernelAndDumpStats(&k);

// Check result
bool ok = true;
for (int i = 0; i < N; i++)
    ok = ok && result[i] == a[i] - b[i]; //changed this to a minus operator

// Display result
puts("Self test: ");
puts(ok ? "PASSED" : "FAILED");
putchar('\n');

return 0;
}
```

## APPENDIX D MODIFIEDMATRIXMULTIPLICATION CODE

The NoCL cpp implementation of ModifiedMatrixMultiplication Code is presented below. The code references implemented codes in [23].

```
// Copyright (c) 2019, NVIDIA CORPORATION. All rights reserved.
//
// Redistribution and use in source and binary forms, with or without
// modification, are permitted provided that the following conditions
// are met:
// * Redistributions of source code must retain the above copyright
//   notice, this list of conditions and the following disclaimer.
// * Redistributions in binary form must reproduce the above copyright
//   notice, this list of conditions and the following disclaimer in the
//   documentation and/or other materials provided with the distribution.
// * Neither the name of NVIDIA CORPORATION nor the names of its
//   contributors may be used to endorse or promote products derived
//   from this software without specific prior written permission.
//
// THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS ``AS IS" AND ANY
// EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR
// PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE COPYRIGHT OWNER OR
// CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL,
// EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO,
// PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR
// PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY
// OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT
// (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE
// OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

#include <NoCL.h>
#include <Rand.h>
```

```

// Matrix multiplication C = A * B
// (wA is A's width and wB is B's width)
template <int BlockSize> struct ModifiedMatrixMultiplication : Kernel {
    int *A, *B, *C;
    int wA, wB;

    void kernel() {
        // Block index
        int bx = blockIdx.x;
        int by = blockIdx.y;

        // Thread index
        int tx = threadIdx.x;
        int ty = threadIdx.y;

        // Index of the first sub-matrix of A processed by the block
        int aBegin = wA * BlockSize * by;

        // Index of the last sub-matrix of A processed by the block
        int aEnd = aBegin + wA - 1;

        // Step size used to iterate through the sub-matrices of A
        int aStep = BlockSize;

        // Index of the first sub-matrix of B processed by the block
        int bBegin = BlockSize * bx;

        // Step size used to iterate through the sub-matrices of B
        int bStep = BlockSize * wB;

        // Csub is used to store the element of the block sub-matrix
        // that is computed by the thread
        int Csub = 0;

        // Loop over all the sub-matrices of A and B
        // required to compute the block sub-matrix
        for (int a = aBegin, b = bBegin;
            a <= aEnd;
            a += aStep, b += bStep) {

```

```

    // Multiply the two matrices together;
    // each thread computes one element
    // of the block sub-matrix
    for (int k = 0; k < BlockSize; ++k) {
        Csub += A[a + wA * ty + k] * B[b + wB * k + tx];
    }
}

// Write the block sub-matrix to device memory;
// each thread writes one element
int c = wB * BlockSize * by + BlockSize * bx;
C[c + wB * ty + tx] = Csub;
}
};

int main()
{
    // Are we in simulation?
    bool isSim = getchar();

    // Matrix dimensions for benchmarking
    // (Must be a multiple of SIMTLanes)
    int size = isSim ? 64 : 256;

    // Input and outputs
    simt_aligned int matA[size*size], matB[size*size],
        matC[size*size], matCheck[size*size];

    // Initialize matrices
    uint32_t seed = 1;
    for (int i = 0; i < size; i++)
        for (int j = 0; j < size; j++) {
            matA[i*size+j] = rand15(&seed) & 0xff;
            matB[i*size+j] = rand15(&seed) & 0xff;
            matCheck[i*size+j] = 0;
        }

    // Instantiate kernel
    ModifiedMatrixMultiplication<SIMTLanes> k;

```

```

// One block of threads per matrix tile
k.blockDim.x = SIMTLanes;
k.blockDim.y = SIMTLanes;
k.gridDim.x = size / SIMTLanes;
k.gridDim.y = size / SIMTLanes;

// Assign parameters
k.wA = size;
k.wB = size;
k.A = matA;
k.B = matB;
k.C = matC;

// Invoke kernel
noclRunKernel(&k); // Used noclRunKernel instead of noclRunKernelAndDumpStats

// Check result
bool ok = true;
for (int i = 0; i < size; i++)
    for (int j = 0; j < size; j++)
        for (int k = 0; k < size; k++)
            matCheck[i*size+j] += matA[i*size+k] * matB[k*size+j];
for (int i = 0; i < size; i++)
    for (int j = 0; j < size; j++)
        ok = ok && matCheck[i*size+j] == matC[i*size+j];

// Display result
puts("Self test: ");
puts(ok ? "PASSED" : "FAILED");
putchar('\n');

return 0;
}

```

## APPENDIX E MATDIV CODE

The NoCL cpp implementation of MatDiv Code is presented below. The code references implemented codes in [23].

```
#include <NoCL.h>
#include <Rand.h>

// Matrix division C = A / B (A divided by B)
// (wA is A's width and wB is B's width)
template <int BlockSize> struct MatDiv : Kernel {
    int *A, *B, *C;
    int wA, wB;

    void kernel() {
        // Block index
        int bx = blockIdx.x;
        int by = blockIdx.y;

        // Thread index
        int tx = threadIdx.x;
        int ty = threadIdx.y;

        // Index of the first sub-matrix of A processed by the block
        int aBegin = wA * BlockSize * by;

        // Index of the last sub-matrix of A processed by the block
        int aEnd = aBegin + wA - 1;

        // Step size used to iterate through the sub-matrices of A
        int aStep = BlockSize;

        // Index of the first sub-matrix of B processed by the block
        int bBegin = BlockSize * bx;

        // Step size used to iterate through the sub-matrices of B
        int bStep = BlockSize * wB;

        // Csub is used to store the element of the block sub-matrix
        // that is computed by the thread
        int Csub = 0;
```



```

// Loop over all the sub-matrices of A and B
// required to compute the block sub-matrix
for (int a = aBegin, b = bBegin;
    a <= aEnd;
    a += aStep, b += bStep) {

    // Divide the two matrices together;
    // each thread computes one element
    // of the block sub-matrix
    for (int k = 0; k < BlockSize; ++k) {
        // Check if the denominator (B) is zero
        if (B[b + wB * k + tx] != 0) {
            Csub += A[a + wA * ty + k] / B[b + wB * k + tx];
        }
    }
}

// Write the block sub-matrix to device memory;
// each thread writes one element
int c = wB * BlockSize * by + BlockSize * bx;
C[c + wB * ty + tx] = Csub;
};

int main() {
    // Are we in simulation?
    bool isSim = getchar();

    // Matrix dimensions for benchmarking
    // (Must be a multiple of SIMTLanes)
    int size = isSim ? 64 : 256;

    // Input and outputs
    simt_aligned int matA[size * size], matB[size * size],
        matC[size * size], matCheck[size * size];

    // Initialize matrices
    uint32_t seed = 1;

```

```

for (int i = 0; i < size; i++) {
for (int j = 0; j < size; j++) {

    matA[i * size + j] = rand15(&seed) & 0xff;
    matB[i * size + j] = rand15(&seed) & 0xff;
    matCheck[i * size + j] = 0;
}
}

// Instantiate kernel
MatDiv<SIMTLanes> k;

// One block of threads per matrix tile
k.blockDim.x = SIMTLanes;
k.blockDim.y = SIMTLanes;
k.gridDim.x = size / SIMTLanes;
k.gridDim.y = size / SIMTLanes;

// Assign parameters
k.wA = size;
k.wB = size;
k.A = matA;
k.B = matB;
k.C = matC;

// Invoke kernel
noclRunKernelAndDumpStats(&k);

// Check result
bool ok = true;
for (int i = 0; i < size; i++) {
    for (int j = 0; j < size; j++) {
        int tempResult = 0; // Temporary variable to accumulate results
        for (int k = 0; k < size; k++) {
            if (matB[k * size + j] != 0) {
                tempResult += matA[i * size + k] / matB[k * size + j];
            }
        }
    }

    matCheck[i * size + j] = tempResult; // Assign the accumulated result to matCheck
}

```

```

        ok = ok && matCheck[i * size + j] == matC[i * size + j];
    }
}

// Display result
puts("Self test: ");
puts(ok ? "PASSED" : "FAILED");
putchar('\n');

return 0;
}

```

## APPENDIX F MODIFIEDSCAN CODE

The NoCL cpp implementation of ModifiedScan Code is presented below. The code references implemented codes in [23].

```

#include <NoCL.h>
#include <Rand.h>

// Kernel for computing the parallel prefix sum (inclusive scan)
// Simple (non-work-efficient) version based on one from "GPU Gems 3"
template <int BlockSize> struct ModifiedScan : Kernel {
    int len;
    int *in, *out;

```

```

void kernel() {
    // Shared arrays
    int* tempIn = shared.array<int, BlockSize>();
    int* tempOut = shared.array<int, BlockSize>();

    // Shorthand for local thread id
    int t = threadIdx.x;

    for (int x = 0; x < len; x += blockDim.x) {
        // Load data
        tempOut[t] = in[x+t];
        __syncthreads();

        // Local scan which is a basic form of Hillis Steele Scan Algorithm
        for (int offset = blockDim.x / 2; offset > 0; offset >>= 1) {
            if (t >= offset)
                tempOut[t] += tempOut[t - offset];
            __syncthreads();
        }

        // Store data
        int acc = x > 0 ? out[x-1] : 0;
        out[x+t] = tempOut[t] + acc;
    }
};

int main()
{
    // Are we in simulation?
    bool isSim = getchar();

    // Vector size for benchmarking
    // Should divide evenly by SIMT thread count
    int N = isSim ? 4096 : 1024000;

    // Input and output vectors
    simt_aligned int in[N], out[N];

```

```
// Initialise inputs
uint32_t seed = 1;
for (int i = 0; i < N; i++) {
    in[i] = rand15(&seed);
}

// Instantiate kernel
ModifiedScan<SIMTWarps * SIMTLanes> k;

// Use a single block of threads
k.blockDim.x = SIMTWarps * SIMTLanes;

// Assign parameters
k.len = N;
k.in = in;
k.out = out;

// Invoke kernel
noclRunKernelAndDumpStats(&k);

// Check result
bool ok = true;
int acc = 0;
for (int i = 0; i < N; i++) {
    acc += in[i];
    ok = ok && out[i] == acc;
}

// Display result
puts("Self test: ");
puts(ok ? "PASSED" : "FAILED");
putchar('\n');

return 0;
}
```

## APPENDIX G MODIFIEDBITONICSORTLARGE

The NoCL cpp implementation of ModifiedBitonicSortLarge Code is presented below. The code references implemented codes in [23].

```
#include <NoCL.h>
#include <Rand.h>

#define LOCAL_SIZE_LIMIT 4096

// Function to calculate the next power of two for a given number
int nextPowerOfTwo(int n) {
    n--;
    n |= n >> 1;
    n |= n >> 2;
    n |= n >> 4;
    n |= n >> 8;
    n |= n >> 16;
    return n + 1;
}

struct ParallelQuicksort : Kernel {
    unsigned *d_DstKey_arg;
    unsigned *d_DstVal_arg;
    unsigned *d_SrcKey_arg;
    unsigned *d_SrcVal_arg;

    // Standard quicksort function
    void quicksort(unsigned *keys, unsigned *vals, int left, int right) {
        if (left < right) {
            int pivotIndex = partition(keys, vals, left, right);
            quicksort(keys, vals, left, pivotIndex - 1);
            quicksort(keys, vals, pivotIndex + 1, right);
        }
    }
};
```

```

    }
}

int partition(unsigned *keys, unsigned *vals, int left, int right) {
    unsigned pivotKey = keys[right];
    unsigned pivotVal = vals[right];
    int i = left - 1;

    for (int j = left; j < right; j++) {
        if (keys[j] <= pivotKey) {
            i++;

            // Swap keys and values
            unsigned tempKey = keys[i];
            keys[i] = keys[j];
            keys[j] = tempKey;

            unsigned tempVal = vals[i];
            vals[i] = vals[j];
            vals[j] = tempVal;
        }
    }

    // Swap the pivot element into its correct position
    unsigned tempKey = keys[i + 1];
    keys[i + 1] = keys[right];
    keys[right] = tempKey;

    unsigned tempVal = vals[i + 1];
    vals[i + 1] = vals[right];
    vals[right] = tempVal;

    return i + 1;
}

void kernel() {
    unsigned *d_SrcKey = d_SrcKey_arg + blockIdx.x * LOCAL_SIZE_LIMIT;
    unsigned *d_SrcVal = d_SrcVal_arg + blockIdx.x * LOCAL_SIZE_LIMIT;
    unsigned *d_DstKey = d_DstKey_arg + blockIdx.x * LOCAL_SIZE_LIMIT;
    unsigned *d_DstVal = d_DstVal_arg + blockIdx.x * LOCAL_SIZE_LIMIT;

```

```

    unsigned keys[LOCAL_SIZE_LIMIT];
    unsigned vals[LOCAL_SIZE_LIMIT];

    // Load data into local arrays
    for (int i = 0; i < LOCAL_SIZE_LIMIT; i++) {
        keys[i] = d_SrcKey[i];
        vals[i] = d_SrcVal[i];
    }

    // Perform parallel quicksort
    quicksort(keys, vals, 0, LOCAL_SIZE_LIMIT - 1);

    // Store sorted data
    for (int i = 0; i < LOCAL_SIZE_LIMIT; i++) {
        d_DstKey[i] = keys[i];
        d_DstVal[i] = vals[i];
    }
}
};

int main() {
    // Are we in simulation?
    bool isSim = getchar();

    // Array size and number of arrays for benchmarking
    int N = 1 << (isSim ? 13 : 18);

    // Input and output vectors
    simt_aligned unsigned srcKeys[N], srcVals[N];
    simt_aligned unsigned dstKeys[N], dstVals[N];

    // Initialise inputs
    uint32_t seed = 1;
    for (int i = 0; i < N; i++) {
        srcKeys[i] = rand15(&seed);
        srcVals[i] = rand15(&seed);
    }

    // Instantiate kernel
    ParallelQuicksort parallelSort;

```



```

parallelSort.d_SrcKey_arg = srcKeys;
parallelSort.d_SrcVal_arg = srcVals;
parallelSort.d_DstKey_arg = dstKeys;
parallelSort.d_DstVal_arg = dstVals;

// Determine the valid blockDim.x and gridDim.x values based on the GPU's limits
int maxThreadsPerBlock = 64; // Get the maximum threads per block for your GPU
int blockSize;

if (maxThreadsPerBlock < LOCAL_SIZE_LIMIT) {
    blockSize = maxThreadsPerBlock;
} else {
    blockSize = LOCAL_SIZE_LIMIT;
}

int numBlocks = (N + blockSize - 1) / blockSize;

parallelSort.blockDim.x = blockSize;
parallelSort.gridDim.x = numBlocks;

// Run parallel sorting kernel
noclRunKernelAndDumpStats(&parallelSort);

// Check result
bool ok = true;
for (int i = 0; i < N - 1; i++)
    ok = ok && dstKeys[i] <= dstKeys[i + 1];

// Display result
puts("Self test: ");
puts(ok ? "PASSED" : "FAILED");
putchar('\n');

return 0;
}

```

## APPENDIX H AES 256

The NoCL cpp implementation of AES 256 Code is presented below. The code references standard AES constant that can be located in [21].

```
#include <NoCL.h>
#include <Rand.h>

// Define Nb and Nr
#define Nb 4
// #define Nr 10

// Define NUM_ROUND_KEYS as a variable
int NUM_ROUND_KEYS;

// Define NUM_ROUNDS as a variable
int Nr = 10;

struct uchar4 {
    unsigned char x;
    unsigned char y;
    unsigned char z;
    unsigned char w;
};

const unsigned char s_box[256] = {
    0x63, 0x7C, 0x77, 0x7B, 0xF2, 0x6B, 0x6F, 0xC5, 0x30, 0x01, 0x67, 0x2B, 0xFE, 0xD7, 0xAB, 0x76,
    0xCA, 0x82, 0xC9, 0x7D, 0xFA, 0x59, 0x47, 0xF0, 0xAD, 0xD4, 0xA2, 0xAF, 0x9C, 0xA4, 0x72, 0xC0,
    0xB7, 0xFD, 0x93, 0x26, 0x36, 0x3F, 0xF7, 0xCC, 0x34, 0xA5, 0xE5, 0xF1, 0x71, 0xD8, 0x31, 0x15,
    0x04, 0xC7, 0x23, 0xC3, 0x18, 0x96, 0x05, 0x9A, 0x07, 0x12, 0x80, 0xE2, 0xEB, 0x27, 0xB2, 0x75,
    0x09, 0x83, 0x2C, 0x1A, 0x1B, 0x6E, 0x5A, 0xA0, 0x52, 0x3B, 0xD6, 0xB3, 0x29, 0xE3, 0x2F, 0x84,
    0x53, 0xD1, 0x00, 0xED, 0x20, 0xFC, 0xB1, 0x5B, 0x6A, 0xCB, 0xBE, 0x39, 0x4A, 0x4C, 0x58, 0xCF,
    0xD0, 0xEF, 0xAA, 0xFB, 0x43, 0x4D, 0x33, 0x85, 0x45, 0xF9, 0x02, 0x7F, 0x50, 0x3C, 0x9F, 0xA8,
    0x51, 0xA3, 0x40, 0x8F, 0x92, 0x9D, 0x38, 0xF5, 0xBC, 0xB6, 0xDA, 0x21, 0x10, 0xFF, 0xF3, 0xD2,
    0xCD, 0x0C, 0x13, 0xEC, 0x5F, 0x97, 0x44, 0x17, 0xC4, 0xA7, 0x7E, 0x3D, 0x64, 0x5D, 0x19, 0x73,
    0x60, 0x81, 0x4F, 0xDC, 0x22, 0x2A, 0x90, 0x88, 0x46, 0xEE, 0xB8, 0x14, 0xDE, 0x5E, 0x0B, 0xDB,
    0xE0, 0x32, 0x3A, 0x0A, 0x49, 0x06, 0x24, 0x5C, 0xC2, 0xD3, 0xAC, 0x62, 0x91, 0x95, 0xE4, 0x79,
    0xE7, 0xC8, 0x37, 0x6D, 0x8D, 0xD5, 0x4E, 0xA9, 0x6C, 0x56, 0xF4, 0xEA, 0x65, 0x7A, 0xAE, 0x08,
    0xBA, 0x78, 0x25, 0x2E, 0x1C, 0xA6, 0xB4, 0xC6, 0xE8, 0xDD, 0x74, 0x1F, 0x4B, 0xBD, 0x8B, 0x8A,
```

```
    0x70, 0x3E, 0xB5, 0x66, 0x48, 0x03, 0xF6, 0x0E, 0x61, 0x35, 0x57, 0xB9, 0x86, 0xC1, 0x1D, 0x9E,  
    0xE1, 0xF8, 0x98, 0x11, 0x69, 0xD9, 0x8E, 0x94, 0x9B, 0x1E, 0x87, 0xE9, 0xCE, 0x55, 0x28, 0xDF,  
    0x8C, 0xA1, 0x89, 0x0D, 0xBF, 0xE6, 0x42, 0x68, 0x41, 0x99, 0x2D, 0x0F, 0xB0, 0x54, 0xBB, 0x16  
};
```

```
// Define subByte function
```

```
inline uint8_t subByte(uint8_t b, const uint8_t *sbox) {  
    return sbox[b];  
}
```

```
// Define xor function
```

```
inline uchar4 Xor(uchar4 A, uchar4 B) {  
    uchar4 C;  
    C.x = A.x ^ B.x;  
    C.y = A.y ^ B.y;  
    C.z = A.z ^ B.z;  
    C.w = A.w ^ B.w;  
    return C;  
}
```

```
// Define subWord function
```

```
inline uchar4 subWord(uchar4 word, const uint8_t *sbox) {  
    word.x = subByte(word.x, sbox);  
    word.y = subByte(word.y, sbox);  
    word.z = subByte(word.z, sbox);  
    word.w = subByte(word.w, sbox);  
    return word;  
}
```

```
// Define rotWord function
```

```
inline uchar4 rotWord(uchar4 word) {  
    unsigned char temp;  
    temp = word.x;  
    word.x = word.y;  
    word.y = word.z;  
    word.z = word.w;  
    word.w = temp;  
    return word;  
}
```

```

// Define addRoundKey function
inline void addRoundKey(uchar4 *state, const uchar4 *roundkey, int round_num) {
    state[0] = Xor(state[0], roundkey[Nb * round_num + 0]);
    state[1] = Xor(state[1], roundkey[Nb * round_num + 1]);
    state[2] = Xor(state[2], roundkey[Nb * round_num + 2]);
    state[3] = Xor(state[3], roundkey[Nb * round_num + 3]);
}

// Define subBytes function
inline void subBytes(uchar4 *state, const uint8_t *sbox) {
    state[0] = subWord(state[0], sbox);
    state[1] = subWord(state[1], sbox);
    state[2] = subWord(state[2], sbox);
    state[3] = subWord(state[3], sbox);
}

// Define make_uchar4 function
inline uchar4 make_uchar4(unsigned char x, unsigned char y, unsigned char z, unsigned char w) {
    uchar4 result;
    result.x = x;
    result.y = y;
    result.z = z;
    result.w = w;
    return result;
}

// Define shiftRows function
inline void shiftRows(uchar4 *state) {
    uchar4 temp;

    // Shift the rows as per AES algorithm
    // Row 0 (no shift)
    // Row 1 (shift left by 1)
    temp = state[1];
    state[1] = make_uchar4(temp.y, temp.z, temp.w, temp.x);

    // Row 2 (shift left by 2)
    temp = state[2];
    state[2] = make_uchar4(temp.z, temp.w, temp.x, temp.y);
}

```

```

// Row 3 (shift left by 3)
temp = state[3];
state[3] = make_uchar4(temp.w, temp.x, temp.y, temp.z);
}

// Define gf_mul function for Galois Field multiplication
inline uint8_t gf_mul(uint8_t a, uint8_t b) {
    uint8_t p = 0;
    for (int i = 0; i < 8; i++) {
        if (b & 1) {
            p ^= a;
        }
        uint8_t carry = a & 0x80;
        a <<= 1;
        if (carry) {
            a ^= 0x1B; // This is the irreducible polynomial for AES
        }
        b >>= 1;
    }
    return p;
}

// Define mixColumns function
inline void mixColumns(uchar4 *state) {
    uchar4 temp0, temp1, temp2, temp3;

    for (int i = 0; i < 4; i++) {
        temp0 = state[i];
        temp1 = state[i];
        temp2 = state[i];
        temp3 = state[i];

        // Mix each column element
        state[i].x = gf_mul(temp0.x, 0x02) ^ gf_mul(temp1.y, 0x03) ^ temp2.z ^ temp3.w;
        state[i].y = temp0.x ^ gf_mul(temp1.y, 0x02) ^ gf_mul(temp2.z, 0x03) ^ temp3.w;
        state[i].z = temp0.x ^ temp1.y ^ gf_mul(temp2.z, 0x02) ^ gf_mul(temp3.w, 0x03);
        state[i].w = gf_mul(temp0.x, 0x03) ^ temp1.y ^ temp2.z ^ gf_mul(temp3.w, 0x02);
    }
}

```

```

}

struct AES : Kernel {
    const uchar4 *roundKeys_in;
    uchar4 data[Nb];
    uint32_t aes_blocks;
    uint8_t *sbox_in;
    uint8_t aes_type;
    uint8_t Nr; // Add Nr as a member variable

    void kernel() {
        uint32_t index = blockIdx.x * blockDim.x + threadIdx.x;

        NUM_ROUND_KEYS = (Nb * (Nr + 1));

        uint8_t sbox[256];
        if (threadIdx.x < 256) {
            // Copy sbox data to shared memory
            int temp = (256 + blockDim.x - 1) / blockDim.x;
            for (int i = 0; i < temp; i++) {
                int temp2 = threadIdx.x * temp + i;
                sbox[temp2] = sbox_in[temp2];
            }
        }

        uchar4 roundkeys[NUM_ROUND_KEYS];
        if (index < NUM_ROUND_KEYS)
            roundkeys[threadIdx.x] = roundKeys_in[threadIdx.x];

        __syncthreads();

        if (index >= aes_blocks)
            return;

        uchar4 state[Nb];

        // Initialize state with your data
        for (int i = 0; i < Nb; ++i) {
            state[i].x = data[i].x; // Copy each element individually

```

```

        state[i].y = data[i].y;
        state[i].z = data[i].z;
        state[i].w = data[i].w;
    }

    addRoundKey(state, roundkeys, 0);

    for (int round = 1; round < Nr; ++round) {
        subBytes(state, sbox);
        shiftRows(state);
        mixColumns(state);
        addRoundKey(state, roundkeys, round);
    }

    subBytes(state, sbox);
    shiftRows(state);
    addRoundKey(state, roundkeys, Nr);

    // Write the result to data array
    for (int i = 0; i < Nb; ++i) {
        data[i] = state[i];
    }
}

};

int main() {
    // Initialize your input data, roundKeys_in, sbox_in, and aes_type here
    uchar4 data[Nb]; // Initialize your data as an array of uchar4
    uint8_t aes_type = 1; // Initialize aes_type with the desired value
    uint32_t aes_blocks = 1; // Set the number of AES blocks to process
    uchar4 state[Nb];

    for (int i = 0; i < Nb; ++i) {
        data[i].x = 0x32; // Replace with the desired value for x component
        data[i].y = 0x88; // Replace with the desired value for y component
        data[i].z = 0x5A; // Replace with the desired value for z component
        data[i].w = 0x30; // Replace with the desired value for w component
    }
}

```

```

uchar4 roundKeys_in[NUM_ROUND_KEYS];

for (int i = 0; i < NUM_ROUND_KEYS; ++i) {
    roundKeys_in[i].x = 0x11; // Replace with the desired value for x component
    roundKeys_in[i].y = 0x22; // Replace with the desired value for y component
    roundKeys_in[i].z = 0x33; // Replace with the desired value for z component
    roundKeys_in[i].w = 0x44; // Replace with the desired value for w component
}

uint8_t sbbox_in[256];

// Assign the desired values for the elements at index i
for (int i = 0; i < 256; ++i) {
    sbbox_in[i] = 255; /* Replace with your desired value for sbbox_in[i] */;
}

// Instantiate kernel
AES k;

// Set blockDim.x and other parameters
k.blockDim.x = 256; // Set the desired blockDim.x value
k.gridDim.x = (aes_blocks + k.blockDim.x - 1) / k.blockDim.x; // Calculate gridDim.x

// Assign parameters to the kernel
k.roundKeys_in = roundKeys_in;
k.aes_blocks = aes_blocks;
k.sbbox_in = sbbox_in;
k.aes_type = aes_type;
k.Nr = Nr;

// Initialize state with your data
for (int i = 0; i < Nb; ++i) {
    k.data[i] = data[i]; // Copy each element individually
}

// Invoke the kernel using NoCL or CUDA
noclRunKernelAndDumpStats(&k);

```



```

// Copy the result from state back to data
for (int i = 0; i < Nb; ++i) {
    data[i] = state[i];
}

// Define an array to count occurrences
uint32_t aes_block_count[256] = {0};

// ...

// Calculate the result
for (int i = 0; i < Nb; ++i) {
    aes_block_count[data[i].x]++;
    aes_block_count[data[i].y]++;
    aes_block_count[data[i].z]++;
    aes_block_count[data[i].w]++;
}

/*// Compare with the computed result
bool ok = true;
for (int i = 0; i < 256; i++) {
    ok = ok && (aes_blocks == data[i]);
}
*/

bool ok = true;

for (int i = 0; i < 256; i++) {
    ok = ok && (aes_block_count[i] == aes_blocks);
}

// Display result
puts("Self test: ");
puts(ok ? "PASSED" : "FAILED");
putchar('\n');

```

```
return 0;
```

```
}
```