UPPSALA
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Practical Lab - Report

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Abstract

This report is the result of a practical lab in the course Power Electronics II 1TE766 at Uppsala University. The report documents the design, fabrication and testing of a square-wave inverter utilizing a H-bridge topology. The square-wave inverter was constructed using MOSFETs, two gate-driver circuits which controlled each leg of the inverter, a function generator and a logic inverter. Primary objectives included analyzing the effects of gate resistances, observing the impact of varying switching frequencies on output performance, testing the undervoltage-lockout feature of the gate-drivers and observing the deadtime of the gate-drivers. Testing and analyzing the inverter revealed insights into the operation of the inverter and how the bootstrap capacitors and gate resistors affected the operation of the inverter. Despite certain anomalies in waveform behaviors, the lab successfully demonstrated key principles in inverter design. Recommendations for further studies include implementing SPWM using microcontroller logic.

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1. Aim of the Project

The aim of the project was to create a square-wave inverter. This was done using MOSFETs, gate drivers, function generator and logic inverter. Resistors of different values were used for the gate and load resistances to study the effect on the inverter. To create the inverter, a H-bridge topology was used where a half-bridge gate driver was used to control each leg of the inverter. To control the half-bridge gate drivers, a function generator was used together with a logic inverter. The uninverted signal was sent to one half-bridge gate driver, and the inverted signal was sent to the other half-bridge gate driver.

The inverter could be used with a RLC load, but only a resistive load was used in testing. Focus was put on testing the undervoltage lockout feature (UVLO) and the effects of changing gate and load resistance, as well as how changing the switching frequency affected the output waveform. For this reason, output power was kept low. The half-bridge drivers and the associated bootstrapping circuit was also looked at in further detail.

2. Schematic Diagram

For the design of the inverter, we used the normal H-bridge topology but included the gate drivers with the suggested bootstrapping from the data sheet. The gate drivers feature a deadtime that prevents shoot through, and an undervoltage lockout feature. To control the gate drivers, logic signals of variable frequency are sent from a logic source, which is first sent to a logical inverter which inverts one pulse to one gate driver, the other gate driver receives a non inverted pulse. The gate drivers are supplied with 15V.

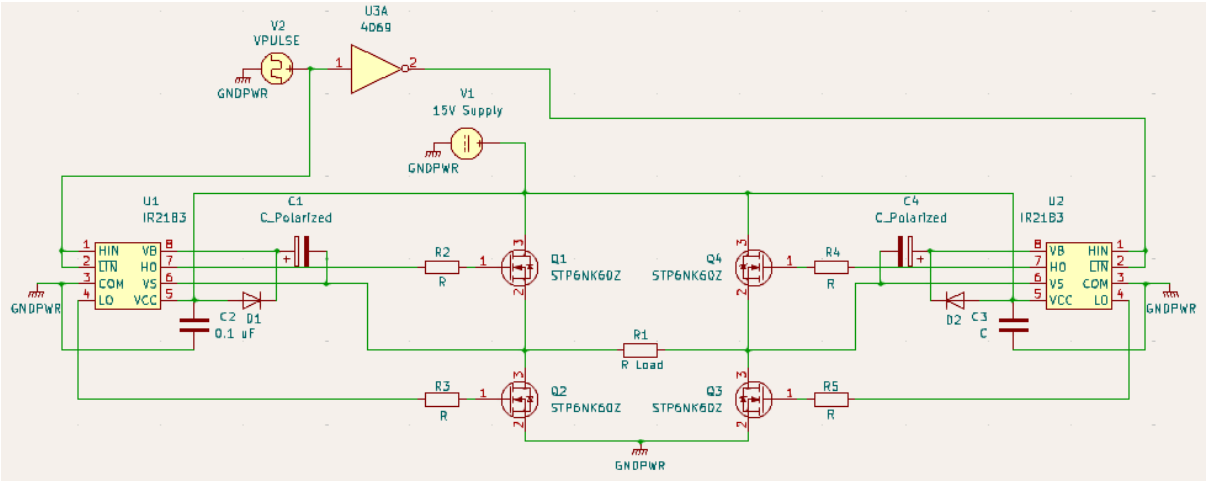

Figure 1: Circuit diagram of the inverter

The hexinverter is an IC which can invert up to 6 signals, but in Figure 1 we use an inverter diode for simplicity. The IC is supplied with 5V using a voltage regulator from the 15V supply. The reason we do not supply the full 15V when possible is because the TTL output from the function generator is 5V, we therefore need to supply only 5V.

Electrolytic capacitors were used for the bootstrapping due to their larger capacitance value. Ceramic capacitors offered better ESR values and were therefore used to filter VCC. Different components can contribute with leakage current (diodes, MOSFETs, capacitors), which can change when the UVLO of the gate driver is triggered. This feature disables the circuit when the voltage over the bootstrap capacitor drops below the voltage required to fully open the high side mosfets. For convenience, the 15V supply was used for both the H-bridge, as well as the gate drivers.

3. Design of the Inverter

This section looks into the decisions made for component selection of the inverter.

3.1 Choice of Supply Voltage and Load Resistor

The inverter is built using four STP6NK60Z n-channel enhancement power MOSFETs and a purely resistive load. Dimensioning the supply voltage and resistive load is limited by the maximum allowed drain current of the MOSFETs. To ensure safe operation, the current through the MOSFETs and the resistive load R_L should be limited and is given by

$$I_L = \frac{V_{dc}}{2 \times R_{ds} + R_L} \quad (1)$$

with $R_{ds(ON)}$ being the drain-source resistance of the MOSFETs and V_{dc} the input voltage of the H-bridge. The maximal drain current is 3.8A according to its datasheet [1]. The minimally needed load resistance is 2Ω using (1) but a maximal current of 10mA was set as a safety requirement by the lab instructors so (1) gave a resistance of 1.5kΩ.

3.2 Generation of Logic Signals

The half-bridge driver IR2183 is used at each leg. TTL pulses at 50% duty cycle are sent to each driver using a function generator; these pulses dictate the switching frequency of the inverter. Each leg operates inverted from the other to ensure synchronized switching. A hexinverter is used to send inverted and synchronized pulses to each leg. The hexinverter needs to be supplied with 5V. The 15V power supply is connected to the linear fixed voltage regulator L7805 which brings the voltage down to 5V.

3.3 Design of Bootstrap Capacitor and Filtering Capacitor

A bootstrap capacitor is required in between V_s and V_B to boost the gate-to-source voltage in high side switches. Dimensioning the bootstrap capacitor was done according to the equation obtained from the driver application note AN-978 [2].

$$C \geq \frac{2\left[2Q_g + \frac{I_{qbs(max)}}{f} + Q_{ls} + \frac{I_{Cbs(leak)}}{f}\right]}{V_{cc} - V_f - V_{LS(ON)} - V_{min}} \quad (2)$$

The equation follows the fundamental definition of capacitance and gathers the required charge to turn the high-side MOSFETs on over the gate-to-source voltage drop with a margin of factor 2. The reason for this minimum is that the driver has a built in safety feature known as the undervoltage lockout (UVLO) V_{min} which acts as a threshold voltage between V_s and V_b. If reached, the driver will not supply the MOSFETs.

To solve for the minimum capacitance with (2) a few design choices need to be discussed and values gathered. The bootstrap capacitor was chosen from the electrolytic type as these have a faster recovery time relative to the common ceramic type, they do however lead to a leakage current $I_{Cbs(leak)}$ of about $4\mu A$ whereas ceramic has close to 0. Relative to the quiescent current I_{qbs} which has a typical value of $150\mu A$[3], the low magnitude of $I_{cbs(leak)}$ for electrolytic types will not cause a drastic increase in minimum capacitance (2). The UF4004 schottky diode placed in between V_{cc} and V_s allows for unidirectional flow that creates the necessary voltage drop over the high side MOSFET. The schottky diode offers a fast recovery time and a low maximum instantaneous forward voltage drop V_f of 1V [4]. [1] states that the gate charge of the high-side MOSFET Q_g has a typical value of $33nC$, [3] gives a typical value for $V_{min} = 8.9V$ and the minimum level shift charge required per cycle Q_{ls} is $5\ nC$ [2]. The voltage drop over the low-side MOSFET while conducting $V_{LS(ON)}$ is negligible due to the low current a previously discussed alongside a low $R_{DS(ON)}$. The operating frequency will vary but to dimension the bootstrap capacitor $f = 1000Hz$ is chosen. With a supply voltage $V_{cc} = 15V$, the minimum bootstrap capacitor size is $C_{min} = 40.9nF$ (2). The bootstrap capacitor used in the inverter was an electrolytic capacitor at $1\mu F$. The oversized capacitor gave a large safety margin in order to give the possibility of lowering the operational frequency.

A filtering capacitor was used for filtering any high frequency harmonics present in the supply voltage. It also serves as a storage for charge to speed up the switching process for the low side MOSFETs. A value of $0.1\mu F$ was deemed suitable to fulfill these requirements.

As previously stated, a lack of capacitance from the bootstrap converter will cause the UVLO system to turn on. With a set value of bootstrap capacitance the operation frequency that turns on this UVLO can be calculated

$$f_{min} = \frac{(I_{Qbs(max)} + I_{Cbs(leak)})}{0.5C_{min}(V_{cc,max} - V_f - V_{LS} - V_{min}) - 2Q_g - Q_{LS}} \approx 13Hz$$

the operating frequency is upperbounded by the driver's deadtime, a built-in function which prevents shoot-through. Deadtime is the amount of time allocated to the drivers before it can proceed with a given command to switch on or switch off. The deadtime of this driver is given in [3] and the maximal operating frequency is calculated by taking the inverse of 2 switching deadtimes

$$f_{max} = \frac{1}{2 \cdot DT} \approx 1.25MHz$$

at this point the command signal would be requiring the driver to perform 2 switches before the driver has managed to complete one switch making it seem like nothing has occurred since the switching state has been brought back to its original state. Operating at high frequencies will result in higher switching losses in the MOSFETs and the bootstrap diode which can cause excessive heat buildup. If not managed with proper heat sinking capabilities the components could overheat, reducing its reliability or causing failure so the high frequency limit is set as an absolute.

3.4 Design of Gate Resistor

To finish the inverter circuit, gate resistors values need to be established. Gate resistors are used to limit the current reaching the gate terminal, too high a current damages the MOSFETs. The gate resistor can't be too large however as this would result in an increased switching time and switching losses of the MOSFETs. Using the minimal value of the high short circuit pulsed current $I_{O+} = 1.4A$ [3] and calculating the minimal gate resistor, $R_{g,min}$, given that the gate-to-source voltage is 15V, $R_{g,min} \approx 11\Omega$. A gate resistor of 33Ω was obtained for this experiment.

4. Overview of Selected Components

The lab kit that was provided for this project contained the following components.

Table 1: Overview of components of inverter.

Amount	Tag (Figure 1)	Type	Manufacturer	Product code / Value
2	D1 & D2	Diode	Onsemi	UF4004
2	U1 & U2	Gate Driver	Infineon Technologies	IR2183
1	U3	Voltage Regulator	STMicroelectronics	LV7805CV
1	U4A	Logic Inverter	STMicroelectronics	HCF4069UBEY
4	Q1 - Q4	MOSFET	STMicroelectronics	STP6NK60Z
2	C2 & C3	Ceramic Capacitor	N/A	0.1µF
2	C1 & C4	Electrolytic Capacitor	N/A	1.0µF
4	R2 - R5	Gate Resistor	N/A	33Ω
1	R1	Load Resistor	N/A	1.5kΩ

The gate resistors R2 - R5 and the bootstrapping capacitors C1 & C4 were the components that were changed when testing the inverter. Only one of the sets of components were changed at a time.

5. Fabrication Steps

For the circuit assembly a breadboard with ground and VCC cable connection was used. The MOSFETs were placed first in a H-bridge topology with the gate resistors and load resistor. The gate drivers were then placed with their surrounding circuitry capacitors, resistors and diodes. The voltage regulator and the logic inverter were placed last. Due to limited access to same colour cables, no colour coloring was done.

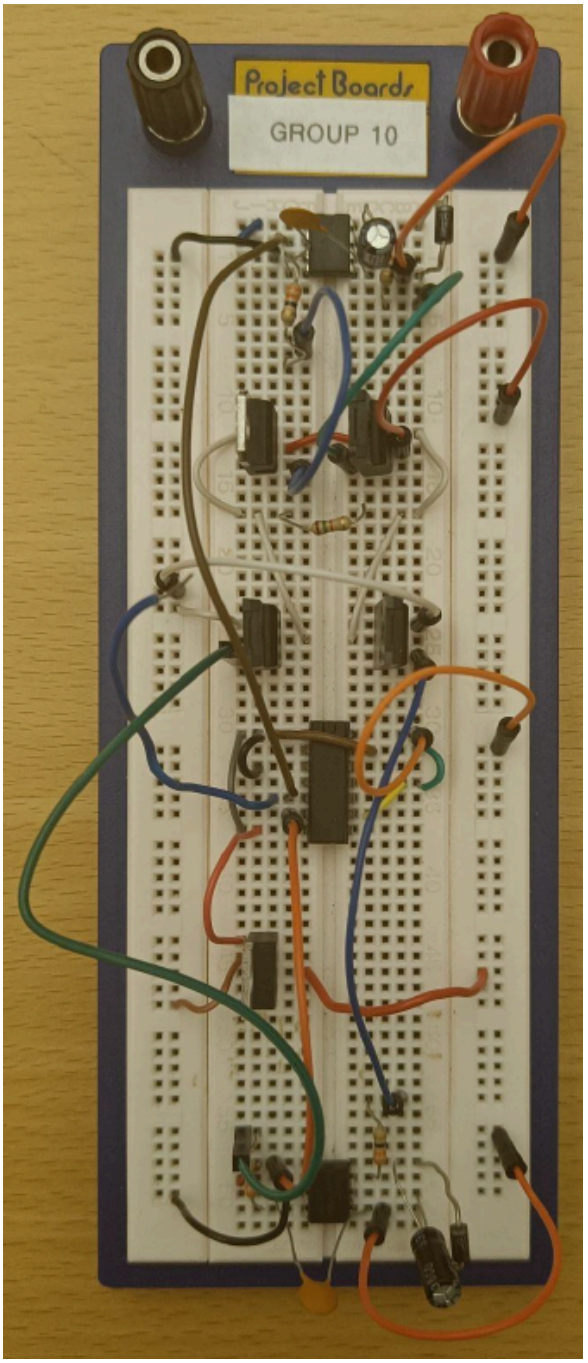

Figure 2: Finalized circuit.

This type of breadboard model had a split in the middle of the cable connected supply rails, it was therefore necessary to connect the rails in the middle, this connection is not shown in Figure 2.

6. Testing Agenda

This section presents the testing agenda used to verify the functioning of the square-wave inverter and measurements performed to be able to do a more in-depth analysis of the inverter.

6.1 Initial Functional Tests

First, tests were carried out to verify that each leg of the inverter behaved as expected before connecting the load resistor and measuring the output voltage. The tests were performed without the load resistor and with one leg disconnected at a time from the rest of the circuit. The “non-inverting” leg was tested first.

The operational frequency was set to 1 kHz by the function generator. Before connecting the logical pulses to the circuit, the amplitude and offset of the waveforms were checked with a digital oscilloscope in order to get the correct logic pulses.

Then the LO and HO pulses of the half-bridge driver were also tested. The logic pulse was sent by the function generator at 1 kHz and a differential probe was connected between LO and COM (pin 4 and pin 3 respectively) to inspect and record the LO pulse. The amplitude of the LO pulse was verified to be 15 V, which was large enough to fully open the MOSFET, as described in Section 3.1. The HO pulses were tested by connecting a differential probe between HO and Vs (pin 7 and pin 6 respectively) and the amplitude of the HO pulse was also verified to be 15 V.

The measurements described in Sections 6.2-6.5 were carried out on the non-inverting leg. Before connecting the load resistor and measuring the output voltage, as described in Section 6.6, the functioning of the “inverting” leg was tested by inspecting its pole voltage to verify that it also behaved as expected. The pole voltage of the inverting leg was compared with the pole voltage of the non-inverting leg and it was verified to be the inverted compared to the pole voltage of the non-inverting leg.

6.2 Measurement of the deadtime

After observing both the LO and HO waveforms, two differential probes were used to observe both waveforms at the same time. This was done to observe and measure the deadtime of the half-bridge driver. According to the datasheet, the half-bridge driver should have a deadtime in the interval of 280-520 ns [3]. The waveforms were recorded using a digital oscilloscope with the following settings:

- Recording 1: 1-2 fundamental periods of both waveforms.
- Recording 2: Zoomed in at the time-instance when LO goes from low to high.
- Recording 3: Zoomed in at the time-instance when LO goes from high to low.

6.3 Measurement of Bootstrap Capacitor Voltage

The voltage across the bootstrap capacitor was then observed and recorded with the following settings:

- 1-2 fundamental periods of the voltage across the bootstrap capacitor on CH1 and the TTL output from the function generator on CH2, which was used as trigger:
    - Recording 4: DC-coupled CH1, for the average value.
    - Recording 5: AC-coupled CH1, for observing the ripple of the waveform.

6.4 Measurement of the Gate-to-Source Voltage

The gate-to-source voltage of both high-side switch and low-side switch was observed and recorded with the following settings:

- Voltage between gate and source of the high-side switch and low-side switch, with the TTL output as external trigger:
    - Recording 6: 1-2 fundamental periods.
    - Recording 7: Zoomed in on the moment when the high-side switch was turning ON.
    - Recording 8: Zoomed in on the moment when the high-side switch was turning OFF.

6.5 Measurement of the Gate Current

To be able to measure the gate current, the voltage across the gate resistor of the high-side switch and low-side switch was observed and recorded with the following settings:

- 1-2 fundamental periods of the voltage across the gate resistor of the high-side switch and the low-side switch, with the TTL output on external trigger:
    - Recording 9: Zoomed in on the moment when the high-side switch is turning ON.
    - Recording 10: Zoomed in on the moment when the high-side switch is turning OFF.

6.6 Measurement of the Output Voltage

Before connecting the load resistor and measuring output voltage, the functioning of the inverting leg was verified by inspecting its pole voltage. Then the output voltage of the H-bridge was observed and recorded with the following settings:

- Recording 11: The output voltage for the case of 1 kHz operational frequency (to verify that the output voltage looked as expected).

The output voltage was also observed and recorded for 4 additional frequencies, to be able to observe the impact of changing the frequency:

- Recording 12: The output voltage for 10 Hz operational frequency.
- Recording 13: The output voltage for 100 Hz operational frequency.
- Recording 14: The output voltage for 10 kHz operational frequency.
- Recording 15: The output voltage for 100 kHz operational frequency.

The output voltage was also observed and recorded for different values of the gate resistors. Since the original value of the resistors was 33 Ω which included a safety margin, as described in Section 3.3, smaller resistors of 10 Ω were used. Note that the minimal value of the gate resistors were calculated to be approximately 11 Ω in Section 3.4, however, the resistors that were available and closest in value to 11 Ω were 10 Ω, hence, they were used.

The operational frequency was again set to 1 kHz and the following waveforms for the case of lower resistors were observed and recorded again:

- Voltage between gate and source of the high-side switch and low-side switch:
    - Recordings 16 and 17: Zoomed in on both transitions as before.

- Voltage across the gate resistor of the high-side switch and low-side switch:
    - Recordings 18 and 19: Zoomed in on both transitions as before.

- The output voltage:
    - Recording 20: 1-2 fundamental periods.
    - Recordings 21 and 22: Zoomed in on both transitions to get the rise-time and fall-time.

6.7 Measurement of the Undervoltage-Lockout Feature

The undervoltage-lockout feature of the half-bridge driver was also tested. This was done by lowering the operational frequency until an undistorted square-wave output voltage was no longer obtained. The undervoltage-lockout was observed and recorded with the following setting:

- Recording 23: Output voltage with the original 1.0 µF bootstrap capacitor at undervoltage-lockout condition.

To be able to see how the value of the bootstrap capacitor affects at what frequency the undervoltage-lockout occurs, the output voltage for a smaller value of the bootstrap capacitor was observed and recorded with the following setting:

- Recording 24: Output voltage with a 0.1 µF bootstrap capacitor at undervoltage-lockout condition.

To be able to see at what voltage level the undervoltage-lockout occurred, the voltage across the bootstrap capacitor on the non-inverting leg and load resistor was observed and recorded with the following setting:

- Recording 25: Voltage across the bootstrap capacitor, 1.0 µF, and load resistor 33 Ω.

7. Results and Discussion

In this section, the results of the measurements described in Sections 6.2-6.7 are presented and discussed. All recordings were plotted using the MATLAB script in Appendix 10.1.

7.1 Half-Bridge Driver Characteristics

The deadtime of the half-bridge driver was measured according to the tests presented in section 6.2. It is enough to analyze recordings 2 and 3 to determine the deadtime of the half-bridge driver. Recording 2 is shown in Figure 3 and recording 3 is shown in Figure 4.

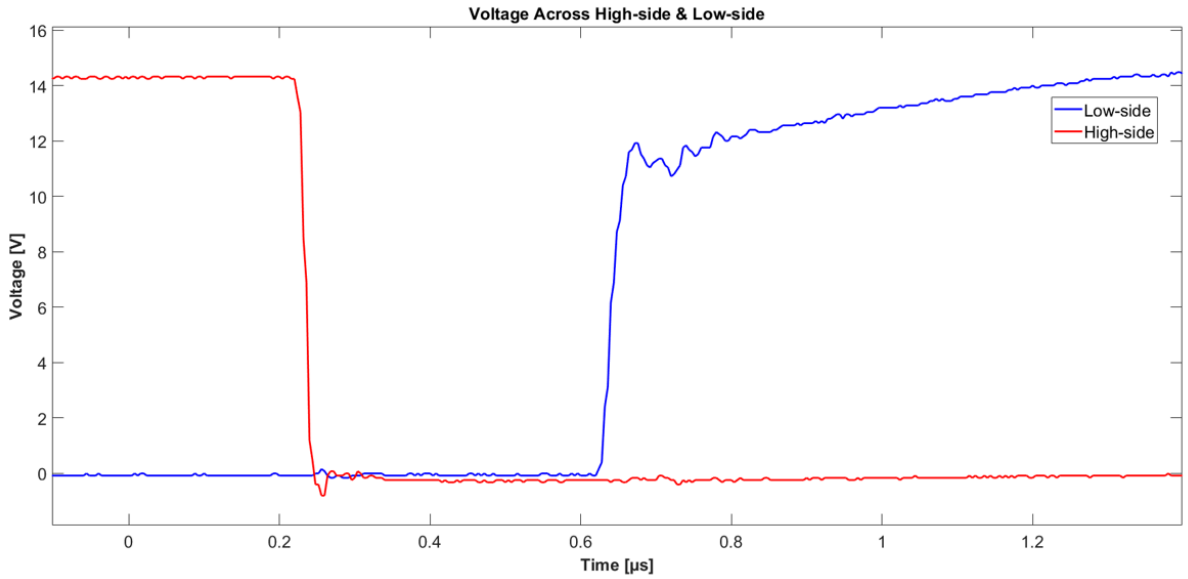

Figure 3: Recording 2, LO goes from low to high.

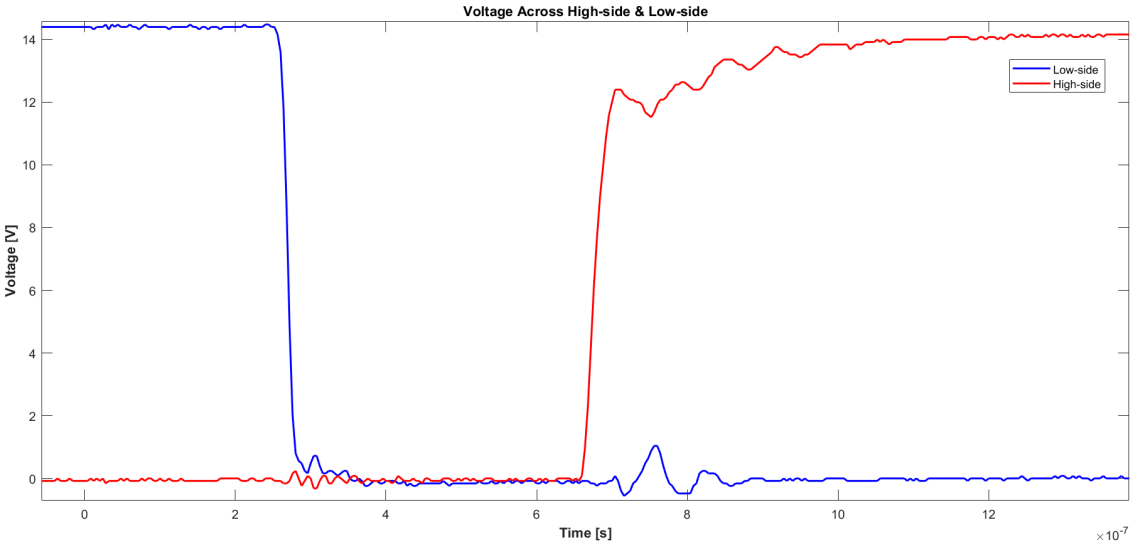

Figure 4: Recording 3, LO goes from high to low.

The deadtime was calculated by use of the MATLAB script in appendix 10.2 and was calculated to be $400 \pm 4\,ns$. According to the datasheet of the half-bridge driver it has a deadtime of 280-520 ns for a supply voltage of 15 V. The typical value for the half-bridge driver is 400 ns. The turn off delay time of the MOSFET is 42 ns according to its datasheet, the deadtime of the driver is therefore satisfactory and sufficient to avoid shoot-through.

7.2 The Effect of the Bootstrap Capacitor

The voltage across the bootstrap capacitor was measured according to the tests presented in section 6.3. The voltage waveform across the bootstrap capacitor was reconstructed by obtaining the mean of the DC-coupled measurement of recording 4 and adding it to the AC-coupled measurement of recording 5. The reconstructed voltage waveform across the bootstrap capacitor is shown in Figure 5.

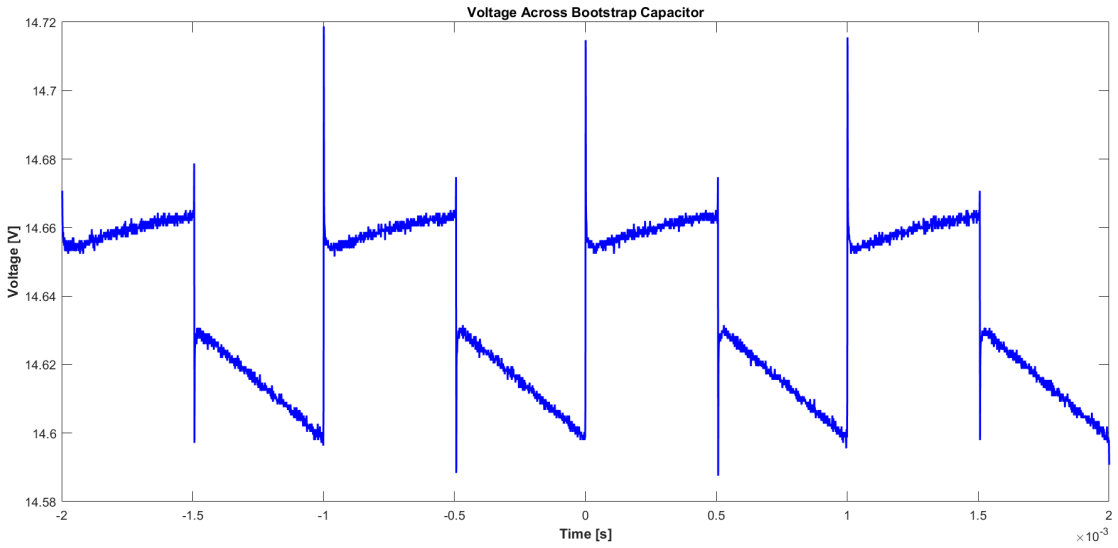

Figure 5: Reconstructed waveform of the voltage across the bootstrap capacitor.

The voltage drop that occurs while the MOSFET is turned ON in Figure 5 is 33mV, the total charge that this equates to is 33nC, following the same principle of equation (2). The typical value of charge required to open the gate is 33nC [1] which checks out nicely. Excluding the sudden spike in voltage as seen at every point of switching, the maximal voltage across the bootstrap capacitor is higher than expected. The diode should cause a voltage drop of 0.4V or higher [4] but the voltage drop here is less than that, the discrepancy may be because of an offset that was not correctly adjusted in recording 4, the DC coupling test seems to have caused a slightly off-centered waveform.

7.3 The Effect of the Gate Resistor

The gate-to-source voltages were measured according to the tests presented in section 6.4. Recording 6 is shown in Figure 6, recording 7 is shown in Figure 7 and recording 8 is shown in Figure 8.

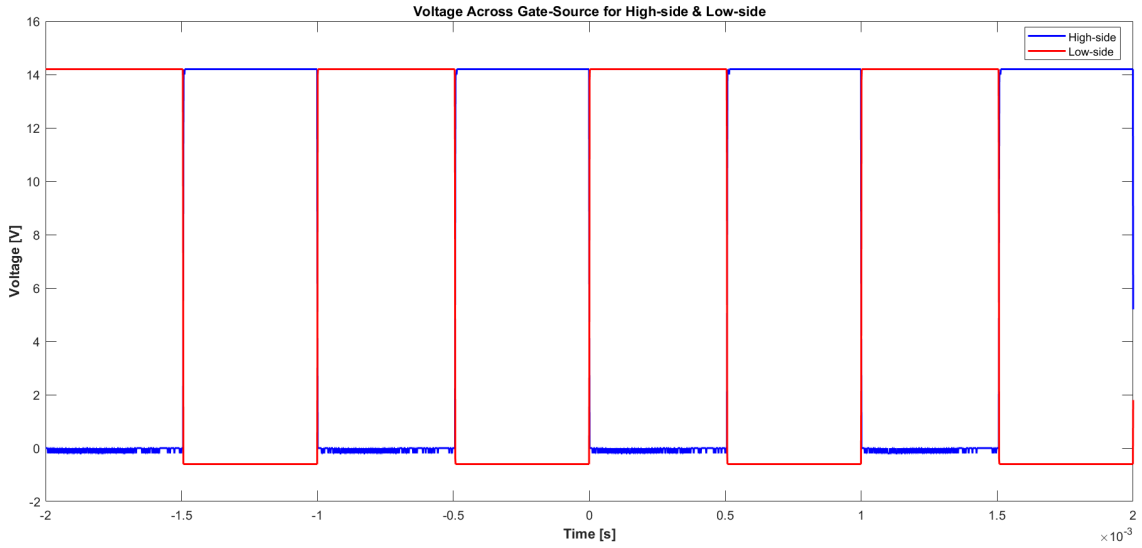

Figure 6: Recording 6, overview of the gate-to-source voltage for the high-side switch and low-side switch. 33 Ω gate resistors.

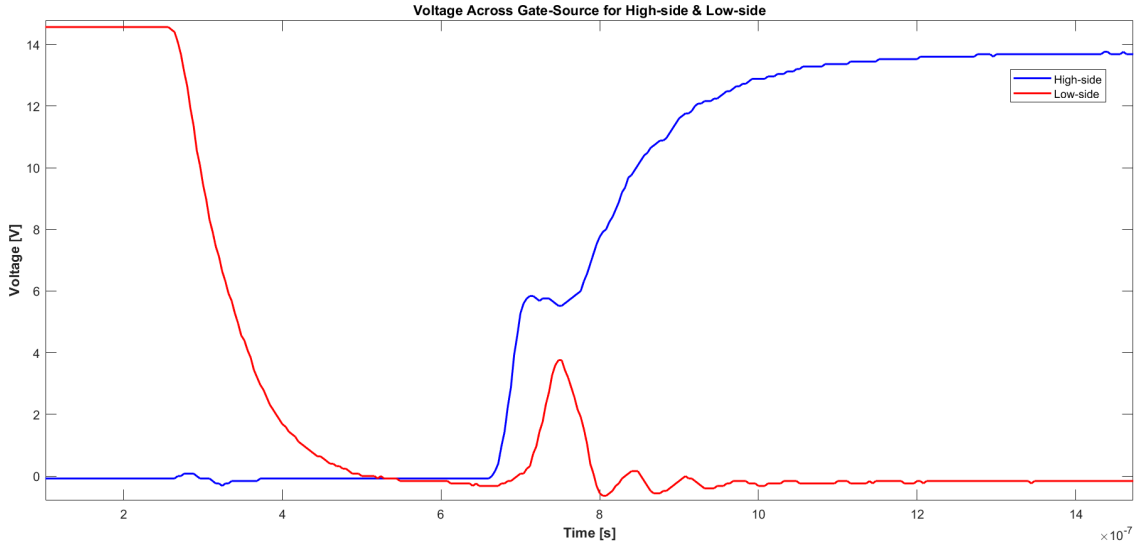

Figure 7: Recording 7, gate-to-source voltage, high-side switch turning ON. 33 Ω gate resistors.

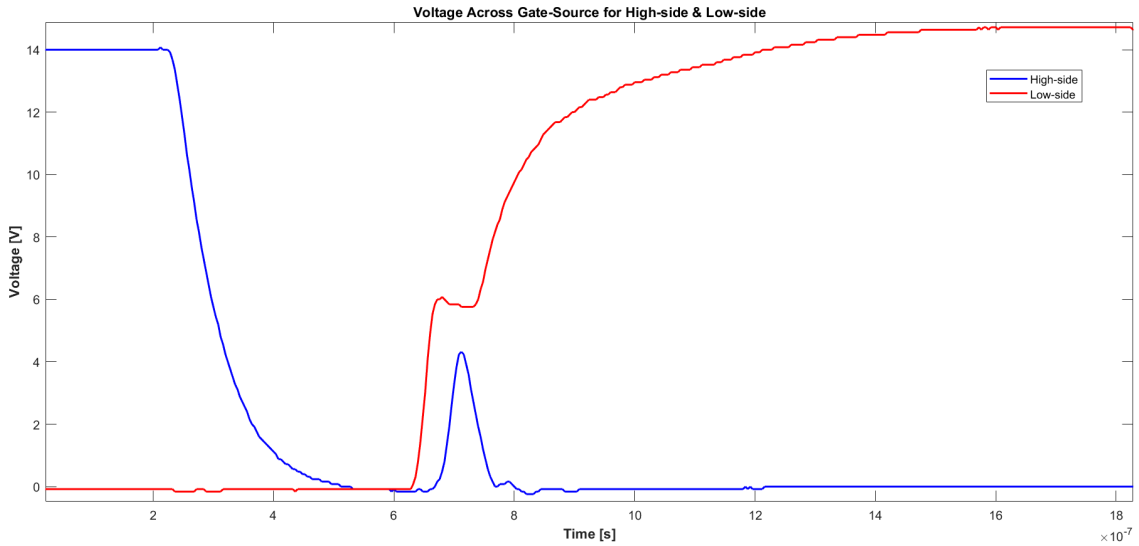

Figure 8: Recording 8, gate-to-source voltage, high-side switch turning OFF. 33 Ω gate resistors.

Table 2: Rise-time, fall-time and peak gate-to-source voltage, for the case of 33 Ω gate resistors.

	Low-side	High-side	Expected Value
Rise time	$(416 \pm 4)\ ns$	$(292 \pm 4)\ ns$	14 ns (typ)
Fall time	$(132 \pm 4)\ ns$	$(148 \pm 4)\ ns$	19 ns (typ)
Peak G-S voltage	14.72 V	13.76 V	N/A

The rise-time and fall-time were calculated between 10% and 90% of the maximum value and vice versa. In this case, the rise-time and fall-time does not match the expected value from the datasheet [1]. The Peak G-S voltage was measured in recordings 7-8, Figure 7 and 8, and was 13.76 V and 14.72 V. The used G-S voltage from the datasheet is 10 V with 4.7 Ω resistor. This probably contributes to the large difference between the measured rise/fall-times and the expected values.

The gate current was obtained by measuring the voltage across the gate resistor for the high-side switch and low-side switch according to the tests presented in section 6.5. The gate current waveforms were calculated in MATLAB by the use of Ohm's law on recording 9 and 10 and are shown in Figure 9 and 10 respectively.

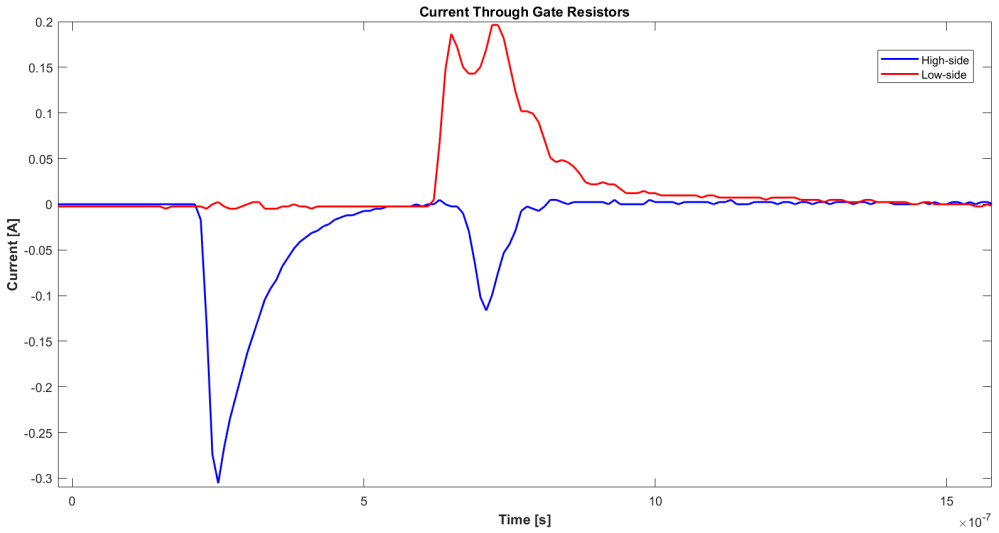

Figure 9: Gate-current, derived from recording 9, high-side switch turning ON. 33 Ω gate resistors.

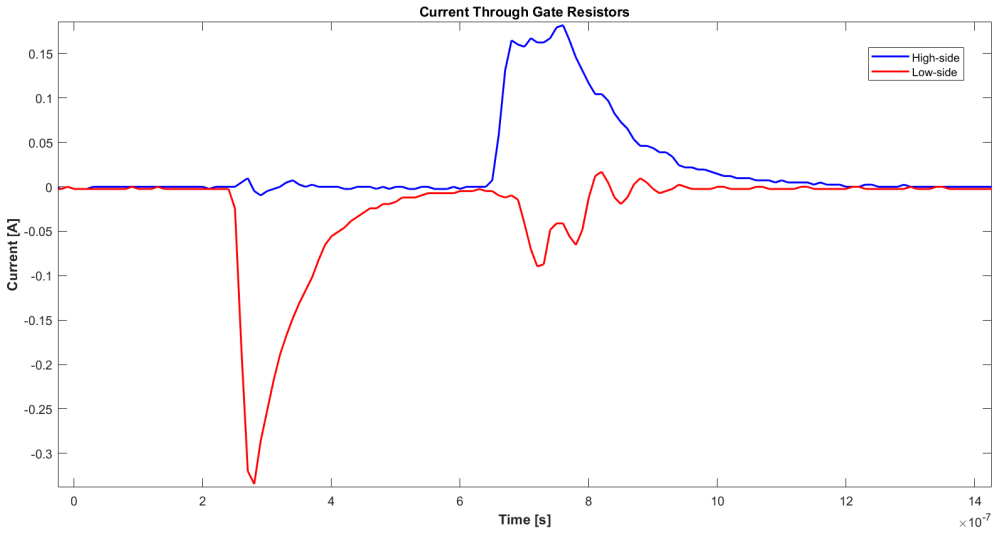

Figure 10: Gate-current, derived from recording 10, high-side switch turning OFF. 33 Ω gate resistors.

Table 3: Peak current and flow of charge into the gate for high-side and low-side turning on, for the case of 33 Ω gate resistors.

	Low-side	High-side	Expected Value
Peak Current	196.4 mA	181.8 mA	N/A
Flow of Charge	32.98 nC	33.418 nC	33 nC (typ turning on)

From Table 3, we can see that the calculated flow of charge is very close to the expected value of 33 nC using the 33Ω gate resistors. Excluding charge lost due to leakage, charge entering low-side should be equal to charge leaving high-side and vice versa when switching.

The original gate resistors had a resistance value of 33 Ω. Since this value included a safety margin, gate resistors of 10 Ω were also used see how the MOSFETs performed. The circuit was then tested according to the tests presented in section 6.6. Recording 16 is shown in Figure 11 and recording 17 is shown in Figure 12.

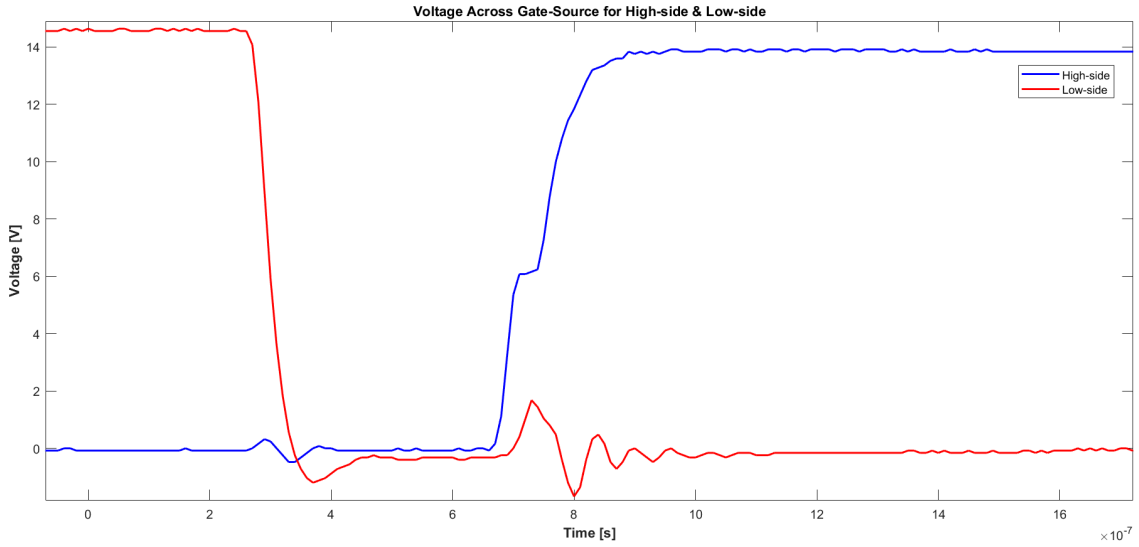

Figure 11: Recording 16, gate-to-source voltage , high-side switch turning ON. 10 Ω gate resistors.

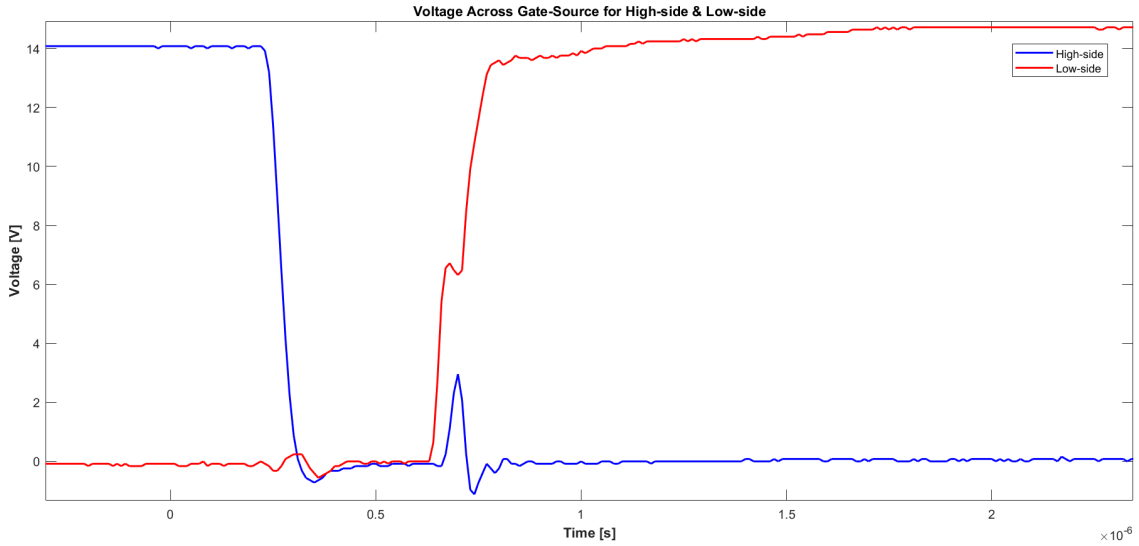

Figure 12: Recording 17, gate-to-source voltage, high-side switch turning OFF. 10 Ω gate resistors.

Table 4: Rise-time, fall-time and peak gate-to-source voltage, for the case of 10 Ω gate resistors.

	Low-side	High-side	Expected Value
Rise time	$(140 \pm 10)\ ns$	$(140 \pm 10)\ ns$	14 ns (typ)
Fall time	$(60 \pm 10)\ ns$	$(60 \pm 10)\ ns$	19 ns (typ)
Peak G-S voltage	14.72 V	13.92 V	N/A

The gate current waveforms were also obtained for the case of 10 Ω gate resistors according to the tests presented in section 6.6. Recording 18 is shown in Figure 13 and recording 19 in Figure 14. Important to note that when switching low & high-side as seen in Figure 8 & 12, there is a small voltage increase for the switched off MOSFET that can exceed gate threshold voltage. This behaviour was seen for both 10 Ω and 33 Ω gate resistance, with a larger voltage seen for the 33 Ω. A large enough voltage for a prolonged time can cause throughshoot.

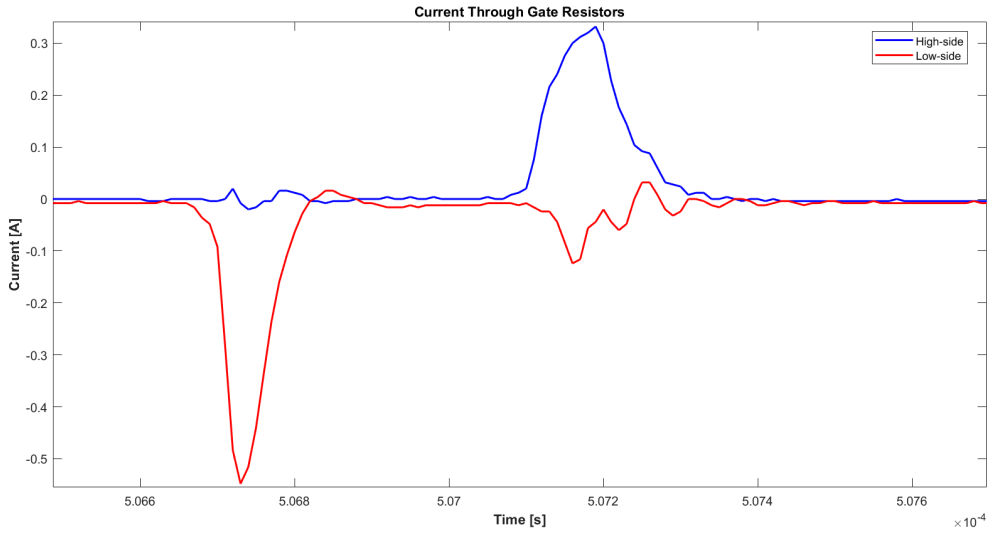

Figure 13: Gate-current, derived from recording 18, high-side switch turning ON. 10 Ω gate resistors.

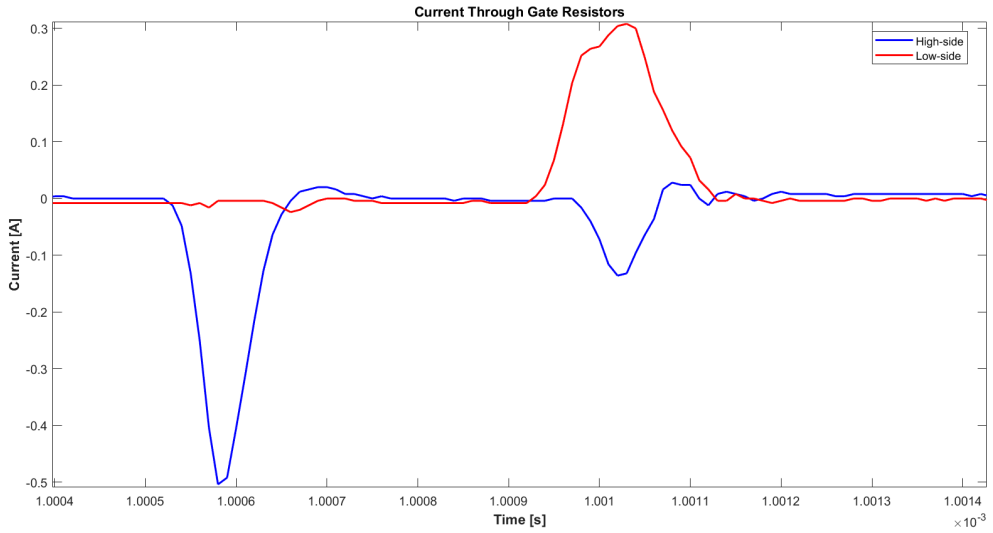

Figure 14: Gate-current, derived from recording 19, high-side switch turning OFF. 10 Ω gate resistors.

Table 5: Peak current and flow of charge into the gate for high-side and low-side turning on, for the case of 10 Ω gate resistors .

	Low-side	High-side	Expected Value
Peak Current	308 mA	332 mA	N/A
Flow of Charge	32.06 nC	35.5 nC	33 nC (typ turning on)

Comparing Table 3 (33 Ω) with Table 5 (10 Ω) we can see that using a smaller gate resistance increases the peak current, which is expected, but we do not see much change in the total charge delivered when opening. This is expected as the datasheet states a typical gate charge of 33nC to open the MOSFET, it would also imply a charge of 33nC is available when turning off the MOSFET [1]. Looking at Figures 9 and 10 (gate current 33 Ω) and Figures 13 and 14 (gate current 10 Ω) we also see that the time we deliver the charge is about the same for both configurations, at around 0.2µs. Using a smaller gate resistance has not shortened the time we deliver our charge, despite a higher peak current drawn. Looking at Table 2 & 4 we also see that the rise & fall times have been significantly affected by using smaller resistors, both of these values are however less than the deadtime, which is what we want. Had a larger gate resistance caused us to shorten our deadtime significantly, we would have needed to choose a smaller resistance to prevent shoot through. Considering that using a smaller gate resistance requires our gate drivers and power supply to be capable of delivering larger peak currents, and that we do not necessarily need, as well as providing surrounding circuitry protection should the MOSFET fail. We suggest using the larger gate resistance instead of the smaller one.

7.4 The Effect of the Switching Frequency

The effect of changing the switching frequency on the output voltage was measured according to the tests in section 6.6. Recordings 11, 12, 13, 14 and 15 are shown in Figures 15, 16, 17, 18 and 19 respectively.

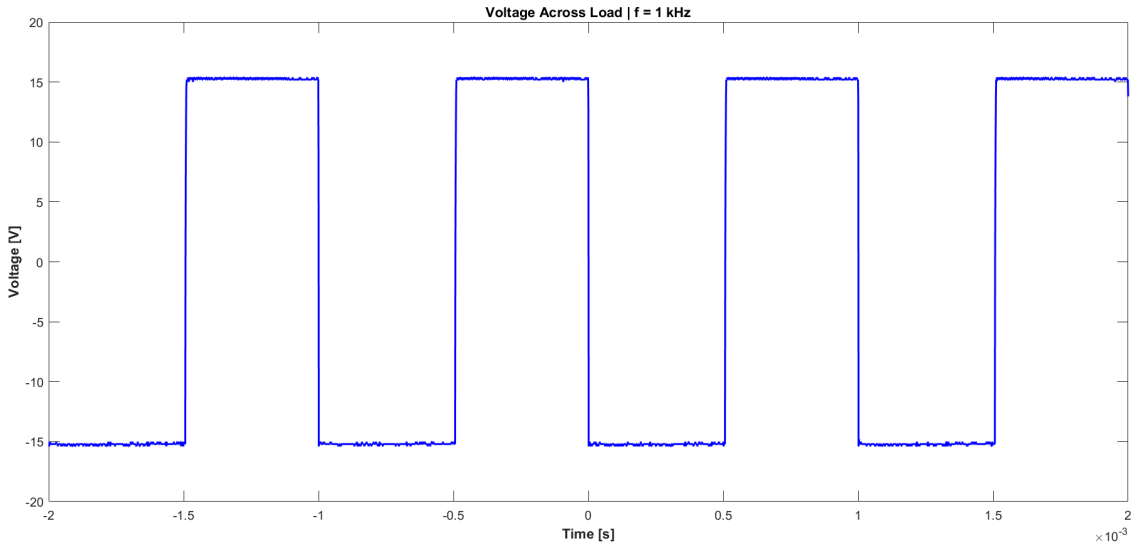

Figure 15: Recording 11, the output voltage for the case of 1 kHz operational frequency.

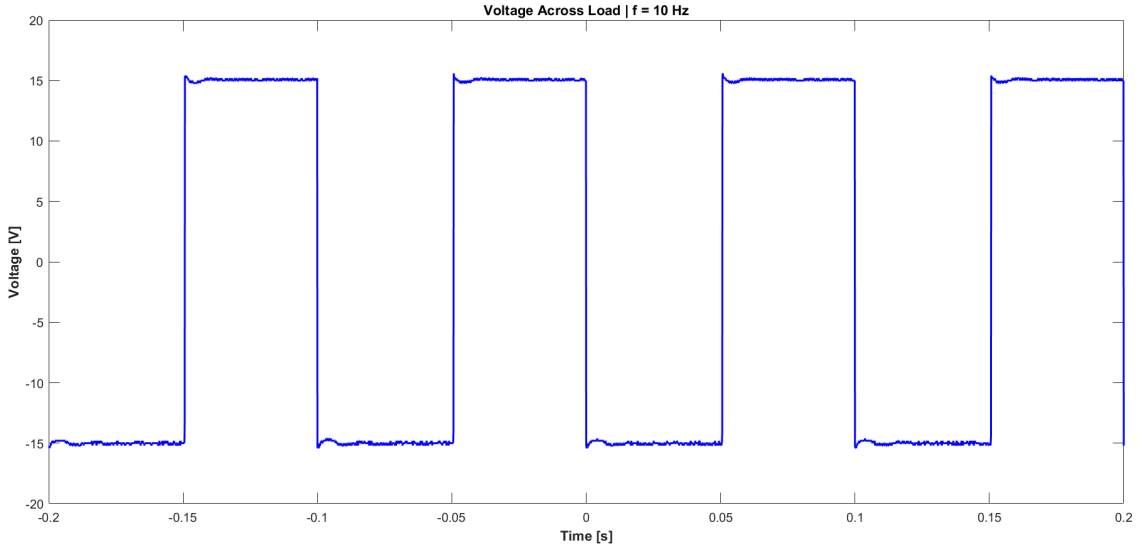

Figure 16: Recording 12, the output voltage for the case of 10 Hz operational frequency.

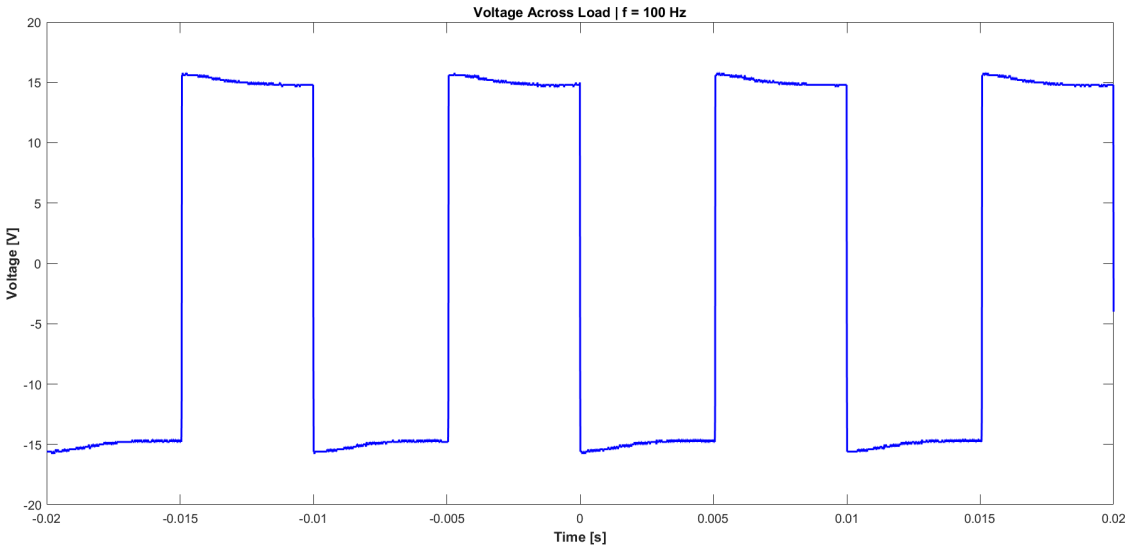

Figure 17: Recording 13, the output voltage for the case of 100 Hz operational frequency.

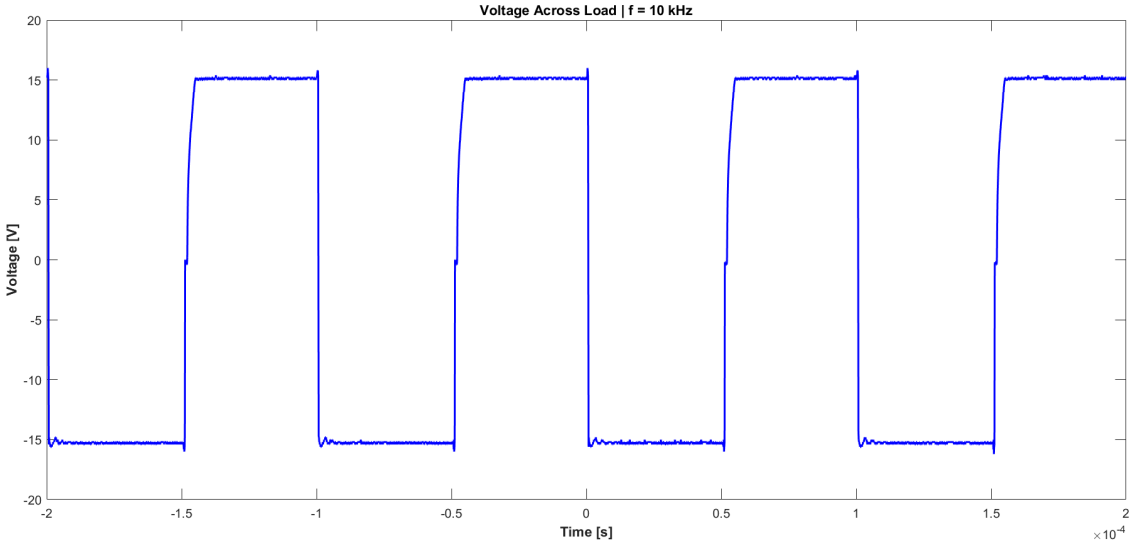

Figure 18: Recording 14, the output voltage for the case of 10 kHz operational frequency.

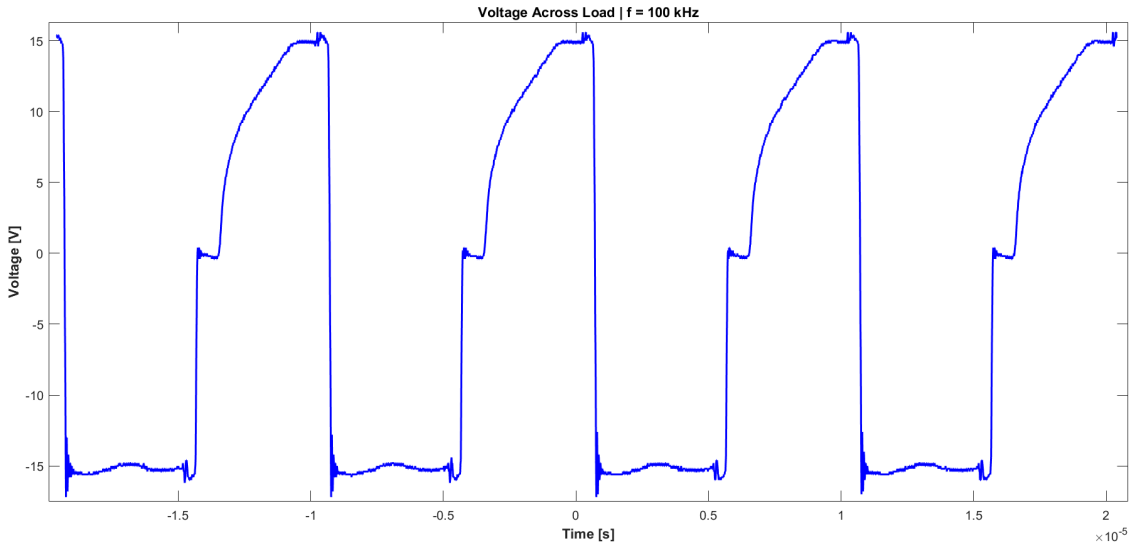

Figure 19: Recording 15, the output voltage for the case of 100 kHz operational frequency.

The output voltage waveforms shown in *Figure 15* (1 kHz), 16 (10 Hz), 17 (100 Hz) and 18 (10 kHz) looks as expected. There is a small gradient on the peak voltages in *Figure 17* (100 Hz), it is unclear why this occurs, it could possibly be some kind of resonance phenomena. For the case of 100 kHz, *Figure 19*, something strange happens, there is a lot of degradation and it reminds of an undervoltage-lockout situation or a voltage waveform with smaller periods than the slew rate for OP amps. In conclusion, it is unclear why this happens and further investigation would have to be performed to determine the cause. For the case of 10 Hz, *Figure 16*, the waveform seems quite unstable at the beginning of each switching state, the minimal operational frequency was calculated in section 3.3 to be 13Hz, since the waveform was operating at the threshold of the drivers UVLO it is reasonable to assume that this can cause instability.

The waveform in Figure 18 and 19 is asymmetric due to deviations in UVLO voltage level for the gate drivers. Variations in components contribute to triggering UVLO differently between the legs. This causes an asymmetrical waveform. This is discussed more in the following Section 7.5.

7.5 The Effect of the Undervoltage-Lockout Feature

The undervoltage-lockout feature of the half-bridge driver was measured according to the tests in section 6.7. For the case of using the original 1.0 µF bootstrap capacitor, undervoltage-lockout occurred at an operational frequency of 4.0 Hz, shown in *Figure 20*.

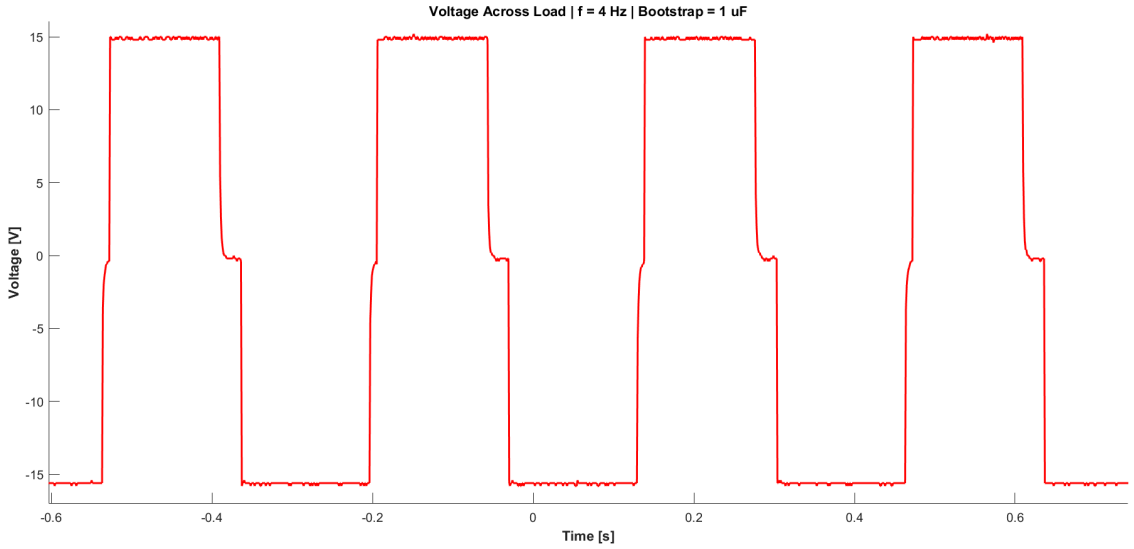

Figure 20: Recording 23, output voltage at undervoltage-lockout condition, 1.0 µF bootstrap capacitor.

For the case of using a smaller 0.1 µF bootstrap capacitor, undervoltage-lockout occurred at an operational frequency of 24 Hz, shown in *Figure 21*.

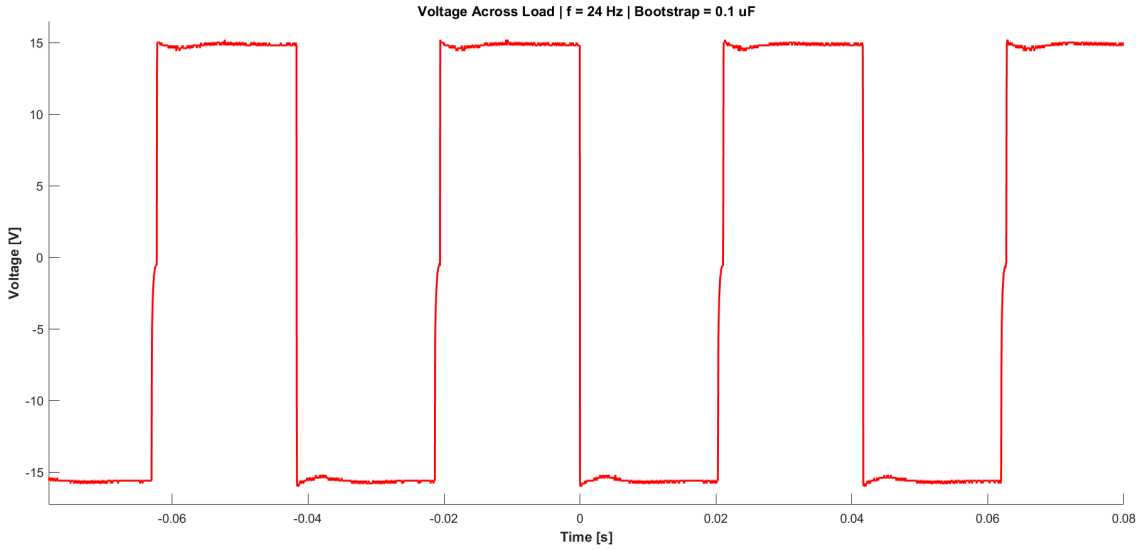

Figure 21: Recording 24, output voltage at undervoltage-lockout condition, 0.1 µF bootstrap capacitor.

As expected, UVLO occurs at a lower frequency for the larger bootstrap capacitor, since it can hold more charge than the smaller capacitor. An interesting thing happens in *Figure 21* is that UVLO

occurs at only one of the legs. This is most likely due to the tolerances of the capacitors and half-bridge drivers. If the frequency was further lowered, then UVLO would have occurred at both legs.

The next Figure shows the voltage level of the bootstrap capacitor (blue) when it enters into UVLO and the resulting output voltage (red).

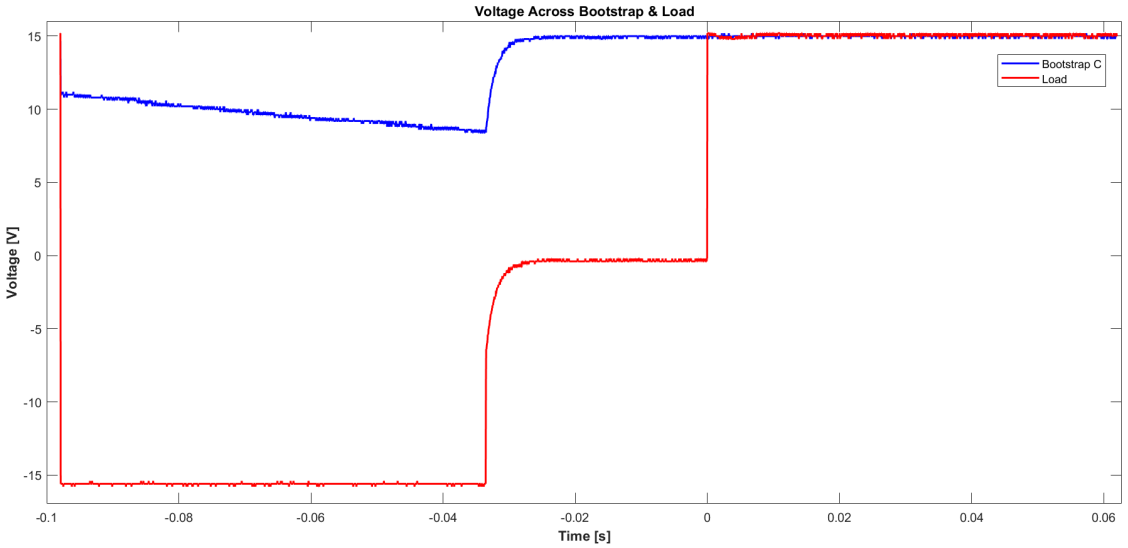

Figure 22: Recording 25, observing the undervoltage-lockout voltage.

The capacitor voltage hits UVLO at 8.4 V. According to the drivers datasheet, the gate driver has a UVLO between 8.0 V and 9.8 V with a typical value of 8.9 V. The value of 8.4 V is only for one of the gate drivers. The other gate driver most likely has a different UVLO level as we have seen asymmetrical clipping when testing UVLO.

8. Summary and Outlook

As part of the practical inverter lab, several key concepts were studied. Undervoltage lockout was looked at, and how changing the bootstrap capacitor changed at what frequency UVLO was triggered. Different capacitor types such as electrolytic and ceramic were also briefly discussed. The gate resistors were also studied, to see how a larger or smaller resistor value affected the current flow and the charge delivered when turning on the MOSFET. Rise & fall times for opening and closing MOSFETs were also looked at, the deadtime was compared to the datasheet of the gate driver.

This lab has been very useful to understand the process of designing a square-wave inverter. The undervoltage lockout feature was especially interesting to observe. Some waveforms that were recorded were however unexpected and difficult to explain. These waveforms are the rise & fall time recordings, where oscillations and unexpected rises in voltages occurred. The waveforms for the gate current, where there is current in the high-side gate when the low-side is opening, and vice versa. The slanting in the load voltages when at lower frequencies, as well as the clipping at higher frequencies were also difficult to explain. These are all topics which could be relevant for an extended study. A SPWM for the inverter could also be built for educational purposes, this requires only an arduino. By exchanging the logic signals, to be logic signals sent by the arduino, one could simulate a SPWM system through their computer.

9. Group Member’s Contributions

Abstract, section 6 - Elias Wallin

Section 1, 2, 5 and 8 - Adrian Gärde

Section 3 - Texas Gullström

Section 7 - Shared

References

[1] STP6NK60Z MOSFET, STMicroelectronics, Available at: https://www.st.com/resource/en/datasheet/stb6nk60z.pdf

[2] Application Note AN-968 “HV Floating MOS-Gate Driver ICs” Available at: https://www.infineon.com/dgdl/Infineon-HV_Floating_MOS_Gate_Drivers-ApplicationNotes-v01_00-EN.pdf?fileId=5546d4626c1f3dc3016c47de609d140a

[3] Half-bridge driver IR2183, International Rectifier, Available at: http://infineon.com/dgdl/Infineon-IR2183-DataSheet-v01_01-EN.pdf?fileId=5546d462533600a4015355c9490e16d1

[4] UF4004 Diode, Available at: https://www.vishay.com/docs/88755/uf4001.pdf

Appendix

Appendix A: MATLAB Figure Export Script

```
% Access the data fields
dataset = A0003;
time = dataset.time * 1e6; % Time vector
voltage_ch1 = dataset.ch1; % Voltage from channel 1
voltage_ch2 = dataset.ch2; % Voltage from channel 2

% Plot the results
Figure;
plot(time, voltage_ch1, 'b', 'LineWidth', 1.5, 'DisplayName', 'High-side');
hold on;
plot(time, voltage_ch2, 'r', 'LineWidth', 1.5, 'DisplayName', 'Low-side');
hold off;
xlim([0 1.5]); %If Figure is not moved after
title('Voltage Across High-side & Low-side');
xlabel('Time [µs]', 'FontWeight', 'bold');
ylabel('Voltage [V]', 'FontWeight', 'bold');
legend('Location', 'best');
fontsize(gcf, 18, "points");
set(gca, 'LooseInset', max(get(gca, 'TightInset'), 0.02)); % Reduce padding
```

Appendix B: MATLAB Script for deadtime Calculation

```
%% example script for plotting LO and HO of the gate driver
%  for the case that A0001.ch1 was LO (going from low to high)
%   and A0001.ch2 was HO (going from high to low)
% Note: You might need to adjust the FontSize and LineWidth for your purpose
% Settings for export format (Word -> SVG, LaTeX -> PDF)
% comment out the non-intended "target":
target = 'Word';
%target = 'LaTeX';
% assign variable names
v_LO = A0027.ch1; % in V
v_HO = A0027.ch2; % in V
time = A0027S.time*1e6; % in µs
% before plotting, we find the flanks and rise/fall time
% HO-flank
V_HO_max = max(v_HO);
V_HO_min = min(v_HO);
[~,idx_HO_50] = min(abs(v_HO - 0.5*(V_HO_max-V_HO_min)));
t_HO_flank = time(idx_HO_50); % time when v_HO is ca 50%
% get HO falltime (90% to 10%)
idx_HO_90 = idx_HO_50;
while v_HO(idx_HO_90) < 0.9*V_HO_max
   idx_HO_90 = idx_HO_90 - 1;
end
idx_HO_10 = idx_HO_50;
```

```
while v_HO(idx_HO_10) > 0.1*V_HO_max
   idx_HO_10 = idx_HO_10 + 1;
end
HO_falltime = 1e3*(time(idx_HO_10)-time(idx_HO_90)); % in ns
% get error in ns due to sampling
HO_falltime_error = (1e3*(time(idx_HO_10+1)-time(idx_HO_90-1)) -
HO_falltime)/2;
disp(['HO fall-time: (',num2str(HO_falltime), char(177),
num2str(HO_falltime_error),') ns']);
% LO-flank
V_LO_max = max(v_LO);
V_LO_min = min(v_LO);
[~,idx_LO_50] = min(abs(v_LO - 0.5*(V_LO_max-V_LO_min)));
t_LO_flank = time(idx_LO_50); % time when v_LO is at 50%
% get LO risetime (10% to 90%)
idx_LO_90 = idx_LO_50;
while v_LO(idx_LO_90) < 0.9*V_LO_max
   idx_LO_90 = idx_LO_90 + 1;
end
idx_LO_10 = idx_LO_50;
while v_LO(idx_LO_10) > 0.1*V_LO_max
   idx_LO_10 = idx_LO_10 - 1;
end
LO_risetime = 1e3*(time(idx_LO_90)-time(idx_LO_10)); % in ns
% get error in ns due to sampling
LO_risetime_error = (1e3*(time(idx_LO_90+1)-time(idx_LO_10-1)) -
LO_risetime)/2;
disp(['LO rise-time: (',num2str(LO_risetime), char(177),
num2str(LO_risetime_error),') ns']);
% also we determine the deadtime
% get time when v_HO is 99% of asymptotic value
v_HO_asym = mean(v_HO(time < time(idx_HO_90)-10e-3*HO_falltime));
idx_HO_99 = idx_HO_90;
while v_HO(idx_HO_99) < 0.99*v_HO_asym
   idx_HO_99 = idx_HO_99 - 1;
end
% get time when v_LO is 1% of LO_max
idx_LO_01 = idx_LO_10;
while v_LO(idx_LO_01) > 0.01*V_LO_max
   idx_LO_01 = idx_LO_01 - 1;
end
deadtime = 1e3*(time(idx_LO_01)-time(idx_HO_99)); % in ns
% get error in ns due to sampling
deadtime_error = (1e3*(time(idx_LO_01+1)-time(idx_HO_99-1)) - deadtime)/2;
disp(['deadtime: (',num2str(deadtime), char(177), num2str(deadtime_error),')
ns']);
%% create (empty) Figure 1
h1 = Figure(1);
% plot LO
plot(time,v_LO,'b',LineWidth=1.5);
hold on
% plot HO
plot(time,v_HO,'r',LineWidth=1.5);
```

```
hold on
% mark 90% of HO
plot(time(idx_HO_90),v_HO(idx_HO_90),'or',MarkerSize=8);
hold on
% mark 10% of HO
plot(time(idx_HO_10),v_HO(idx_HO_10),'or',MarkerSize=8);
hold on
% mark 90% of LO
plot(time(idx_LO_90),v_LO(idx_LO_90),'ob',MarkerSize=8);
hold on
% mark 10% of LO
plot(time(idx_LO_10),v_LO(idx_LO_10),'ob',MarkerSize=8);
hold on
% mark location, when HO goes low
plot(time(idx_HO_99).*[1 1],V_HO_max.*[-0.05 1.05],':r',LineWidth=1);
hold on
% mark location, when LO goes high
plot(time(idx_LO_01).*[1 1],V_LO_max.*[-0.05 1.05],':b',LineWidth=1);
hold off
fontsize(gcf,12,"points");  % Set general fontsize to 12
xlim([0 1.2]); % adjust time period for the "interesting part"
xlabel('Time [µs]',FontSize=14,FontWeight='bold');    % Increase xlabel
fontsize
ylabel('Voltage [V]',FontSize=14,FontWeight='bold');  % Increase ylabel
fontsize
% add legend with waveform names in LaTeX encoding (and increased fontsize)
legend({'$v_{LO}(t)$','$v_{HO}(t)$'},Interpreter="latex",
Location="best",FontSize=14);
%% save the modified Figure in SVG or PDF format
export_filename = ['Figure_',num2str(h1.Number),'_export_',
char(datetime('now','Format', 'yyyy-MM-dd_HH-mm-ss'))];
set(gca, 'LooseInset', [0,0,0,0]);  % remove white space
if strcmp(target,'Word')
   % save the modified Figure in SVG format (for Microsoft Word)
   print(h1,'-vector','-dsvg',[export_filename,'.svg']);
end
if strcmp(target,'LaTeX')
   % save the modified Figure in PDF format (for LaTeX)
   set(h1,'PaperUnits','Centimeters');
   set(h1,'Units','Centimeters');
   pos = get(h1,'Position');
   set(h1,'PaperPositionMode','Manual','PaperUnits','Centimeters',
'PaperSize',[pos(3),pos(4)]);
   print(h1,'-vector','-dpdf','-bestfit',[export_filename,'.pdf']);
   % To remove the white space around the Figure uncomment the following
line:
   %pdf_crop([export_filename,'.pdf']);
end
```