TI MCU with graphics interface

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Industrial Systems

AM261 – uLED/display driver

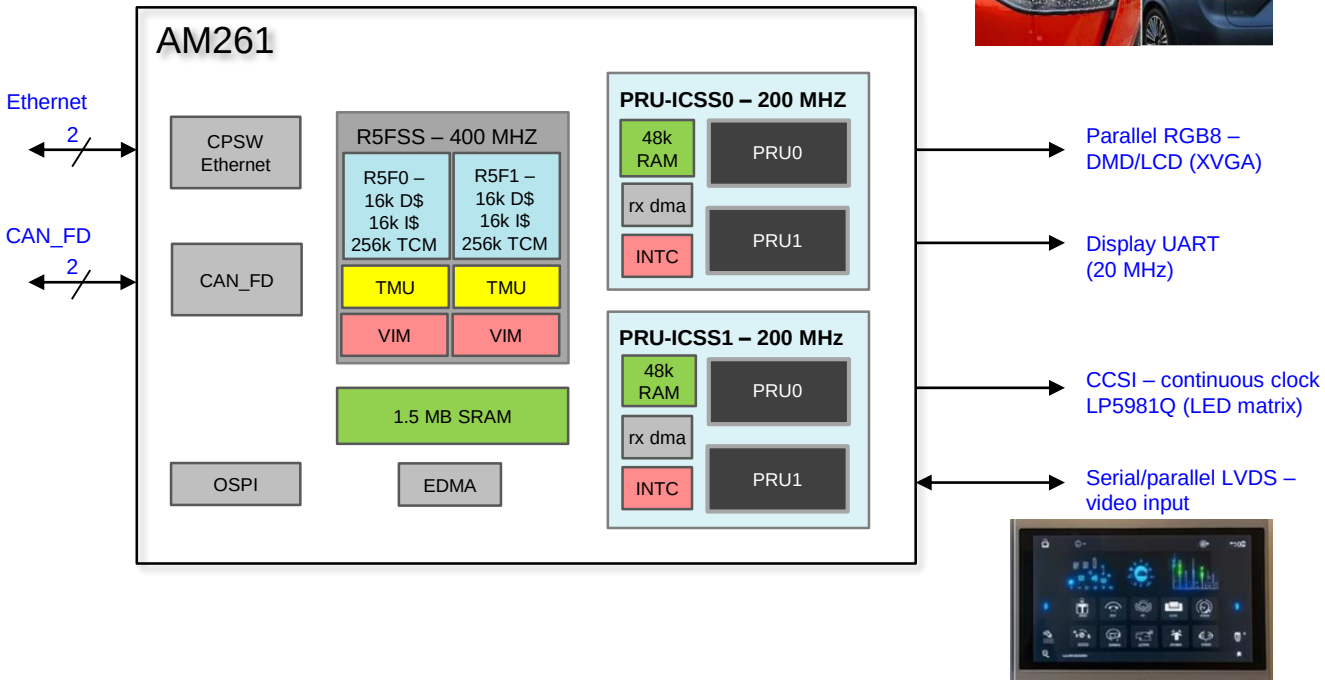
Target application
- Automotive lighting
- Industrial displays

Output Interfaces:
- Parallel LCD/RGB24
- Display UART (25 MHz)
- CCSI – continuous clock SPI

Compute: (interface + image proc)
- 2 x 400 MHz R5F
- 4 x 200 MHz PRU

Input Interface:
- CAN_FD
- Ethernet (10/100/1G TX/T1)
- Serial/parallel LVDS RGB format

Robustness:
- ASIL-B
- Cyber security



LCD interface with parallel RGB24

Example: NHD-4.3-800480CF-ASXP-CTP (800 x 480 @ 60 Hz, 24 bpp color)

Timing:

NEWHAVEN DISPLAY INTERNATIONAL

Timing Characteristics - TFT

Parallel RGB Input Timing Requirements

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	28.2	29.2	40	MHz	-
DLCK Period		Tclk	25	34	-	ns	-
HSYNC	Period Time	Th	908	928	1088	DCLK	Thw + Thbp = 88 DLCK is fixed
	Display Period	Thdisp		800		DCLK	
	Pulse Width	Thw	1	48	87	DCLK	
	Back Porch	Thbp	87	40	1	DCLK	
	Front Porch	Thfp	20	40	200	DCLK	-
VSYNC	Period Time	Tv	517	525	613	H	Tvw + Tvbp = 32 H is fixed
	Display Period	Tvdisp		480		H	
	Pulse Width	Tvw	1	1	3	H	
	Back Porch	Tvbp	31	31	29	H	
	Front Porch	Tvfp	5	13	101	H	-

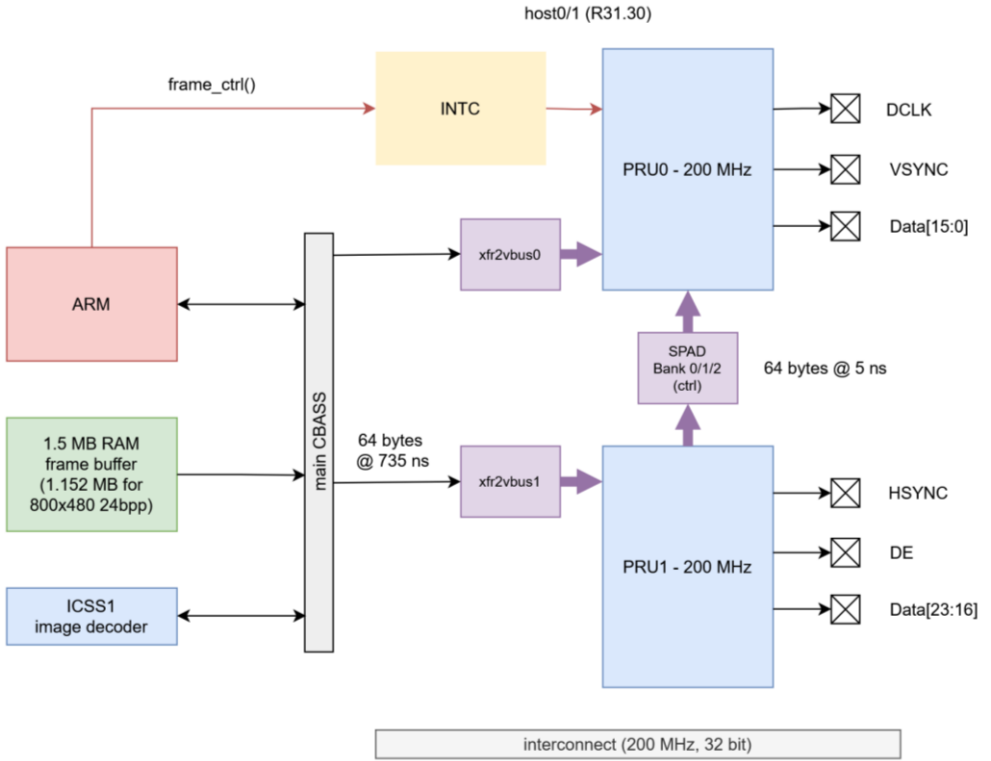
PRU architecture for RGB24 interface

Frame Buffer
- 800 x 480 x 24 bits = 1.152 Mbytes
- On-chip SRAM, < 100 ns read latency

DMA
- xfr2vbus read DMA in 64 byte auto increment mode, reads every 735 ns
- Direct broadside read into PRU register
- Non blocking single cycle read for 64 bytes

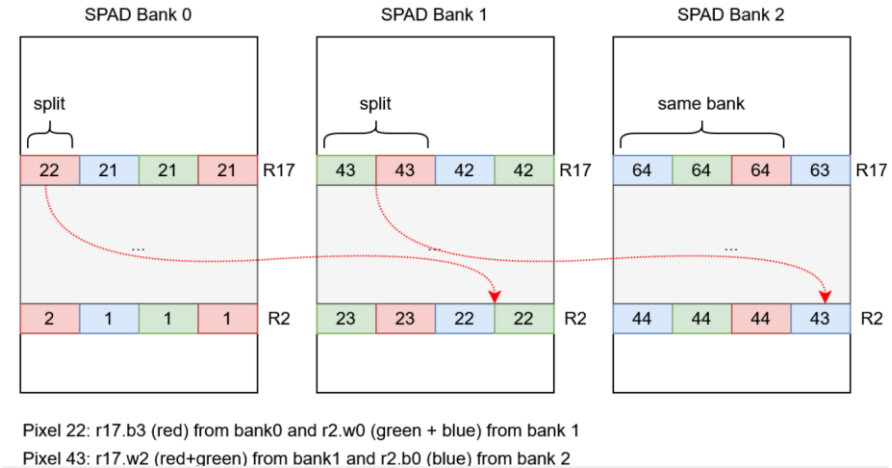
Output Interface
- 2 x PRU @ 200 MHz in direct GPO mode
- 30 PRU GPOs split across two PRO cores
- PRU cores run in sync – same clock cycle
- LUT for blue color bit mapping (EVM limitation)
- Shift for green color bit mapping (EVM limitation)

Output Timing:
- 35 ns DCLK based on 5 ns PRU cycle time – 7 cycles
- HSYNC: 40 + 800 + 40 + 48 DCLK
- VSYNC: 31 + 480 +13 +1 HSYNC
- 10 ns setup and hold time (8 ns in LCD spec)



Line size vs DMA transfer size alignment

- One Line is stored in sequential memory location: 800 pixel + 24 bit = 1200 bytes.
- DMA from frame buffer to register bank is 64 bytes at a time which is not and integer multiple for pixels and line size.
- First DMA has 22 pixel for red color and 21 pixel for green and blue color. Pixel 22 is split into two dma transfers
- 800 pixel line ends at a half 64 byte DMA
- Macros for sending even and odd line which are repeated 240 time -> 480 lines.



Pin Mapping with AM243x Launchpad

- Red Data: continuous bits and byte aligned
- Green Data: continuous bits no alignment
- Blue Data: no bit and no byte alignment
- DE: PRU0 GPO as critical setup and hold time
- DCLK: PRU0 GPO as critical setup and hold time
- VSYNC: low latency PWM in init mode
- HSYNC: PRU1 GPO
- DSIP: system GPIO

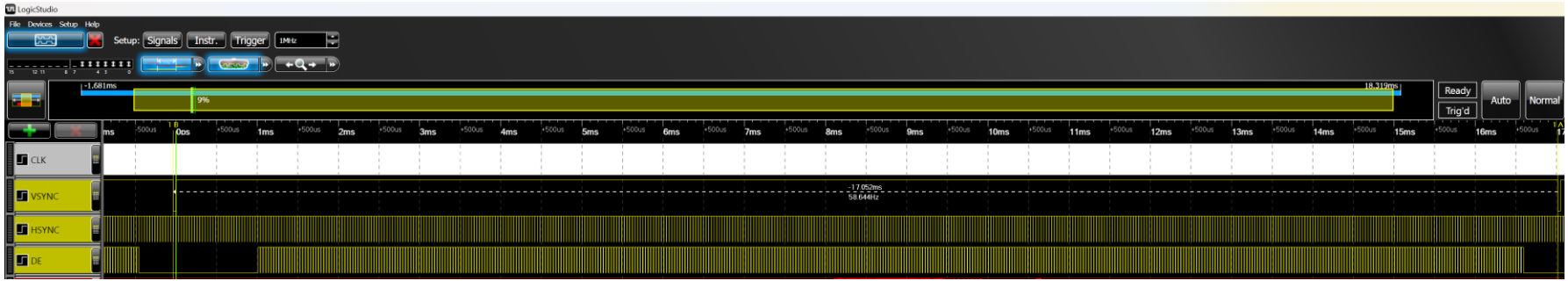
Note: dedicated/customer hardware should use color bits bit aligned and byte aligned to free up PRU cycles for LUT and shift operation!

Function	PRU0	LP
R0	0	BP.33
R1	1	BP.32
R2	2	BP.31
R3	3	BP.19
R4	4	BP.17
R5	5	BP.13
R6	6	BP.48
R7	7	BP.44
CLK	8	BP.51
G0	11	BP.43
G1	12	BP.05
G2	13	BP.15
G3	14	BP.14
G4	15	BP.12
G5	16	BP.07
G6	17	BP.18
G7	18	BP.8
DE	19	BP.45

Function	**PRU1**	**LP**
B0	0	BP.11
B1	1	BP.67
B2	2	BP.68
B3	6	BP.69
B4	11	BP.70
B5	12	BP.72
B6	13	BP.71
B7	15	BP.59
HSYNC	16	BP.57
Function	GPIO	LP
VSYNC	PRG0_PWM2_A0	BP.40
DISP	GPIO1_41	BP.51

Timing from PRU – RGB24 interface (VSYNC/HSYNC)

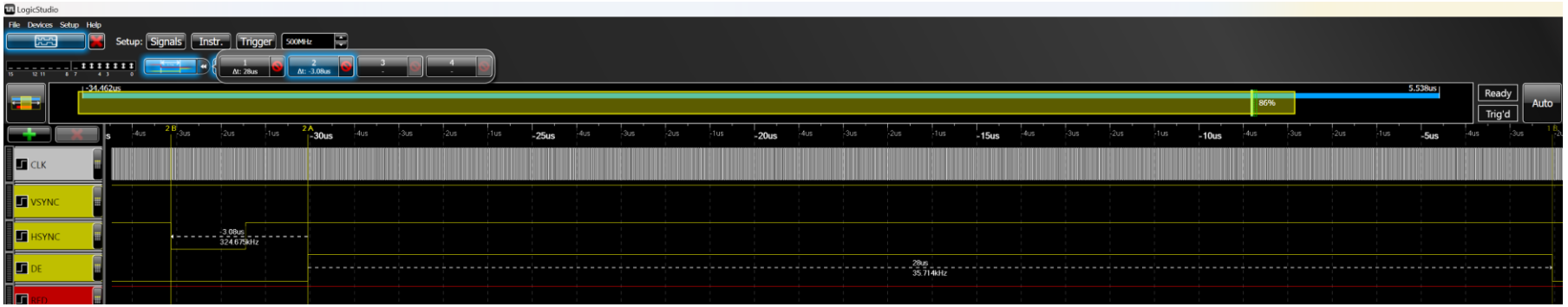
VSYNC period: 17.052 ms = 928 * 525 * 35 ns



HSYNC period: 32.480 us = 928 * 35 ns

Timing from PRU – RGB24 interface (DCLK/DE/RGB)

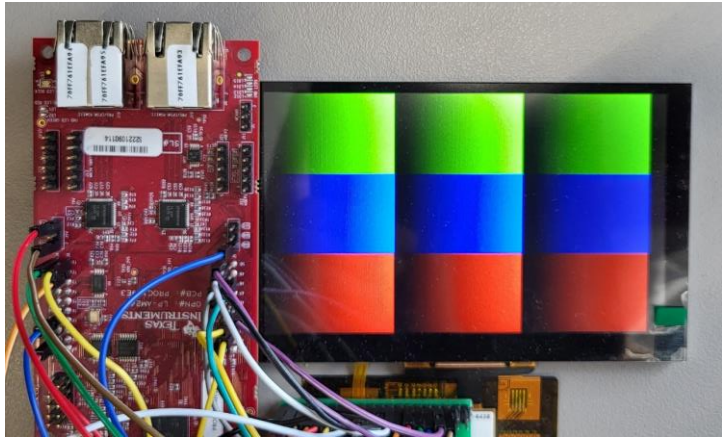
HSYNC BACK PORCH + SYNC: 3.08 us = (48 + 40) * 35 ns DE: 28.0 us = 800 * 35 ns

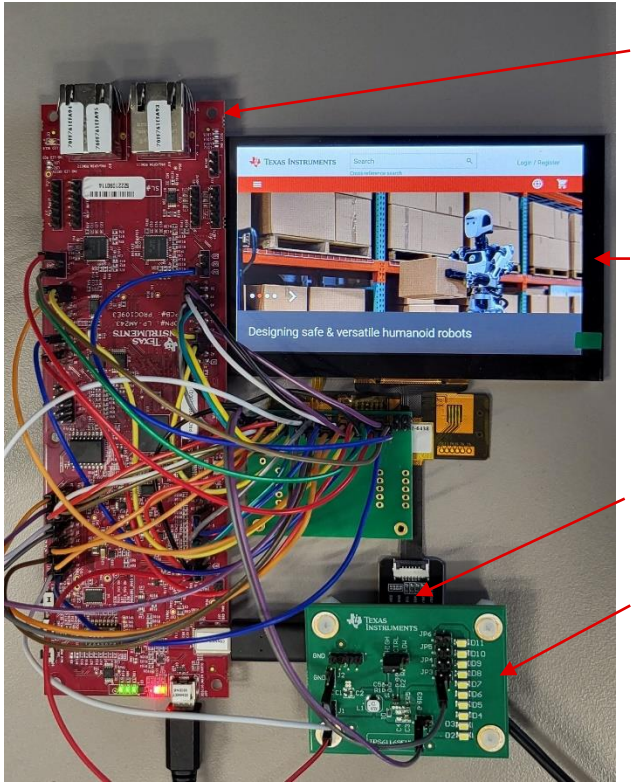


DCLK period: 35 ns (140 ns for 4 x DCLK)
DE setup time: 20 ns
DE hold time: 15 ns

Demo (ICSS_M IP with 200 MHz)

- CCS Project with ARM driver and PRU firmware
- Image download via CCS memory load
- Test image generation with RTU_PRU (used to detect correct color mapping)
- Optional diming using PWM signal to back-light control





AM243 LP

NHD-4.3-800480CF
-ASXP-CTP
(800 x 480, RGB24)

I2C Capacitive
Touch interface

TPS61169 EVM
40 mA backlight
Controller
(R5 = 5.1 Ohm)

Customization and Boundaries

AM261/AM263 (ICSS_M IP@200 MHz)

- Max DCLK = 30 ns – 6 cycles (800 x 600 @ 60fps)
- DCLK period 5ns steps: 30ns , 35 ns, 40 ns, ….
- Max resolution: 800 x 600 @ 24 bpp = 1.44 Mbytes SRAM

AM243/AM64 (ICSS_G IP @ 333 MHz)

- MAX DCLK = 18 ns – 6 cycles (1280 x 720 @ 60 fps)
- DCLK period in 3/3.3/4/4.14/5 ns steps (various PRU clocks)
- Max resolution: 1280 x 720 @ 16 bpp = 1.84 Mbytes SRAM more colors and frame buffers through external RAM.

Customization Guideline:

1. Understand resolution, frame rata and colors
2. Map to DCLK and memory boundaries of given device.
3. Optional LVDS conversion with external bridge device.