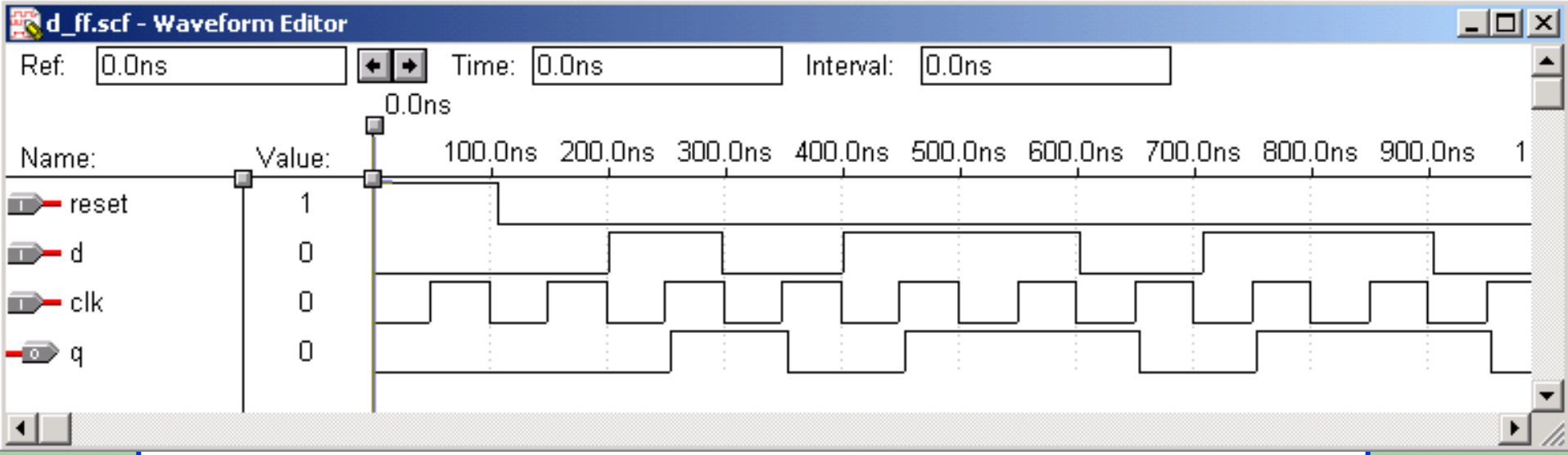
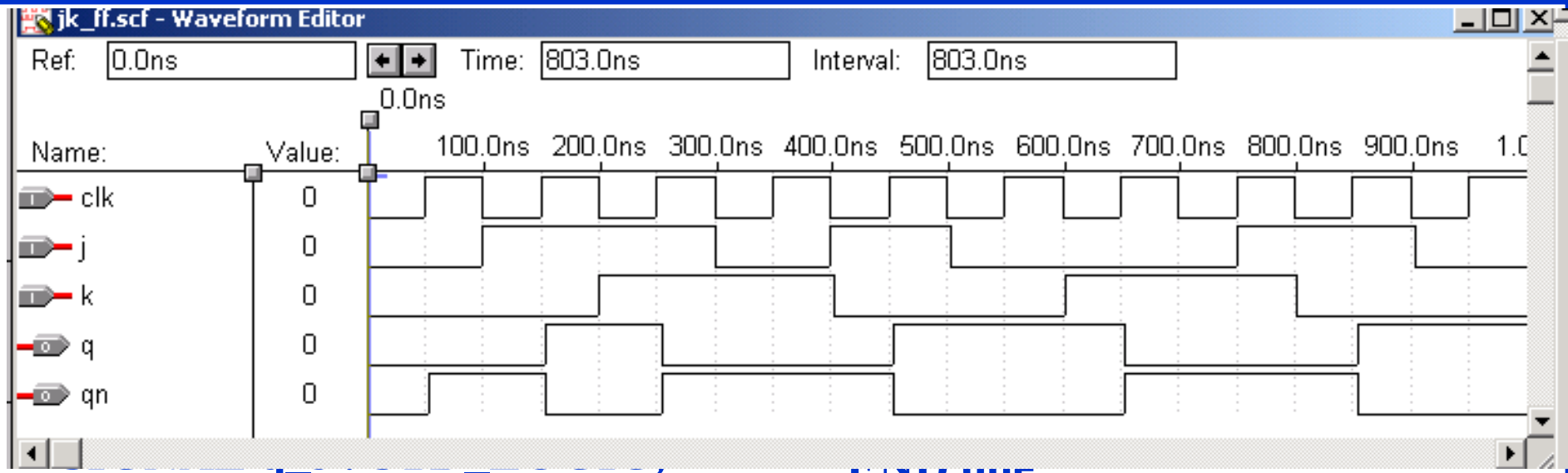
4.5 触发器的VHDL描述及其仿真

[例4.5.1] 同步D触发器的VHDL描述和仿真




```
        PROCESS (clk)
          BEGIN
          IF clk'EVENT AND clk='1' THEN
              IF reset='1' THEN
          Q<='0';
          ELSE q<=d;
        END IF;
        END IF;
    END PROCESS;
END one;
```

[例4.5.2] 边沿JK触发器的VHDL描述和仿真




```
BEGIN
    PROCESS (j,k,clk)
        BEGIN
        IF clk'EVENT AND clk='1' THEN
        IF J='0'  AND k='0' THEN
        q_s<= q_s;
        ELSIF J='0'  AND  k='1' THEN
        q_s<='0';
        ELSIF J='1'  AND  k='0' THEN
        q_s<='1';
```