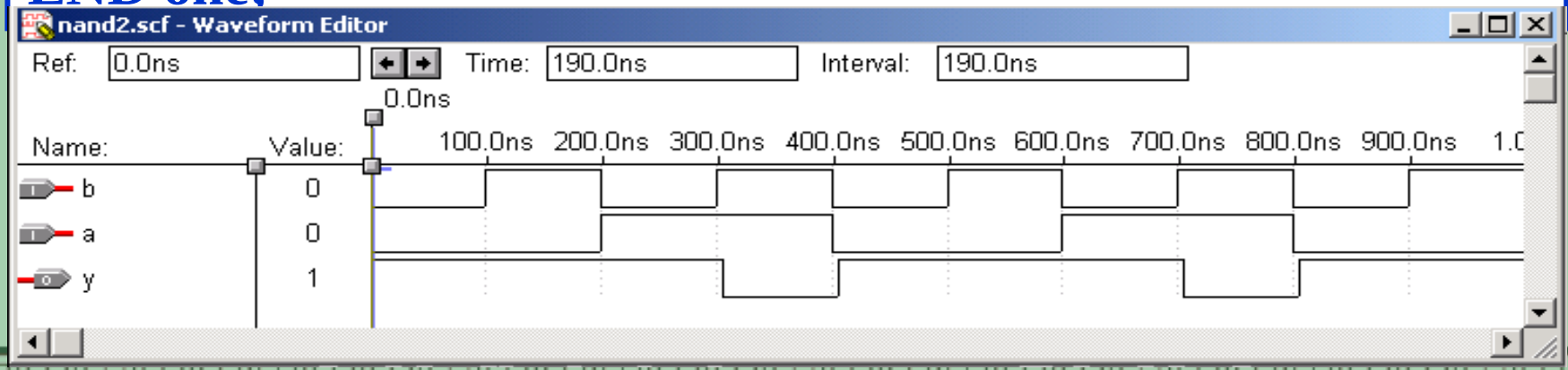
# 2.5 门电路的 VHDL 描述及其仿真

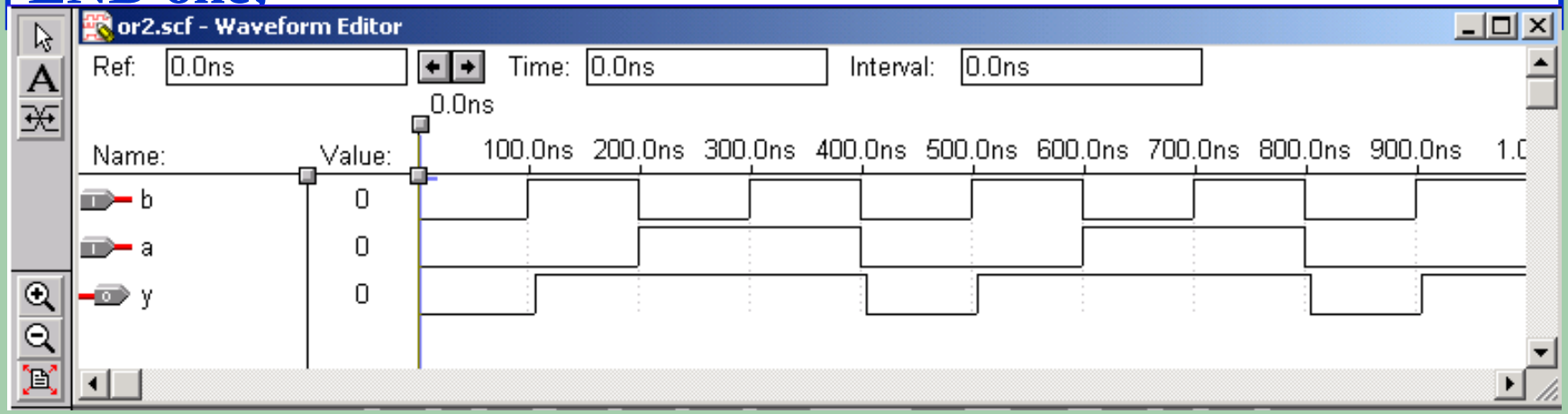
## [例2.5.1] 2输入与非门的 VHDL 描述及仿真

```
LIBRARY IEEE;
    USE IEEE.STD_LOGIC_1164.ALL;
    ENTITY nand2 IS
    PORT(a, b : IN  STD_LOGIC;
            y: OUT STD_LOGIC);
    END nand2;
    ARCHITECTURE one OF nand2 IS
    BEGIN
        y<= a nand b;
END one;
```



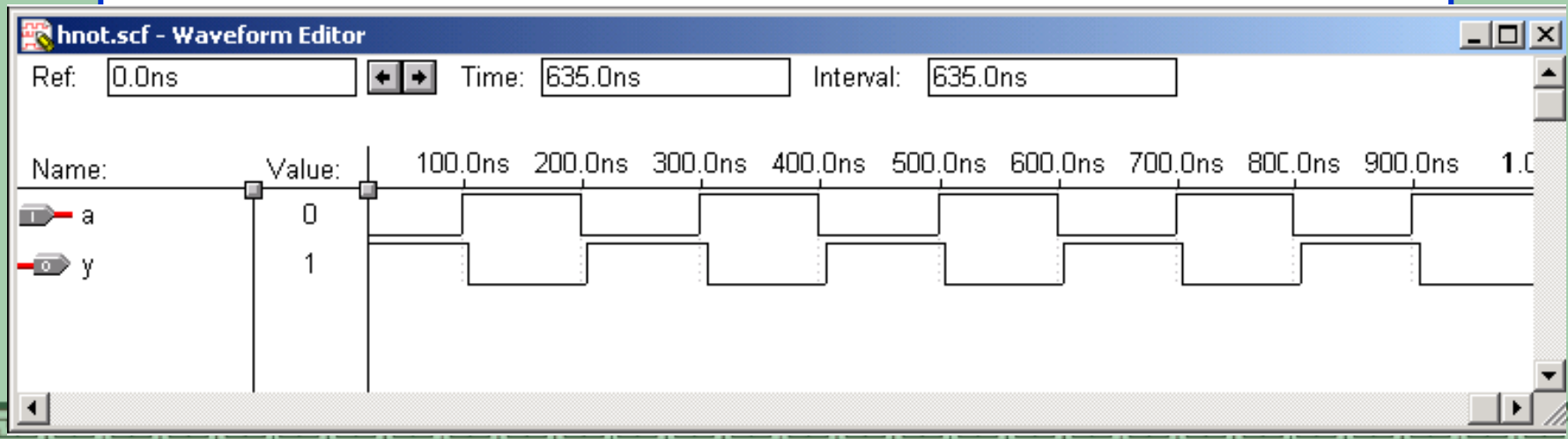
# [例 2 .5 .2 ] 2 输入或门的 VHDL 描述及仿真

```
LIBRARY IEEE;
    USE IEEE.STD_LOGIC_1164.ALL;
    ENTITY or2 IS
    PORT(a, b : IN  STD_LOGIC;
            y: OUT STD_LOGIC);
    END or2;
    ARCHITECTURE one OF or2 IS
    BEGIN
        y<= a or b;
END one;
```



# [例 2 .5 .3 ] 非门的 VHDL 描述及仿真

```
LIBRARY IEEE;
    USE IEEE.STD_LOGIC_1164.ALL;
    ENTITY hnot IS
    PORT(a : IN  STD_LOGIC;
           y: OUT STD_LOGIC);
    END hnot;
    ARCHITECTURE one OF hnot IS
    BEGIN
        y<= not a;
END one;
```



# [例 2 .5 .4 ] 异或门的 VHDL 描述及仿真

```
LIBRARY IEEE;
    USE IEEE.STD_LOGIC_1164.ALL;
    ENTITY xor2 IS
    PORT(a, b : IN  STD_LOGIC;
              y: OUT STD_LOGIC);
    END xor2;
    ARCHITECTURE one OF xor2 IS
    BEGIN
        y<= a xor b;
END one;
```