
Technology of Microelectronic- Important values

An Open-Source Summary

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1 First Chapter

Positive etch mask = exposed area will be removed. Negative vice versa.

| Wafer Size | Thickness |
|------------|-------------------|
| 4" | 400 μm |
| 8-12" | 1.2 mm |

1.1 Silicon properties

Cheap and strong, fragile. Resistivity $0.001 - 20 \text{ k}\Omega/\text{cm}$. Can be SCS, poly or amorphous. Can deform without cracking for quite some time.

\sim having into 1 direction 10^5 atoms that aren't $>$ a 1cm
 $\bullet 10^{15}/\text{cm}^3 \rightarrow 10^5/\text{cm} = 10/\mu\text{m}$ (!)
 $\bullet 1\text{cm} = 10^8\text{\AA}$
 $1\text{\AA} = 0,1\text{ nm}$

| Dopant level | Designation | Dopant concentration (cm^{-3}) | Resistivity n/p (ohm-cm) |
|--------------------|------------------|---|--------------------------|
| Very lightly doped | n^{--}, p^{--} | $<10^{14}$ | $>100/>30$ |
| Lightly doped | n^-, p^- | $10^{14}-10^{16}$ | $1-100/0.3-30$ |
| Moderately doped | n, p | $10^{16}-10^{18}$ | $0.03-1/0.02-0.3$ |
| highly doped | n^+, p^+ | $10^{18}-10^{19}$ | $0.01-0.03/0.005-0.02$ |
| Very highly doped | n^{++}, p^{++} | 10^{19} | $0.001 < 0.01/0.005$ |

Figure 1: Resistivity

In a Si cube we have 8 atoms inside the cell. with:

$$\text{Volume} = (.543\text{nm})^3 \quad \frac{8}{\text{Volume}} = 5 \cdot 10^{22} \text{atoms/cm}^3$$

SCS has a purity up to 11 nines ! and is 2 FCC lattices displaced by .25, .25, .25.

1.2 Boule making

To create a Boule we can use a Czochralski pulling at 1420C. The pull rate is around **mm/min**. 30 hours for 2m + 30 hours for cooling!

1.2.1 Wafer treatment

First we have to cut then to get a perfect wafer we will have:

1. Lapping: $20\mu\text{m}/\text{side}$
2. Edge profiling: makes edge cleaner
3. Etching (chemical): $20\mu\text{m}/\text{side}$

4. Polishing (CMP): $25\mu\text{m}/\text{side}$

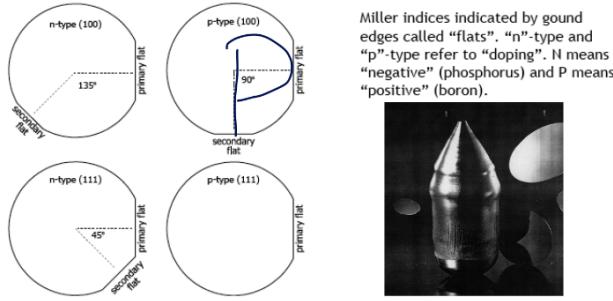


Figure 2: For fully doped wafer

A boat can contain between 12 to 24 wafer.

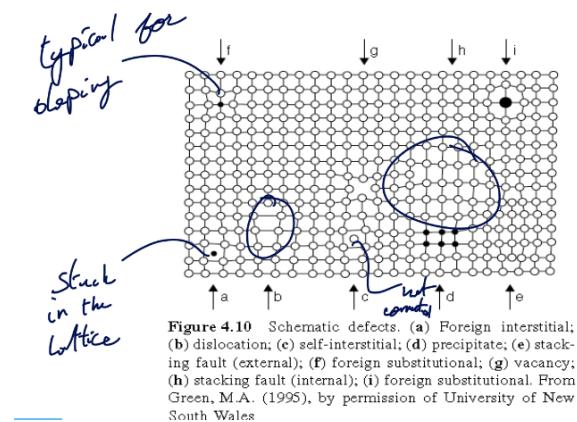


Figure 3: Source of non-idealities

We drop some die on the chips that aren't good due to a defect. Lower defect ratio allows to put bigger transistor. But going smaller isn't always the best as the interconnect cost can quickly ramp up as we go too small. So optimization process between Packaging and reliability (yield).

| Class | 1 | 10 | 100 | 1000 | 10 000 |
|-----------------------------------|----|-----|------|--------|---------|
| No. of particles $0.5\mu\text{m}$ | 1 | 10 | 100 | 1000 | 10 000 |
| No. of particles $0.1\mu\text{m}$ | 35 | 350 | 3500 | 35 000 | 350 000 |

| | $0.1\mu\text{m}$ | $0.2\mu\text{m}$ | $0.3\mu\text{m}$ | $0.5\mu\text{m}$ | $1\mu\text{m}$ | $5\mu\text{m}$ |
|-------------|------------------|------------------|------------------|------------------|----------------|----------------|
| ISO class 1 | 10 | 2 | | | | |
| ISO class 2 | 100 | 24 | 10 | 4 | | |
| ISO class 3 | 1000 | 237 | 102 | 35 | 8 | |
| ISO class 4 | 10 000 | 2370 | 1020 | 352 | 83 | |
| ISO class 5 | 100 000 | 23 700 | 10 200 | 3520 | 832 | 29 |

Figure 4: ISO classification

| ISO Class | FS209 Class | Certification Particle Size (μm) | | | | | |
|-----------|-------------|---|---------|---------|------------|-----------|---------|
| | | 0.1 | 0.2 | 0.3 | 0.5 | 1.0 | 5.0 |
| 1 | --- | 10 | 2 | --- | --- | --- | --- |
| 2 | --- | 100 | 24 | 10 | 4 | --- | --- |
| 3 | 1 | 1,000 | 237 | 102 | 35 | 8 | --- |
| 4 | 10 | 10,000 | 2,370 | 1,020 | 352 | 83 | --- |
| 5 | 100 | 100,000 | 23,700 | 10,200 | 3,520 | 832 | 29 |
| 6 | 1,000 | 1,000,000 | 237,000 | 102,000 | 35,200 | 8,320 | 293 |
| 7 | 10,000 | --- | --- | --- | 352,000 | 83,200 | 2,930 |
| 8 | 100,000 | --- | --- | --- | 3,520,00 | 832,000 | 29,300 |
| 9 | --- | --- | --- | --- | 35,200,000 | 8,320,000 | 293,000 |

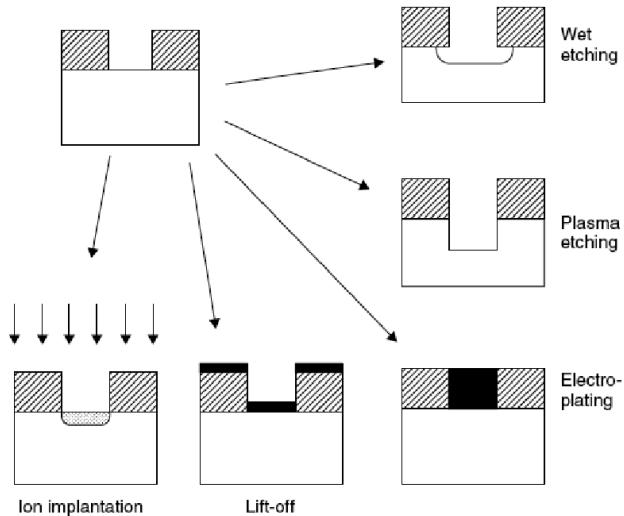
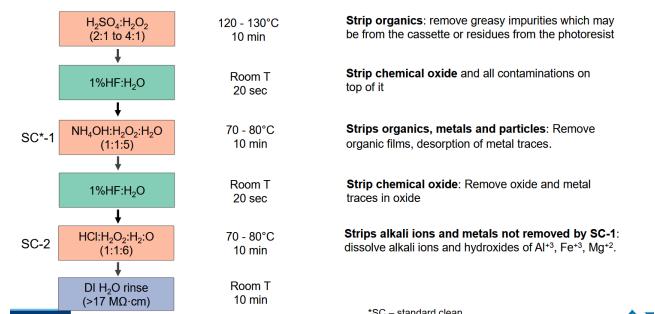
! watch : how are microchips made

Figure 5: ISO and FS209

Class ISO:

- 10,000: PCB, packaging
- 1,000: MEMS, packaging, HDD
- 100: MEMS, RF/Photonic ICs
- 10: IC

2 Lithography

**Figure 6:** Various type of etching**Figure 7:** RCA clean sequence

After this we can apply some HMDS to remove the OH group at the top of the wafer to make the photoresist sticks better. We must also apply some anti-reflective coating to avoid the UV light to strike unwanted area.

2.1 Resist spinning

We drop a little bit of the photoresist and then spin it faster to make it a nice and even coat:

$$T = \frac{KC^\beta \eta^\gamma}{\omega^\alpha}$$

The thickness is $0.05 - 100\mu m$. The thickness varies due to step on the wafer (previously deposited material).

| Start time (sec) | Duration (sec) | rpm | Dispense | Comments |
|------------------|----------------|------|----------------|--------------------------------|
| 0 | 0 | 0 | — | Load wafer |
| 0 | 2 | 1000 | N ₂ | Blow off wafer |
| 2 | 10 | 500 | HMDS spray | Apply primer |
| 12 | 10 | 3000 | — | Spin-dry primer |
| 22 | 1 | 0 | — | Allow wafer to stop spinning |
| 23 | 3 | 0 | Resist | Dispense resist and let spread |
| 26 | 5 | 500 | — | Spread resist |
| 31 | 20 | 3000 | — | Spin resist |
| 51 | 0 | 0 | — | Unload wafer |

Figure 8: Takes around a minute to apply resist

We can also use some *spray coating* to spray and rinse through a nozzle. The step coverage is better and more uniform. There is also dip coating and laminating while they are less used in this industry.

After this we usually do some soft baking to improve resolution. If too long we may decompose the resist watch out !

- few mins at 100C
- 30 mins in a convection oven

2.2 Optic

PSM is a prime example to improve resolution. With ARC we also trap some lights in the resist creative some over exposed and ripple in the sidewalls.

So we usually bake PEB to improve the sidewalls ripple ! We use some OPC to correct and get the desired shape that may looks different on the mask. Usually we print on a metal on chrome mask using an e-beam. Either we use a master mask and directly use it to print on the wafer or we first use the master mask to create a larger mask with multiple master mask print on it. Reduction by **4 to 5** times reduction from mask to wafer !!!

3 types of printing

1. Contact printing: Mask is touching the wafer

- Better resolution (less diffraction)
- Mask wear and wafer damage

2. Proximity printing: not touching this time
 - Lower resolution
 - Better mask lifetime
3. Project printing: uses a set of lenses to focus on the mask and then on the wafer
 - Expensive technique but best of both

2.3 Mask and formulas

The most important metrics are:

- **Critical Dimension:** $CD = k_1 \frac{\lambda}{NA}$
- **Numerical Aperture:** $NA = n \sin(\theta)$
- **Depth of Focus:** $DOF = k_2 \lambda / NA^2$ where $k_2 < 1$

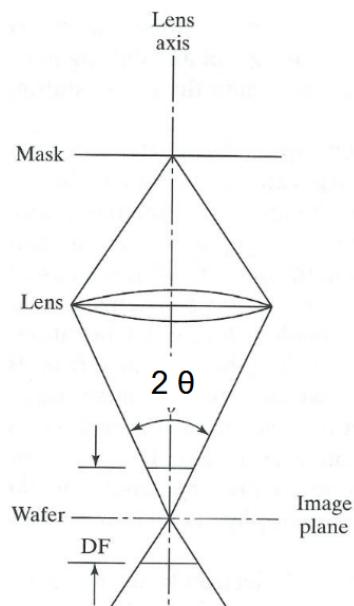


Figure 9: Lens

So clearly, we can see why having a small wavelength matters to get better precision. To improve again we can use a wider θ .

With the DOF, some part could be in focus while other not which is really problematic. We can't have a nice and uniform resolution accross multiple lengths.

2.4 Lights

| Source | Wavelength (nm) | Name |
|------------------------------|---|-----------------------------------|
| Hg arc lamp | 436 (blue) 405 (violet) 365 (UV) 248 | g-line h-line i-line DUV |
| KrF excimer laser | 248 | DUV |
| ArF excimer laser | 193 | DUV |
| F ₂ excimer laser | 157 | DUV (vacuum UV) |
| plasma | 13 | EUV (long x-ray) |

Figure 10: Important lights value

2.5 Double patterning

We can use two mask to get virtually smaller features by combining those two together.

- LELE: reduces k_1 , double the cost since double patterning. Overlay issue :((
- SADP: self aligning. Simply use dummy fill then add THICKKK sidewalls, etch it a lil, remove dummy and boom 2 pattern for the price of 1.
- LFLE: based on a freezing process.
- SAQP: close to SADP but pitches less than 38nm

2.6 EUV

We can't use lenses anymore. **7 mirrors with 70% reflection per mirror!** No pellicles that are EUV transparent yet.

To tune the linewidth we can change the exposure and development time.

For etching:

- wet etching: using acetone, IPA, water rinse. 2% NaOH for positive resists
- plasma etching: O₂ plasma

3 Deposition

- Vaporize a target material onto the substrate - 0.1 – 1 nm/s
- 1. Thermal evaporation
 - Heat up a Tungsten filament that holds the target material
 - Heat up the target
 - Only for low melting point material and will have some parasitic from crucible
- 2. Electron beam evaporation
 - Use electron source to hit the target material
 - Cooling the crucible to avoid parasitic particle
 - Good for high melting point material
- 3. Sputtering - 1 – 10 nm/s

Figure 11: Slide of presentation

| Method | Description | Pros ✓ | Cons X |
|-----------------|--|---|--|
| Atmospheric | Roll the wafer in with some ozone and TEOS gas | Simple and fast growth rate | Low temperature |
| Low Pressure | Same as APCVD but wafer rolls in their boat and under a vacuum | Large scale, better result than APCVD and EPCVD | Slow growth rate, higher temperature |
| Plasma Enhanced | Same principle as before but use RF to generate Plasma | High deposition rate, low temperature, good step coverage | More complex, plasma can induce damage |

Figure 12: CVD

| Method | Description | Pros ✓ | Cons X |
|-----------------|---|---|---|
| Electroplating | Simple, use an anode and cathode (wafer) to deposit Cu, Ni, Au, ... | Simple and fast growth rate - 0.1 – $10 \mu\text{m}/\text{min}$ | Can be a bit rough → use Damascene process |
| Electroless | Like Electroplating but without a DC current | No DC, conformal coating | Slow growth rate- $100 \text{ nm}/\text{min}$, need to replace often the bath's solution |
| Spin on Glasses | Spin coating to deposit silicon-based dielectric film | Re-use of equipment, conformal coating - 50 – 100 mm | Softer film, higher defect, shrinkage while curing, ... |

Figure 13: Liquid Phase deposition

| Method | Description | Pros ✓ | Cons X | Accuracy |
|--------------------|---|---|---|----------------------------------|
| Needle measurement | Using a small needle, measure the thickness | Simple and good for PCB | Scratch the surface, low accuracy | $\frac{1}{2} \mu\text{m}$ |
| Reflectometry | Measure vertically (normal). Top surface and substrate reflects and interfere | Compact equipment | Less accurate for thin films, only 1 layer, no polarization information | $10 \text{ nm} - 50 \mu\text{m}$ |
| Ellipsometry | Like reflectometry but on the side. Quantize amplitude ratio and phase difference | Good for thin films, multi-layer stacks and precise | More complex and expensive setup | $< 100 \mu\text{m}$ |

Figure 14: Measurements

4 Oxidation, wet, dry

SiO₂ is forming a *tetrahedral arrangement*. Can create some amorphous structure too. The quality is determined based on the ratio of bridging to non-bridging elements.

In elec, we use some amorphous.

| Spec | Value |
|----------------------------------|---------------------------|
| density | $2 - 2.3 \text{ gm/cm}^3$ |
| ε_r | 3.9 |
| reflection index n | 1.5 |
| Breakdown field | 10^7 V/cm |
| Trap/defect density at interface | 10^{11} cm^{-2} |

4.1 Thermal oxidation

Natural growth of a oxide exposed to air and enhanced by temperature. Useful for:

- 1) implant/diffusion mask
- 2) surface passivation
- 3) isolation between transistors
- 4) key component of MOS structures
- 5) dielectric for multilevel interconnect
- 6) cleaning

This grows in both way but slightly more outwards (**54/46**). SiO₂ is 2.2 times larger than Si. Dry thermal is slower but better than wet oxidation. Dry has a higher breakdown voltage $\rightarrow 5 - 10 \text{ MV/cm}$ so really good for gate oxide (since they are getting smaller and smaller)!

For $.5\mu\text{m}$ @ 1200C :

- Dry: 6 hours
- Wet: 1 hour

We can have some interface issue as the step is not exactly the same and so the development won't be equal. Can use color to determine the thickness:

| Thickness (μm) | Color |
|-----------------------------|--------------|
| 0.07 | Brown |
| 0.31 | Blue |
| 0.39 | Yellow |
| 0.41 | Light orange |
| 0.47 | Violet |

4.2 LOCOS

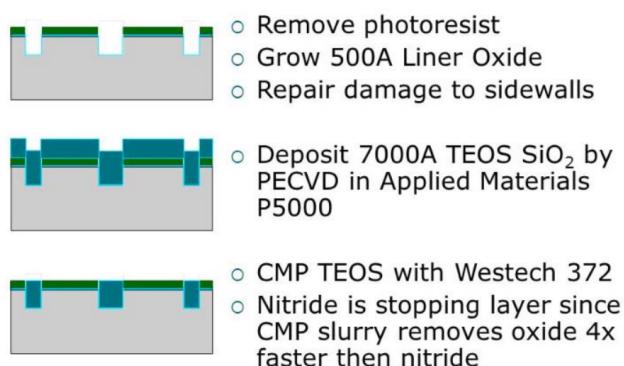
To have some isolation between transistor. Reduces topography by 56%. use some Nitrite which has a higher thermal expansion than Si. Add padoxide as stress release.

- Si₃N₄: 100 – 200nm
- SiO₂: padoxide: 20 – 30nm

Wet oxi creating bird beak and then removing those oxide.

4.3 STI

Use CVD for the oxidation and CMP of the oxide avoids bird's beak and mechanical stress.

**Figure 15:** STI process

Better precision, the width drawn is the actual width. We also use some dry oxidation which makes it better for large drive current.

4.4 Doping

We use either:

- gas, coating or ion implementation

4.4.1 Diffusion Theory

We have a diffusion *flux* of *impurities* in one dimension. (We are always using x as the vertical direction of diffusion).

$$F = -D \frac{\partial C(x, t)}{\partial x} \quad D = D_0 \exp\left(\frac{-E_\alpha}{kT}\right)$$

We have D that is the *diffusion coefficient* in cm^2/s . C is the dopant concentration per unit volume. We have D_0 that is the diffusion coefficient in cm^2/s at infinite temperature and E_α is the activation energy in eV.

At low concentrations of dopant in silicon ($10^{12} - 10^{16} \text{ cm}^{-3}$) can be seen as constant. With this simplification, we can easily solve the equation, we also see that gold, copper, ... have high diffusion coefficient which is why we tend to avoid such metal in the clean room.

If we do not have a source or sink of the impurity, we know that the *change in impurity concentration with time must equal the local decrease of diffusion flux*:

$$\frac{\partial C}{\partial t} = -\frac{\partial F}{\partial x} = \frac{\partial}{\partial x} \left(D \frac{\partial C(x, t)}{\partial x} \right) \quad \frac{\partial C}{\partial t} = D \frac{\partial^2 C(x, t)}{\partial x^2} \text{ if } D \text{ cst}$$

There are 2 methods of diffusion:

1. Constant-surface-concentration: using vapor, we have a constant concentration of dopants at the surface.
2. Constant-total-dopant: thin layer, we have constant amount of impurity at the surface.

4.4.2 Constant-surface-concentration

$$\text{Init: } C(x, 0) = 0$$

$$C(0, t) = Cs$$

$$C(\infty, t) = 0$$

$$C(x, t) = Cs \operatorname{erfc} \left(\frac{x}{2\sqrt{Dt}} \right) \quad \operatorname{erfc}(z) = 1 - \operatorname{erf}(z) \quad \operatorname{erf}(z) = \frac{2}{\sqrt{\pi}} \int_0^z e^{-y^2} dy$$

We have \sqrt{Dt} that is called the *diffusion length* in cm. The total number of dopant atoms per unit area that has diffused into the semiconductor is given by:

$$Q(t) = \int_0^\infty C(x, t) dx = \frac{2}{\sqrt{\pi}} Cs \sqrt{Dt} \approx 1.13 Cs \sqrt{Dt}$$

4.4.3 Constant-total-dopant

$$C(x, 0) = 0 \quad \int_0^\infty C(x, t) dx = \phi$$

$$C(\infty, t) = 0$$

$$C(x, t) = \frac{\phi}{\sqrt{\pi Dt}} \exp \left(-\frac{x^2}{4Dt} \right)$$

Where ϕ is the *total amount of dopant* per unit area. So the surface concentration ($x = 0$) is $\phi / \sqrt{\pi Dt}$.

We usually use those two methods and we call this a *two step diffusion process*. a pre-deposition diffused layer is first formed using constant-surface-concentration condition. Then a drive-in (or redistribution) diffusion is used using constant-total-dopant condition.

For most practical cases the diffusion length for the pre-deposition stage is much smaller than the diffusion length of the drive-in diffusion. This allows to make deep junctions, e.g. for wells for CMOS.

| <u>approximate table</u> | | | |
|--------------------------|-----------------------------------|---|--------------------------|
| Dopant level | Designation | Dopant concentration (cm^{-3}) | Resistivity n/p (ohm-cm) |
| Very lightly doped | n ⁻ , p ⁻ | <10 ¹⁴ | >100/>30 |
| Lightly doped | n ⁺ , p ⁺ | 10 ¹⁴ -10 ¹⁶ | 1-100/0.3-30 |
| Moderately doped | n, p | 10 ¹⁶ -10 ¹⁸ | 0.03-1/0.02-0.3 |
| highly doped | n ⁺ , p ⁺ | 10 ¹⁸ -10 ¹⁹ | 0.01-0.03/0.005-0.02 |
| Very highly doped | n ⁺⁺ , p ⁺⁺ | 10 ¹⁹ | 0.001 < 0.01/0.005 |


 $A = w \cdot t$
 $R = (\rho / t)(L / w) = \rho_s (L / w)$
 $\rho_s = \rho / t$ [ohm/m]


 $R = \rho L / t$
 $\rho = \rho_s (L / w)$
 $\rho_s = q (H_n n + H_p p)$ (L / w) = number of squares resistors
△ mr

Figure 16: Resistivity vs Doping

We also need a minimum mask width to be able to absorb all those ions in the doping process.

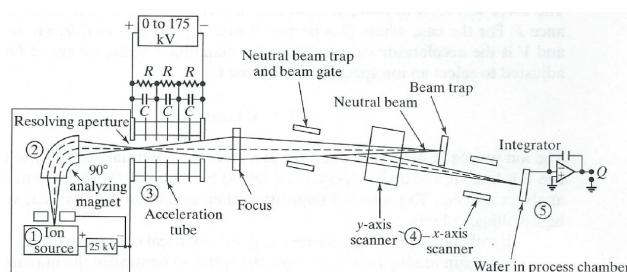


Figure 17: Ion Implanter

4.5 Ion Implantation

The source is at around $25kV$ and the high voltage accelerator goes above $> 5MeV$. There will be some undercut as the path traveled inside won't be straight and it will bounce. So the depth is a gaussian. Can have special behavior where the ion travels all the way through the lattice without bouncing.

$$N(x) = N_p \exp\left(-\frac{(x - R_p)^2}{2\Delta R_p^2}\right) \quad N_p = \frac{\phi}{\sqrt{2\pi}\Delta R_p}$$

ΔR_p being the *projected straggle* distance from the peak with concentration reduced by 40%.

Need some **rapid annealing** to repeat the lattice after, will spread out the concentration sadly.

5 Etching, wet, dry, plasma, DRIE

Wet etching is cheaper **10k** while dry etching is **1M**. But wet etching is mostly isotropic meaning it goes into all direction which leads to a lot of undercut.

Wet etching is quite simple using a bath and a quick dump to stop precisely the etching and using some nozzle to stop any reaction. This limits the feature size as too close gaps can be bridged during the process $< 3\mu m$. We use **HF** for **SiO₂** **WATCH OUT** it will get through your skin without any pain but starts attacking your bones after.

5.1 Anisotropic

It has a preferred lattice orientation that will be etched faster. Dry etching is a combination of temperature and vacuum.

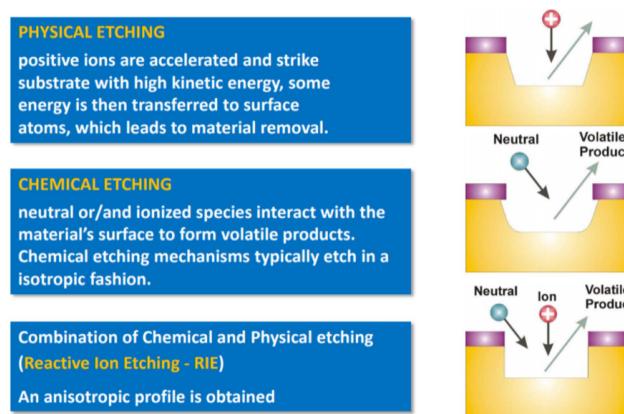
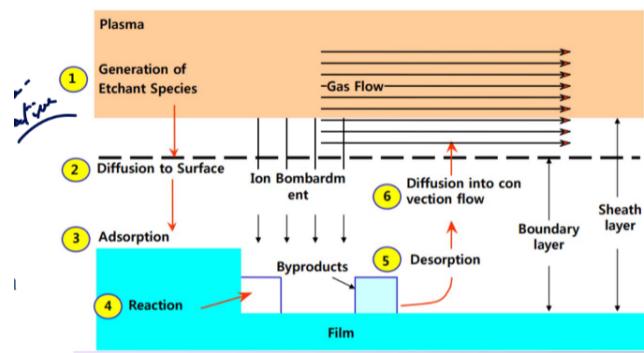


Figure 18: Main type of Dry Etching

5.1.1 Plasma Etching

Same amount of positive and negative charges but a different number of unionized molecules. Large electric field applied to a gas up to the **breakdown of the gas**.

**Figure 19:** 6 steps of Plasma Etching

Needs **high kinetic energy and chemical reactions**. There are about 10^{15} cm^{-3} neutral species and $10^8 - 10^{12} \text{ cm}^{-3}$. Ions go on the surface and strike it to remove some molecules.

| TABLE 2.3 Etching Pressure Ranges | |
|-----------------------------------|-------------------|
| Etching Mode | Pressure (Torr) |
| Ion Milling | $10^{-4}-10^{-3}$ |
| Reactive Ion Etching/Ion Milling | $10^{-3}-10^{-1}$ |
| Plasma Etching | $10^{-1}-5$ |

Figure 20: Pressure: PE = Isotropic Chemical Etching

RIE will create a DC bias to accelerate the ions and add some extra kinetic energy towards the substrate. This is a combination of **chemical and sputter etching**. The chemical is purely isotropic and with little electrical damage while the sputtering is anisotropic and slower (this is ion milling).

| | Plasma Etching | | Reactive Etching | | Physical Etching | |
|---|----------------------|---------------------------------|--------------------------------|-----------------------------|--------------------------------|-----------------------------|
| | Barrel Reactor | Planar Reactor | Ion | Ion Beam | Sputtering | Ion Beam Milling |
| Substrate Location | Surrounded by plasma | On grounded electrode in plasma | On powered electrode in plasma | In beam, remote from plasma | On powered electrode in plasma | In beam, remote from plasma |
| Pressure (torr) | $10^{-1} \sim 1$ | $10^{-1} \sim 1$ | $10^{-2} \sim 10^{-1}$ | $10^{-4} \sim 10^{-3}$ | $10^{-5} \sim 10^{-3}$ | 10^{-4} |
| Ion energy(eV) | 0 | $1 \sim 100$ | $100 \sim 1000$ | $100 \sim 1000$ | $100 \sim 1000$ | $100 \sim 1000$ |
| Active Species | Atoms, Radicals | Atoms, radicals, reactive ions | Radicals, reactive ions | Reactive ions | Ar^+ ions | Ar^+ ions |
| Products | Volatile | Volatile | Volatile | Volatile | Nonvolatile | Nonvolatile |
| Mechanism | Chemical | Chemical/Chemical-Physical | Chemical/Physical | Chemical/Physical | Physical | Physical |
| Etch Profile | Isotropic | Isotropic/Anisotropic | Isotropic/Anisotropic | Anisotropic | Anisotropic | Anisotropic |
| Selectivity | $30 : 1 - 10 : 1$ | $10 : 1 - 5 : 1$ | $30 : 1 - 5 : 1$ | $10 : 1 - 3 : 1$ | $1 : 1$ | $1 : 1$ |
| Resist Compatibility | Excellent | Excellent | Good | Good | Poor | Poor |
| Device Damage | Little | Little | Some possible | Some possible | Very possible | Very possible |
| Etch Rate ($\mu\text{m}/\text{min}$) | $0.1 \sim 0.5$ | $0.1 \sim 0.5$ | $0.05 \sim 0.1$ | $0.05 \sim 0.1$ | $0.02 \sim 0.05$ | $0.02 \sim 0.05$ |
| Resolution ($\mu\text{m}/\text{min}$) | 3 | 2 | $1 \sim 2$ | $1 \sim 2$ | $0.5 \sim 1$ | $0.5 \sim 1$ |

Ref: J. D. Lee, "Silicon Integrated Circuit microfabrication technology," 2nd edition

Figure 21: RIE possibilities

RIE is a sophisticated and complex process where changing a single parameters could impact the total chain of the reaction leading to issues.

5.1.2 DRIE

With this method we can obtain an **aspect ratio of 20-50** and the etch rate is around $> 10 \mu\text{m}/\text{min}$.

6 Interconnect

Aluminium has a fairly low melting point at around $577C$. The interconnect and contact Al is done during the same step. But Al has the tendency to fall into the crevices left by the Si that diffuses inside the Al. So add 1% of Si in Al or use barrier material like TiW.

We want to further reduce the contact resistance so we must employ some alloy mixed with Si. We are using the fact that Si diffuses into the metal so then we can remove the non-reacted metal and boom we got some nice salicide.

6.1 Electromigration

If the track is not made thick enough, the electrons can take with them some bits of the material and move them further. Creating gaps and increasing the resistance. One solution is to add 4% copper to the mix making the interconnect Al-Cu-Si, 95-4-1.

6.2 Interconnect

For stack up layer we may be misaligned so we must make the via wider each time as we go up or add some offset.

After making an interconnect we tend to planarize to have a fresh and flat surface to work on. So we will use some CMP process to make everything smooth. Damascene process is based on this idea.

We may need to add some dummy fill oxide to ensure a global planarity after the CMP. Or another technique is using some *reverse tone litho* and already pre-etch oxides that are on top of other stuff and are too wide.

But at some point, Al is not fast enough, too much delay for a small feature size. We had to go for Copper even though it has a high diffusivity. Issue with adhesion, ...

So we have to add a **seed layer** to avoid this diffusion. This seed layer is a thin conductive layer and then we can put the big chunk of copper.

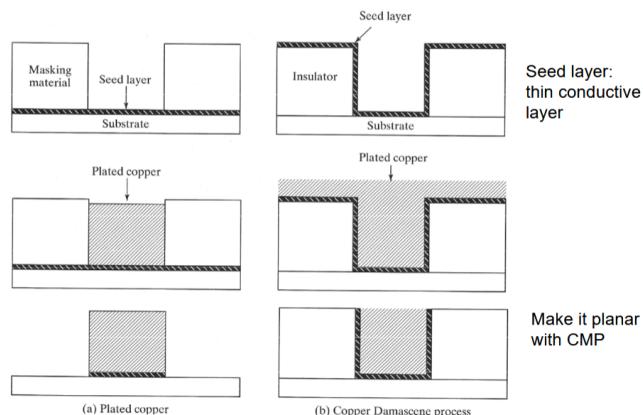


Figure 22: Electroplating

Dual damascene is used when creating those wider form of via. Good for vias and interconnect traces.

It is often hard to etch metal so we can use lift off where we first apply the photoresist and then the metal. Finally we simply need to etch the mask and everything should come off. Here we want a **bad step coverage**.

7 IC Processing Overview

up to slide 47

The biggest issue currently is the non-aligning gate. With the Aluminium gate we **can't use some ion implantation** since it is happening above the melting point of the gate. So the process is trickier and same for etching, only low temp process → mostly isotropic and wet. Good for $> 5\mu m$.

We ditched it to go for some nice polygate, can use fancier process and they are self aligning. Good for $< 10\mu m$.

7.1 Al vs poly

Here, we first need to dope the substrate before depositing the gate as we usually go into melting point order. From high to low.

For poly, we first deposit the gate and then dope the wafer. This will make sure that drain and source are already aligned !

Here, we still do some LOCOS operation to isolate our PMOS and NMOS. And then once the base is laid down we can start adding our poly-gate. We apply all the tips and informations we have seen in the course to build a good transistor.

- | | |
|--|---|
| 1. Starting wafer 2. Initial oxidation 3. N-well photolithography 4. Oxide and photoresist etch 5. N-well implant oxidation 6. N-well implant 7. N-well drive-in 8. Oxide etch 9. Pad oxidation 10. Nitride deposition 11. Active photolithography 12. Plasma nitride etch 13. Field implant photolithography 14. Field implant 15. Photoresist removal 16. Field (LOCOS) oxidation 17. Nitride and pad oxide etch 18. Sacrificial oxidation 19. Threshold implant | 20. Sacrificial oxide etch 21. Gate oxidation 22. Poly-Si deposition 23. Gate definition 24. Plasma polysilicon etch 25. N ⁺ S/D photolithography 26. N ⁺ S/D implant 27. Photoresist removal 28. N ⁺ anneal 29. P ⁺ S/D photolithography 30. P ⁺ S/D implant 31. Photoresist removal 32. PSG deposition and densification 33. Contact photolithography 34. Contact etch 35. Metallization 36. Metal photolithography 37. Metal etch 38. Truncate/reflect Nmos |
|--|---|

Figure 23: Process of such transistor

7.2 Latch-up issue

For this, it is important to use some good EPI and STI to avoid any cross connection resulting in a possible *thyristor*.

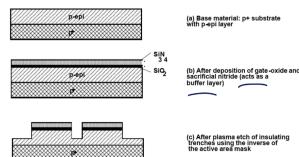
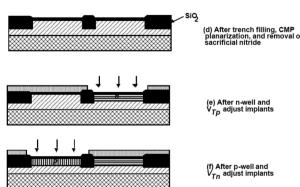
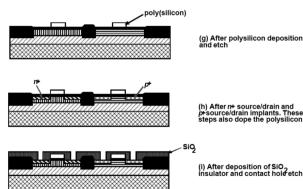
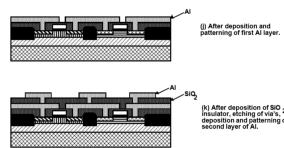


Figure 24: Advanced CMOS process 1

**Figure 25:** Advanced CMOS process 2**Figure 26:** Advanced CMOS process 3**Figure 27:** Advanced CMOS process 4

7.3 Hot carrier effect

It happens when a strong EM field is applied and when an electron has enough *kinetic energy* to break lattice bonds and hence create another electron-hole pair. They have an energy over kT . This will increase the current in the channel but the holes will be absorbed by the substrate creating a little current that can be monitored. This creates a sort of BJT.

This is why we often add some spacer to help with this effect.

7.4 Contacting issues

For this we again use some salicides, by blanket depositing, a bit of the metal will react and simply diffuse. The other non-reacted can be targeted and removed. Contact is now made easy. We usually do some **annealing** to improve the resistivity of the contact.

7.4.1 Gate last

Here we first add a dummy gate and at the end attach contact of the gate using some metal, replacement of poly-silicon.

8 Packaging

Not seen this year.

9 Extra table – Used Gemini / Notebook LM

Here is a summary of the growth and etching rates, presented in a table for clarity. This response incorporates information from both the newly provided sources and our conversation history, with clear indications where information from the previous summary is not directly supported by the current set of source documents.

9.0.1 Growth and Etching Rates in Microfabrication Processes

Table 4: about Deposition

| Process / Material | Rate / Parameter |
|---|--|
| Photoresist Coating | 0.05 μm to 100 μm. |
| PVD Evaporation | 0.1-1 nm/s |
| PVD Sputtering | 1-10 nm/s |
| CVD Polysilicon from Silane (SiH4) | Approximately 10 nm/min at 630C and 400 mTorr |
| Dry Oxidation | About 0.5 μm in approximately 6 hours at 1200C |
| Wet Oxidation | About 0.5 μm in approximately 1 hour at 1200C |

Table 5: about etching

| Process / Material | Rate / Parameter |
|---|--|
| Wet Etching (HF 49% for SiO2 / PSG) | > 1 $\mu\text{m}/\text{min}$ |
| Wet Etching (Dilute HF 1% for native oxide) | Approximately 10 nm/min |
| Wet Etching (Silicon with HNO3 : HF : CH3COOH) | > 10 $\mu\text{m}/\text{min}$ is possible |
| RIE | Can be between 0.1 – 0.5 $\mu\text{m}/\text{min}$ depending on the combination |
| Deep Reactive Ion Etching (DRIE) | > 10 $\mu\text{m}/\text{min}$ |

Table 6: Concentrations and Quantitative Measures in Microfabrication Processes

| Category | Specific Parameter | Value / Range | Unit | Notes |
|---|---|---------------------------------|------|--|
| Photoresist (Layer Characteristics) | Uniform Thickness | 5 nm | - | Refers to the uniformity of the thickness of the photoresist layer formed by centrifugal force. |
| Photoresist (Layer Characteristics) | Total Thickness Range | 0.05 μm to 100 μm | - | The range of thicknesses that can be achieved for a photoresist layer. |
| Plasma (Ionization) | Degree of Ionization | 10^-2 to 10^-6 | - | This is the ratio of ionized particles to total neutral atoms/molecules in the “weak” plasma used for IC microfabrication. |
| Dopant Concentration (General) | Impurities of SCS (Lower Limit) | 1E13 cm^-3 | - | |
| Dopant Concentration (Thermal Diffusion) | Intrinsic Carrier Concentration (at 1000C) | 5x10^18 cm^-3 | - | Basic diffusion theory is valid for doping concentrations less than this intrinsic carrier concentration. |
| Dopant Concentration (Thermal Diffusion) | Upper Limit (Solid Solubility) | ~1E14 to ~1E21 cm^-3 | - | This range represents the maximum solubility of various dopants in silicon, varying with the specific element (e.g., P, As, B, Sb, Al, Ga, Cu, In, Au, Fe, Zn) and temperature (700-1100C), as observed from the provided graph. |
| Dopant Concentration (Typical Doping) | MOS Transistor Sources/Drains and Bipolar Transistor Emitters | 1x10^20 cm^-3 | - | Typical doping concentration for these specific regions in integrated circuits. |
| Dopant Concentration (UV Photodiode Example) | Range Across Different Regions | 1x10^15 to 1x10^20 cm^-3 | - | Example doping concentrations found in different regions of a UV photodiode, such as p+ anode, n+ cathode, p-base, n-collector, and n+ buried layer. |

| Category | Specific Parameter | Value / Range | Unit Notes |
|--|--|----------------------|--|
| Dopant Concentration (Ion Implantation) | CMOS Well | 10^15 - 10^17 | atoms/cm^3 Typical concentration range for doping in a CMOS well. |
| Dopant Concentration (Ion Implantation) | Source/Channel/Drain | 10^17 - 10^20 | atoms/cm^3 Typical concentration range for doping in source, channel, and drain regions of a device. |
| Dopant Concentration (Ion Implantation) | Phosphorous Implantation Peak (example for 50, 100, and 150 keV) | Over 10^20 | cm^-3-Derived from the graph showing impurity concentration versus depth for phosphorous implantation at various energies; specific values can be read, e.g., approximately $2 \times 10^{20} \text{ cm}^{-3}$ for 50 keV. |
| Ion Implantation (Dose) | Ion Dose (Area Under Gaussian) | 1E15 | /cm^2 This is the total amount of dopant per unit area for the specific phosphorous implantation example given. |

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