DAMSIC Questions

An Open-Source Summary

Thomas Debelle

KU LEUVEN

June 24, 2025

Contents

1 Recap of questions per chapter

1.1 S&H

Q	page	Q	page
1	19	**2**	31
3	44		

1.2 DAC

Q	page	Q	page
4	16-17	**5**	28
6	36		

1.3 ADC

Q	page	Q	page
7	9-11	**8**	38
9	40-41	**10**	56
11	63	**12**	71
13	89		

Used notebook LM on top of already answered questions:

2 H05E3A - Exam Questions

Here is a comprehensive response to your query, drawing on the provided sources:

1. Describe the pedestal step and a possible solution for the problem.

    - **Pedestal Step and Solution:** The **pedestal step** is a non-ideality observed in Sample and Hold (S&H) circuits, appearing as an **abrupt change in the output voltage (V_{out})** during the transition from the sampling phase to the hold phase. This effect is visually represented as a sudden upward or downward jump in the V_{out} waveform at the moment the input signal is sampled. It is primarily caused by **charge injection from the channel** and by **parasitic capacitance between the gate and output** from the switch as it turns off, specifically due to the switch's drain-capacitance and unintended coupling.
    - A possible solution for pedestal step compensation involves using **half-sized dummy switches**. These dummy switches are designed to absorb the charge from the main switch, thereby reducing the unwanted pedestal step. For this method to work effectively, the charge must split approximately 50% between the main and dummy switches. However, the success of this compensation technique is critically dependent on the **careful timing of clock edges**. If there are unequal impedances on the left and right sides of the main switch, or if clock edges are too fast, it can lead to an unequal charge split, which will diminish the effectiveness of the compensation. Therefore, ensuring that the **impedances are as equal as possible** is crucial for optimal compensation.

2. Discuss the need for bootstrapped switches in switched-capacitor circuits.

    - The main issue is the fact that $R_{on} \propto 1/V_{gs}$. So by changing the input voltage we change the RC time constant and so it creates **DISTORTION** which is highly unwanted in TH circuits. Solution –> Keep it constant using **bootstrapping** aka keep a constant V_{gs}.
    - So we need to keep V_{gs} high to avoid any saturation. The higher the Vgs the smaller the R_on resistance. We first need to do a hold phase on the cap to charge it up to Vdd then in the track phase that input voltage is added on top of the cap.
    - Challenges: make sure the body diodes do not open which will result in current to substrate, charge lost and latch-up !
    - **Need for Bootstrapped Switches in Switched-Capacitor Circuits:** Bootstrapped switches are important components in switched-capacitor (SC) circuits, particularly when **high accuracy** is required. In the context of Delta-Sigma converters, for example, they are specifically utilized **at high accuracies** to mitigate the effects of **clock feedthrough**.

3. Discuss offset and noise in the flip-around T/H circuit.

    - With a regular T&H circuit, the signal transfer function should be 1. This means that the sampling capacitor should be equal to the feedback capacitor. This results in a feedback factor of 1/2, so a closed loop gain of two.
    - An alternative is the flip-around T&H, which uses no feedback capacitor. During both phases, the opamp is in unity gain feedback. The offset and low frequency noise are cancelled out, because they affect both the V_C_hold and the output voltage. The high frequency noise is amplified by a factor of two.

- The offset voltage cancels out because the opamp creates its own virtual ground in both phases. Noise transfer function from opamp input node to output. The sampled thermal noise on C_hold is still present.

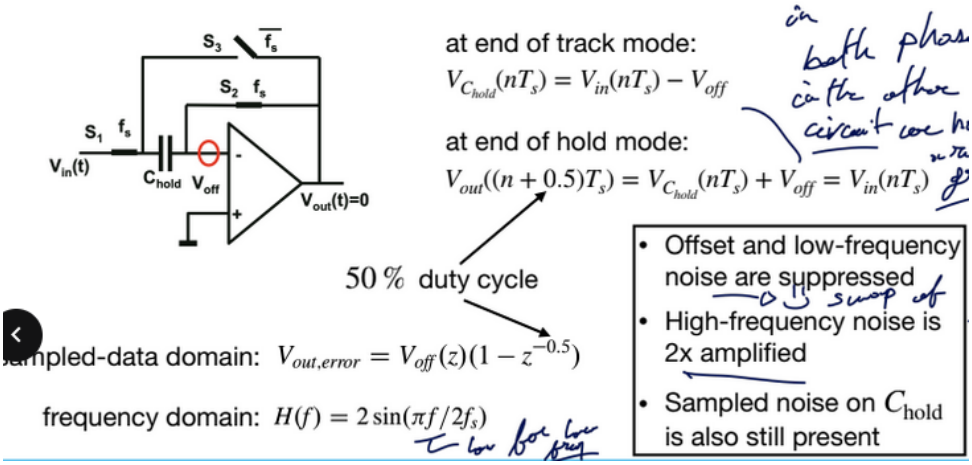

Figure 1: Equations for Flip around

-

4. Discuss the effect of the impedance variation in a resistor ladder in resistive DACs

   - **Effect of Impedance Variation in Resistor Ladder DACs:** In resistive Digital-to-Analog Converters (DACs) employing a resistor ladder, the output impedance exhibits a significant variation with the input code. This variation is characterized as a **parabolic function**. The equivalent resistance ($R_{eq}(m)$) can be calculated using the formula $R_{eq}(m) = \frac{m(2^N - m)}{2^{N+1}} R_{tot}$, where m is the digital input code and 2^N is the total number of resistors. The maximum equivalent resistance, equal to $0.25 \cdot R_{tot}$, occurs at the midpoint of the digital range.
   - This **parabolic variation of impedance** has several detrimental effects on the DAC's performance:
     - It leads to **signal-dependent current delivery**, meaning the current supplied to the load changes non-linearly with the input signal. In other terms **DISTORTION**
     - For a fixed capacitive load, the **time constant becomes signal-dependent**, which affects the settling behavior of the DAC output.
     - Collectively, these signal-dependent characteristics introduce **distortion at high frequencies**, degrading the overall linearity and dynamic performance of the DAC.

5. Discuss the common-centroid layout in the framework of current-steering DACs.

   - Current steering DAC can be unary or binary. Unary are preferred for MSB to avoid big current switch off and on and binary for LSB.
   - Current steering DACs (unary) are very sensitive to mismatches. Instead of using matrix decoding, where all sources are placed sequentially (according to bit order) in a grid, issue:
     - Doping, oxide thickness not constant
     - PSS drop
     - Clock timing
     - Temperature

- they can be placed according to a common-centroid layout. This layout is symmetrical in both dimensions. **Any linear gradient in the production process is cancelled** out by the fact that two opposing sources are used (vertical, horizontal and slant). The addressing of the sources is less straightforward than with matrix decoding.
- To go even further, every current cell can be subdivided and distributed across the array with some Q^2 schemes which improve reliability against second order effect.

6. Describe the problem of stray capacitances in the design of capacitive DACs.

   - **Problem of Stray Capacitances in Capacitive DACs:** Stray capacitors are capacitance from the switches right next to the (binary scaled) capacitors. The stray capacitor at the left poses no problem (not added to output). The charge of the right one is added to the feedback capacitor, which means that the total charge transferred is no longer correct. The problem can be solved by using four switches per capacitor instead of two.
   - In the charge phase, the first stray cap is charged but not the right one. The trick in the transfer phase is that the charged left cap will have both inputs connected to the same Vref- so it will discharge onto this. Thanks to the virtual ground of the opamp, the right cap will not be charged making the error 0.
   - Right stray is never charged (thanks to virtual ground of the AMP) and left one will charge and discharge on itself

7. What limits the regeneration in a latch-based comparator, and how can it be improved?

   - Comparators are difficult blocks as we need **High BW, high AMP, High Accuracy, Wide range, Low power** so latch helps with it thanks to a feedback loop but we need a David Goliath latch to still be able to change the value on it. Latch is better than cascade of amp as cascading amp is **SLOWWWWW** + Memory effect.
   - 2 phase latch with first pre-amp and then latch behavior.
   - **Limits to Regeneration in Latch-Based Comparators and Improvements:** In a latch-based comparator, the regeneration process, where a small input difference is amplified to a full digital output, is characterized by an exponential growth of the differential voltage $V(t)$ across the latch outputs, given by $V(t) = \alpha V_{LSB} e^{+t/\tau}$. The regeneration speed is fundamentally determined by the **time constant** $\tau = C/g_{m,l}$, where C is the parasitic capacitance at the output nodes and $g_{m,l}$ is the transconductance of the latch's gain stage. Pre amp –> $A_{pre} = \frac{g_{min}}{C} T_{pre}$
   - The regeneration in a latch-based comparator is limited by three regimes based on the input differential voltage (ΔV_{in}):
     - **High** ΔV_{in}: The regeneration time is limited by the inherent **propagation delay** of the latch circuit. –> Tech constant max speed
     - **Medium** ΔV_{in}: The comparator operates within the **exponential regime**, where the signal grows exponentially. –> Take a bit of time to get the result $\tau \approx 10ps$.
     - **Small** ΔV_{in}: In this critical regime, **noise dominates the input**, leading to potential errors in the decision-making process. This is closely related to the phenomenon of **metastability**, where the comparator fails to produce a stable output within the required time, resulting in an ambiguous output. Metastability can lead to conversion errors in Analog-to-Digital Converters (ADCs).

- To improve regeneration performance and mitigate metastability errors:
  - One can **reduce the effective number of bits (N)** in the converter, or conversely, **increase the sampling period (T_s)**, which effectively reduces the operating speed. –> longer Pre-amp stage to avoid the small ΔV_{in}.
  - Another approach is to **reduce the time constant** τ. This can be achieved by decreasing the parasitic capacitance C or increasing the transconductance $g_{m,l}$ of the latch (so higher power consumption, wider NMOS, weak inversion).
  - While metastability is a critical issue for general comparators, in Delta-Sigma ($\Delta\Sigma$) converters, it is considered **"not an issue"** for the comparator itself because any comparator error will be shaped and subsequently filtered. However, it is essential to ensure that the digital bit fed to the decimation filter is the same as the one fed to the DAC, which typically requires placing a **synchronization latch**.

8. How can averaging improve the performance of a flash ADC?

- **How Averaging Can Improve Flash ADC Performance:** The provided sources do not explicitly detail a general "averaging" technique applied to the overall output of a flash ADC to improve its performance. However, they discuss how certain *comparator-level* techniques, which involve aspects of mitigation or compensation across elements, address issues like offset and noise that would otherwise degrade flash ADC performance.
- A flash Analog-to-Digital Converter (ADC) utilizes $2^N - 1$ comparators to convert an analog input into an N-bit digital word. A major non-ideality in flash ADCs is **comparator offset**, which results in non-ideal thresholds and contributes to differential non-linearity (DNL) errors.
- While direct "averaging" of multiple comparator outputs for improved resolution or linearity is not explicitly described, the following related techniques are mentioned that contribute to better performance:
  - **Auto-zeroing schemes**: These techniques are employed to **cancel comparator offset** and suppress both offset and low-frequency noise within individual comparators. This can be seen as a form of "temporal averaging" or correction within each comparator.
  - **Comparator with Offset Cancellation**: An approach for open-loop comparator offset cancellation involves selecting a subset (e.g., "four-out-of-eight minimally sized input pairs") from multiple input pairs. While not explicitly stated as averaging their outputs, this selection process aims to achieve a more ideal performance by potentially averaging out random offsets across a pool of devices.
  - **Majority voting**: In the context of Successive Approximation Register (SAR) ADCs, it's mentioned that **majority voting** can be used to mitigate **comparator noise**. While stated for SAR ADCs, the principle of using multiple decisions to reduce noise and errors could conceptually be applied to other ADC architectures like flash ADCs if multiple comparator outputs are available and processed.
- Therefore, while the sources don't present a method of "averaging the flash ADC" as a whole, they illustrate how individual comparator imperfections, particularly offset and noise, can be mitigated through techniques like auto-zeroing and strategic design choices (like selecting multiple input pairs or employing majority voting in other ADC types), which improve the overall ADC accuracy.

9. Discuss the folding technique, its advantages, and challenges.

- **Folding Technique, Advantages, and Challenges:** The provided sources **mention the "folding" technique as a type of Analog-to-Digital Converter (ADC) architecture, but they do not provide a detailed discussion of its advantages or challenges**.
- Specifically, the "Comparator Schematics" section refers to a publication on "CMOS folding and interpolating A/D converter". This indicates that folding is a known and utilized architecture in high-speed ADC design, often combined with interpolation. However, no further information regarding its operational principles, specific benefits (such as reduced comparator count compared to flash ADCs), or design challenges (such as folding amplifier linearity or bandwidth requirements) is elaborated upon within the given text.
- Without additional information, a comprehensive discussion on the advantages and challenges of the folding technique cannot be constructed from these sources.

10. **Advantages and Disadvantages of a 1.5-bit Pipeline Converter Compared to a 1-bit Pipeline Converter:**

    Pipeline converters break down the analog-to-digital conversion into multiple stages, each processing a certain number of bits. The comparison between 1-bit and 1.5-bit stages primarily revolves around trade-offs in speed, complexity, and accuracy.

    1-bit Pipeline Converter:

    - **Advantages:**
      - **Maximum speed**: With its subrange limited to a single bit, it typically uses an amplifier with a 2x gain, which can achieve high conversion speeds.
      - **Intrinsic linearity**: The 1-bit DAC in its feedback loop is inherently linear, contributing to the overall intrinsic N-bit precision of the converter. A 1-bit DAC is always perfectly linear, and time-domain converters leverage this for excellent linearity.
      - **Simplicity**: Requires only a single comparator for its analog-to-digital conversion within each stage.
      - The basic building block is a Multiplying Digital-to-Analog Converter (MDAC).
    - **Disadvantages:**
      - **Delay**: The full digital value is available after N+3 clock periods, as each stage processes one bit sequentially. This delay, while exchanged for speed, can be problematic in feedback loops.
      - Potentially more stages required for a given resolution compared to multi-bit stages, which could increase overall complexity and power (though per-stage power is low).

    1.5-bit Pipeline Converter (a type of Multi-Bit MDAC Pipeline Converter):

    - **Advantages:**
      - **More aggressive stage-scaling**: By processing more than one bit per stage (e.g., 1.5 bits, 2.5-4 bits), these converters allow for a reduction in the total number of stages required for a given resolution. This can lead to more compact designs.
      - **Error Correction Margin**: Having more levels per stage (e.g., six segments for 2.5 bits) provides a margin to correct errors that might occur in the comparators.

  - **Higher Overall Performance**: Can achieve higher effective number of bits (ENOB) at comparable or higher sample rates compared to purely 1-bit per stage designs, as seen in examples where 2.5-bit stages are used at the front-end followed by 1.5-bit stages.

- **Disadvantages/Challenges:**
  - **Slower amplifier settling**: Due to the higher gain required in multi-bit stages (e.g., 4x or 8x gain), the amplifiers need more time to settle accurately.
  - **More complex DACs**: The first stage requires a multi-level DAC (e.g., a five-level DAC for a 2.5-bit stage) that must maintain the **full accuracy of the entire converter**. This multi-bit DAC is a critical component and its non-linearity due to mismatch can be a significant problem.
  - **Increased Complexity for DAC Linearity**: Mismatch in multi-bit DACs can generate non-linearity errors. Techniques like **Data Weighted Averaging (DWA)** are used to make these errors noise-like so they can be filtered by oversampling, resulting in much lower harmonic distortion. This adds complexity to the digital processing.

3 License