Technology of Microelectronic- Important values

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First Chapter

Positive etch mask = exposed area will be removed. Negative vice versa.

Wafer Size	Thickness
4”	400 μm
8-12”	1.2 mm

Silicon properties

Cheap and strong, fragile. Resistivity 0.001 - 20 $k\Omega/cm$. Can be SCS, poly or amorphous. Can deform without cracking for quite some time.

looking into 1 direction 10^5 atoms that aren't $\sim$ on 1cm

- $10^{15}/cm^3$ -> $10^5/cm$ = 10/µm (!)
- 1cm = 10^8Å

1Å = 0,1 nm

Dopant level	Designation	Dopant concentration (cm^{-3})	Resistivity n/p (ohm-cm)
Very lightly doped	n^{--}, p^{--}	$<10^{14}$	>100/>30
Lightly doped	n^-, p^-	$10^{14}-10^{16}$	1–100/0.3–30
Moderately doped	n, p	$10^{16}-10^{18}$	0.03–1/0.02–0.3
highly doped	n^+, p^+	$10^{18}-10^{19}$	0.01–0.03/0.005–0.02
Very highly doped	n^{++}, p^{++}	10^{19}	0.001 < 0.01/0.005

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In a Si cube we have 8 atoms inside the cell. with:

$$Volume = (.543nm)^3 \qquad \frac{8}{Volume} = 5 \cdot 10^{22} atoms/cm^3$$

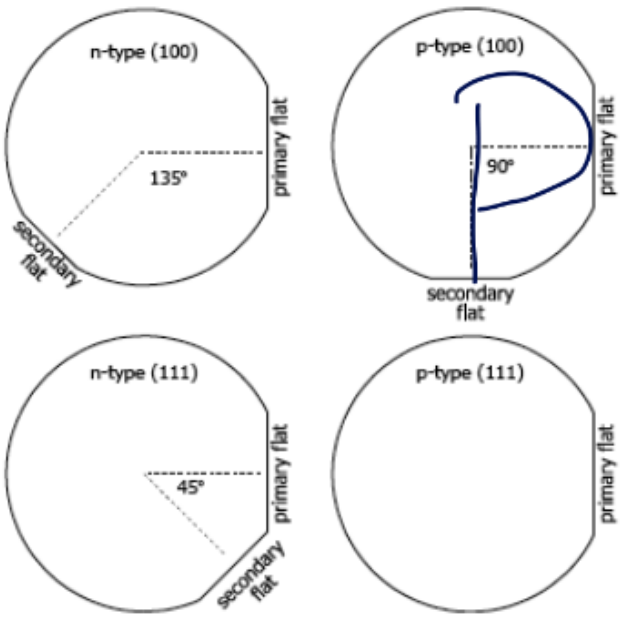
SCS has a purity up to 11 nines ! and is 2 FCC lattices displaced by .25, .25, .25.

Boule making

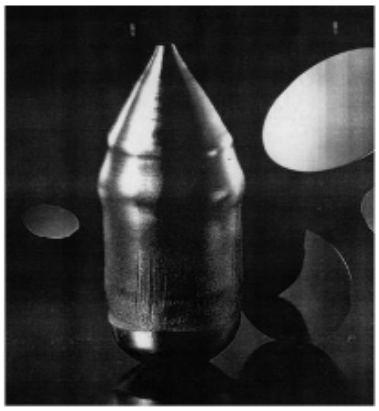
To create a Boule we can use a Czochralski pulling at 1420C. The pull rate is around **mm/min**. 30 hours for 2m + 30 hours for cooling!

Wafer treatment First we have to cut then to get a perfect wafer we will have:

1. Lapping: $20\mu m$/side
2. Edge profiling: makes edge cleaner
3. Etching (chemical): $20\mu m$/side
4. Polishing (CMP): $25\mu m$/side



Miller indices indicated by gound edges called "flats". "n"-type and "p"-type refer to "doping". N means "negative" (phosphorus) and P means "positive" (boron).



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A boat can contain between 12 to 24 wafer.

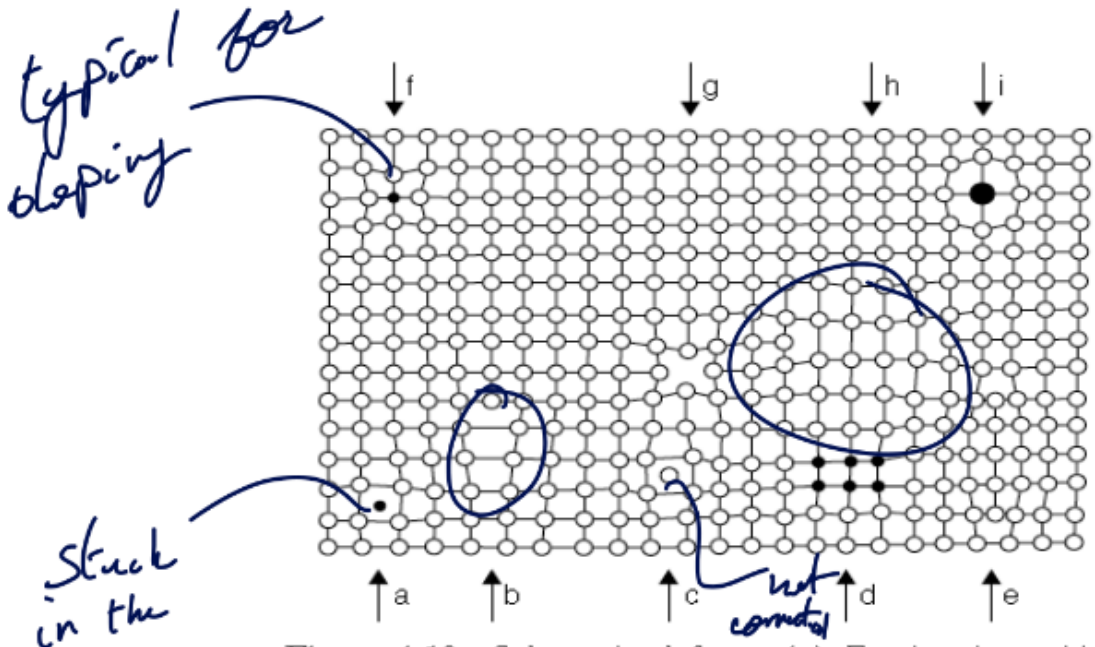

Figure 4.10 Schematic defects. (**a**) Foreign interstitial; (**b**) dislocation; (**c**) self-interstitial; (**d**) precipitate; (**e**) stacking fault (external); (**f**) foreign substitutional; (**g**) vacancy; (**h**) stacking fault (internal); (**i**) foreign substitutional. From Green, M.A. (1995), by permission of University of New South Wales

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We drop some die on the chips that aren't good due to a defect. Lower defect ratio allows to put bigger transistor. But going smaller isn't always the best as the interconnect cost can quickly ramp up as we go too small. So optimization process between Packaging and reliability (yield).

Class	1	10	100	1000	10 000
No. of particles 0.5 µm	1	10	100	1000	10 000
No. of particles 0.1 µm	35	350	3500	35 000	350 000

	0.1 µm	0.2 µm	0.3 µm	0.5 µm	1 µm	5 µm
ISO class 1	10	2				
ISO class 2	100	24	10	4		
ISO class 3	1000	237	102	35	8	
ISO class 4	10 000	2370	1020	352	83	
ISO class 5	100 000	23 700	10 200	3520	832	29

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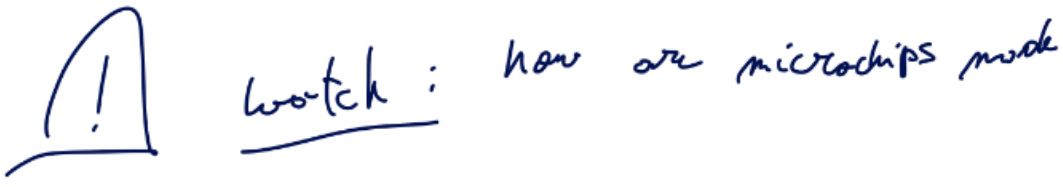
ISO	FS209	Certification Particle Size (µm)					
Class	Class	0.1	0.2	0.3	0.5	1.0	5.0
1	---	10	2	---	---	---	---
2	---	100	24	10	4	---	---
3	1	1,000	237	102	35	8	---
4	10	10,000	2,370	1,020	352	83	---
5	100	100,000	23,700	10,200	3,520	832	29
6	1,000	1,000,000	237,000	102,000	35,200	8,320	293
7	10,000	---	---	---	352,000	83,200	2,930
8	100,000	---	---	---	3,520,00	832,000	29,300
9	---	---	---	---	35,200,000	8,320,000	293,000



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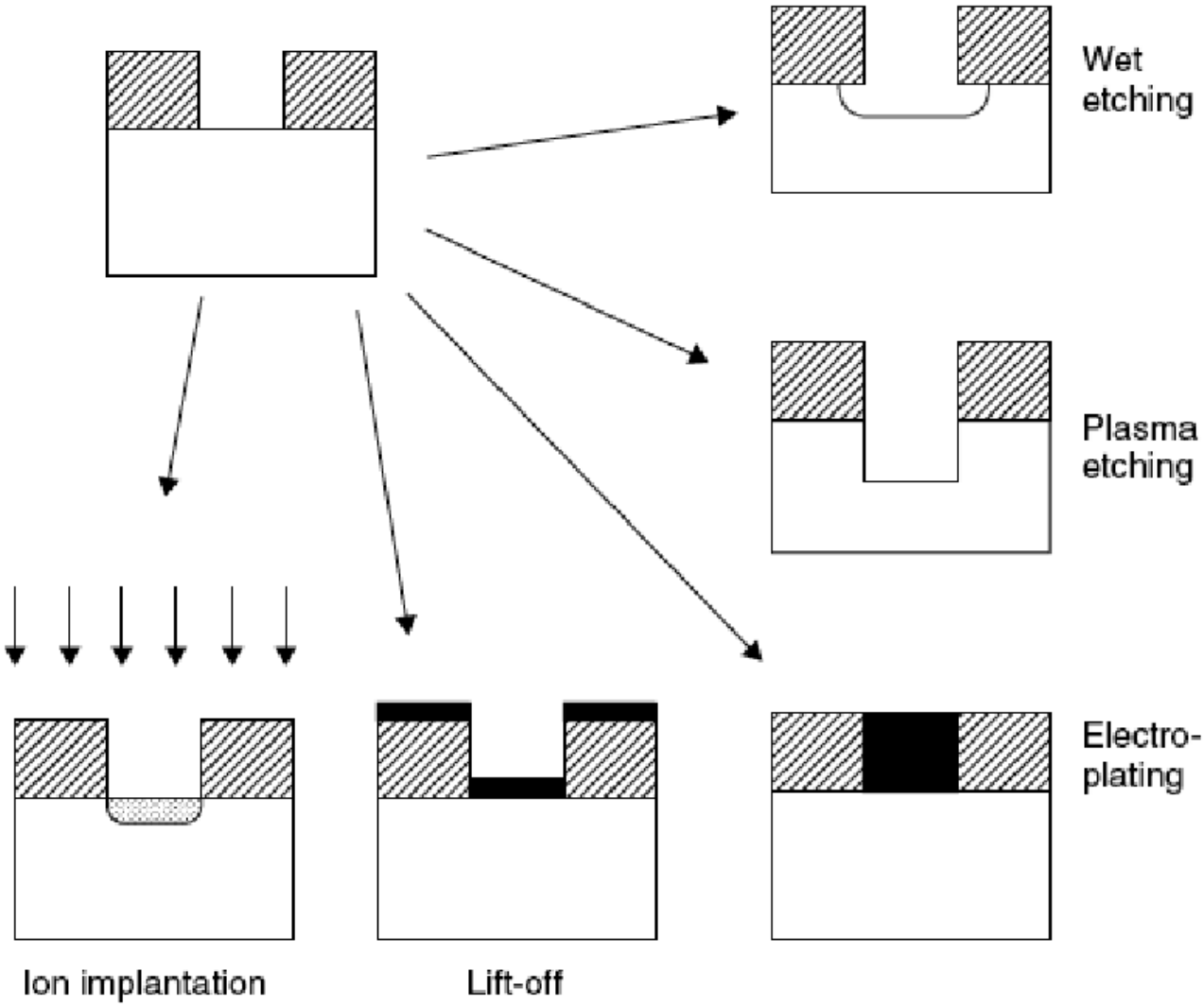
Class ISO:

- 10.000: PCB, packaging
- 1.000: MEMS, packaging, HDD
- 100: MEMS, RF/Photonic ICs
- 10: IC

2 Lithography



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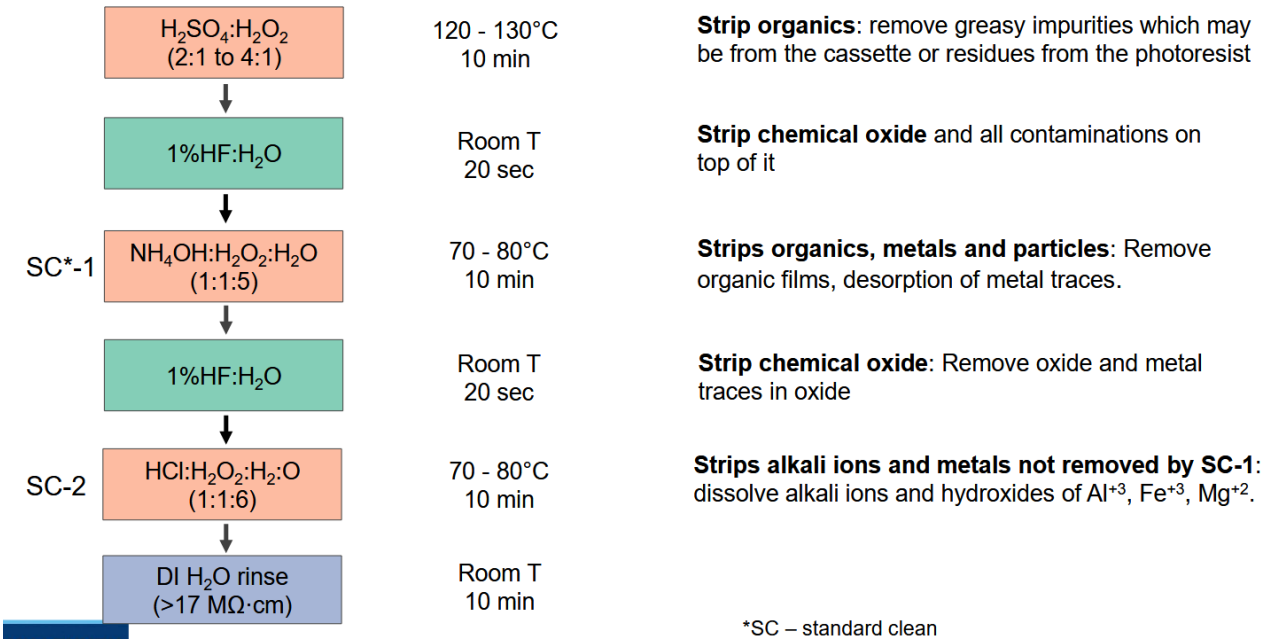

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After this we can apply some HMDS to remove the OH group at the top of the wafer to make the photoresist sticks better. We must also apply some anti-reflective coating to avoid the UV light to strike unwanted area.

Resist spinning

We drop a little bit of the photoresist and then spin it faster to make it a nice and even coat:

$$T = \frac{KC^{\beta}\eta^{\gamma}}{\omega^{\alpha}}$$

The thickness is $0.05 - 100\mu m$. The thickness varies due to step on the wafer (previously deposited material).

Start time (sec)	Duration (sec)	rpm	Dispense	Comments
0	0	0	—	Load wafer
0	2	1000	N_2	Blow off wafer
2	10	500	HMDS spray	Apply primer
12	10	3000	—	Spin-dry primer
22	1	0	—	Allow wafer to stop spinning
23	3	0	Resist	Dispense resist and let spread
26	5	500	—	Spread resist
31	20	3000	—	Spin resist
51	0	0	—	Unload wafer

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We can also use some *spray coating* to spray and rinse through a nozzle. The step coverage is better and more uniform. There is also dip coating and laminating while they are less used in this industry.

After this we usually do some soft baking to improve resolution. If too long we may decompose the resist watch out !

- few mins at 100C

- 30 mins in a convection oven

Optic

PSM is a prime example to improve resolution. With ARC we also trap some lights in the resist creative some over exposed and ripple in the sidewalls.

So we usually bake PEB to improve the sidewalls ripple ! We use some OPC to correct and get the desired shape that may looks different on the mask. Usually we print on a metal on chrome mask using an e-beam. Either we use a master mask and directly use it to print on the wafer or we first use the master mask to create a larger mask with multiple master mask print on it. Reduction by **4 to 5** times reduction from mask to wafer !!!

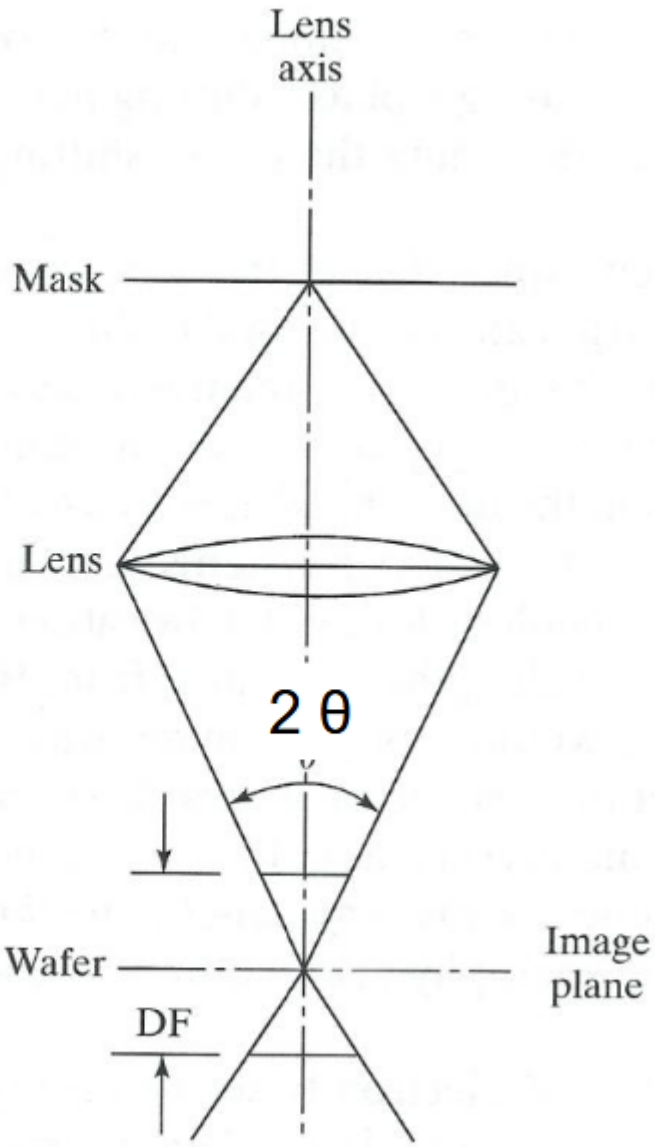
3 types of printing

1. Contact printing: Mask is touching the wafer
   - Better resolution (less diffraction)
   - Mask wear and wafer damage
2. Proximity printing: not touching this time
   - Lower resolution
   - Better mask lifetime
3. Project printing: uses a set of lenses to focus on the mask and then on the wafer
   - Expensive technique but best of both

Mask and formulas

The most important metrics are:

- **Critical Dimension**: $CD = k1\frac{\lambda}{NA}$
- **Numerical Aperture**: $NA = nsin(\theta)$
- **Depth of Focus**: $DOF = k_2\lambda/NA^2$ where $k_2 < 1$



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So clearly, we can see why having a small wavelength matters to get better precision. To improve again we can use a wider θ.

With the DOF, some part could be in focus while other not which is really problematic. We can't have a nice and uniform resolution accross multiple lengths.

Lights

Source	Wavelength (nm)	Name
Hg arc lamp	436 (blue)	g-line
	405 (violet)	h-line
	365 (UV)	i-line
	248	DUV
KrF excimer laser	248	DUV
ArF excimer laser	193	DUV
F_2 excimer laser	157	DUV (vacuum UV)
plasma	13	EUV (long x-ray)

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Double patterning

We can use two mask to get virtually smaller features by combining those two together.

- LELE: reduces $k1$, double the cost since double patterning. Overlay issue :((
- SADP: self aligning. Simply use dummy fill then add THICKKK sidewalls, etch it a lil, remove dummy and boom 2 pattern for the price of 1.
- LFLE: based on a freezing process.
- SAQP: close to SADP but pitches less than $38nm$

EUV

We can't use lenses anymore. **7 mirrors with 70% reflection per mirror!** No pellicles that are EUV transparent yet.

To tune the linewidth we can change the exposure and development time.

For etching:

- wet etching: using acetone, IPA, water rinse. 2% NaOH for positive resists
- plasma etching: O2 plasma

4 Oxidation, wet, dry

SiO2 is forming a *tetrahedral arrangement*. Can create some amorphous structure too. The quality is determined based on the ratio of bridging to non-bridging elements.

In elec, we use some amorphous.

Spec	Value
density	$2 - 2.3gm/cm^3$
ε_r	3.9
reflection index n	1.5

Spec	Value
Breakdown field	$10^7 V/cm$
Trap/defect density at interface	$10^{11} cm^{-2}$

Thermal oxidation

Natural growth of a oxide exposed to air and enhanced by temperature. Useful for:

1) implant/diffusion mask
2) surface passivation
3) isolation between transistors
4) key component of MOS structures
5) dielectric for multilevel interconnect
6) cleaning

This grows in both way but slightly more outwards (**54/46**). SiO2 is 2.2 times larger than Si. Dry thermal is slower but better than wet oxidation. Dry has a higher breakdown voltage –> $5 - 10 MV/cm$ so really good for gate oxide (since they are getting smaller and smaller)!

For $.5\mu m$ @ 1200C :

- Dry: 6 hours
- Wet: 1 hour

We can have some interface issue as the step is not exactly the same and so the development won't be equal. Can use color to determine the thickness:

Thickness (μm)	Color
0.07	Brown
0.31	Blue
0.39	Yellow
0.41	Light orange
0.47	Violet

LOCOS

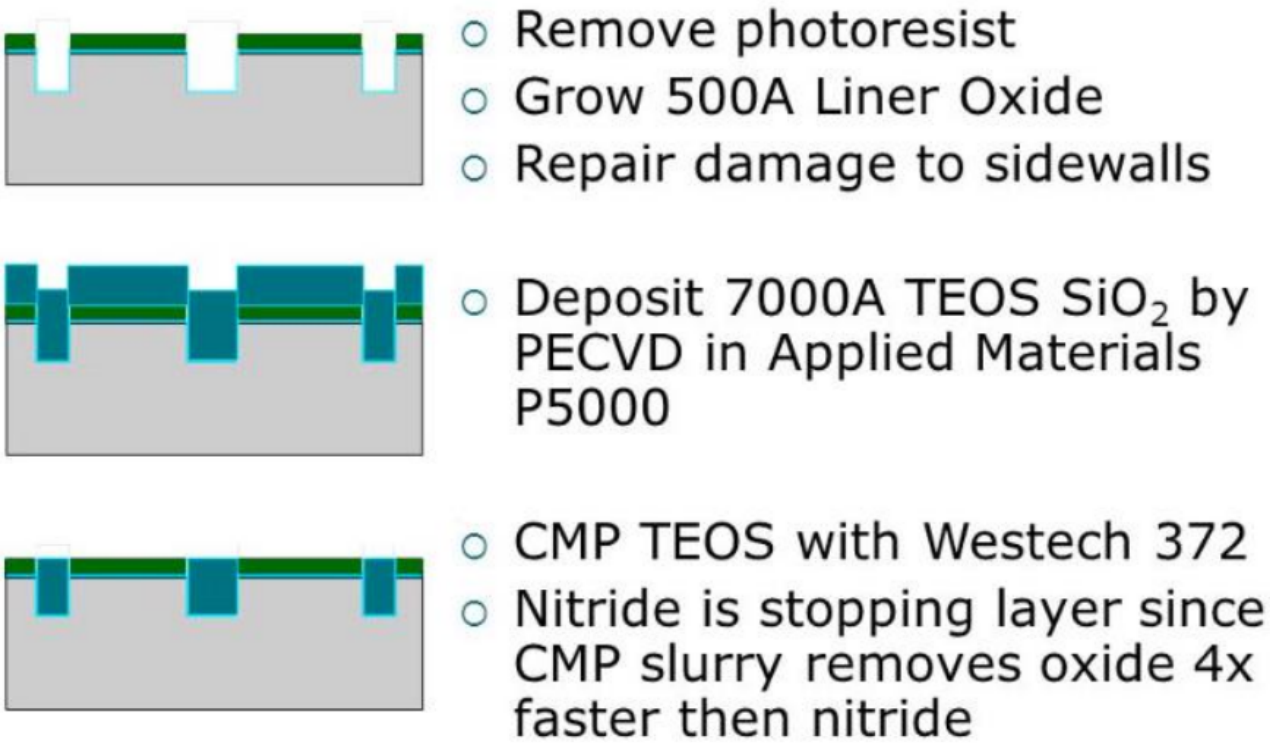
To have some isolation between transistor. Reduces topography by 56%. use some Nitrite which has a higher thermal expansion than Si. Add padoxide as stress release.

- Si3N4: $100 - 200nm$
- SiO2: padoxide: $20 - 30nm$

Wet oxi creating bird beak and then removing those oxide.

STI

Use CVD for the oxidation and CMP of the oxide avoids bird's beak and mechanical stress.



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Better precision, the width drawn is the actual width. We also use some dry oxidation which makes it better for large drive current.

Doping

We use either:

- gas, coating or ion implementation #### Diffusion Theory

We have a diffusion *flux* of *impurities* in one dimension. (We are always using x as the vertical direction of diffusion).

$$F = -D\frac{\partial C(x,t)}{\partial x} \quad D = D_0 exp\left(\frac{-E_\alpha}{kT}\right)$$

We have D that is the *diffusion coefficient* in cm^2/s. C is the dopant concentration per unit volume. We have D_0 that is the diffusion coefficient in cm^2/s at infinite temperature and E_α is the activation energy in eV.

At low concentrations of dopant in silicon ($10^{12} - 10^{16} cm^3$) can be seen as constant. With this simplification, we can easily solve the equation, we also see that gold, coper, ... have high diffusion coefficient which is why we tend to avoid such metal in the clean room.

If we do not have a source or sink of the impurity, we know that the *change in impurity concentration with time must equal the local decrease of diffusion flux*:

$$\frac{\partial C}{\partial t} = -\frac{\partial F}{\partial x} = \frac{\partial}{\partial x}\left(D\frac{\partial C(x,t)}{\partial x}\right) \quad \frac{\partial C}{\partial t} = D\frac{\partial^2 C(x,t)}{\partial x^2} \text{ if D cst}$$

There are 2 methods of diffusion:

1. Constant-surface-concentration: using vapor, we have a constant concentration of dopants at the surface.
2. Constant-total-dopant: thin layer, we have constant amount of impurity at the surface.

Constant-surface-concentration

$$\text{Init: } C(x,0) = 0 \qquad C(0,t) = Cs \qquad C(\infty,t) = 0$$

$$C(x,t) = C_S erfc\left(\frac{x}{2\sqrt{Dt}}\right) \quad erfc(z) = 1 - erf(z) \quad erf(z) = \frac{2}{\sqrt{\pi}}\int_0^{\pi} e^{-y^2} dy$$

We have $\sqrt{Dt}$ that is called the *diffusion length* in cm. The total number of dopant atoms per unit area that has diffused into the semiconductor is given by:

$$Q(t) = \int_0^{\infty} C(x,t)dx = \frac{2}{\sqrt{\pi}} C_s\sqrt{Dt} \approx 1.13 C_s\sqrt{Dt}$$

Constant-total-dopant

$$C(x,0) = 0 \quad \int_0^{\infty} C(x,t)dx = \phi \qquad C(\infty,t) = 0$$

$$C(x,t) = \frac{\phi}{\sqrt{\pi Dt}} exp\left(-\frac{x^2}{4Dt}\right)$$

Where ϕ is the *total amount of dopant* per unit area. So the surface concentration ($x = 0$) is $\phi/\sqrt{\pi Dt}$.

We usually use those two methods and we call this a *two step diffusion process*. a pre-deposition diffused layer is first formed using constant-surface-concentration condition. Then a drive-in (or redistribution) diffusion is used using constant-total-dopant condition.

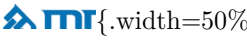
For most practical cases the diffusion length for the pre-deposition stage is much smaller than the diffusion length of the drive-in diffusion. This allows to make deep junctions, e.g. for wells for CMOS.

approximate to-bk

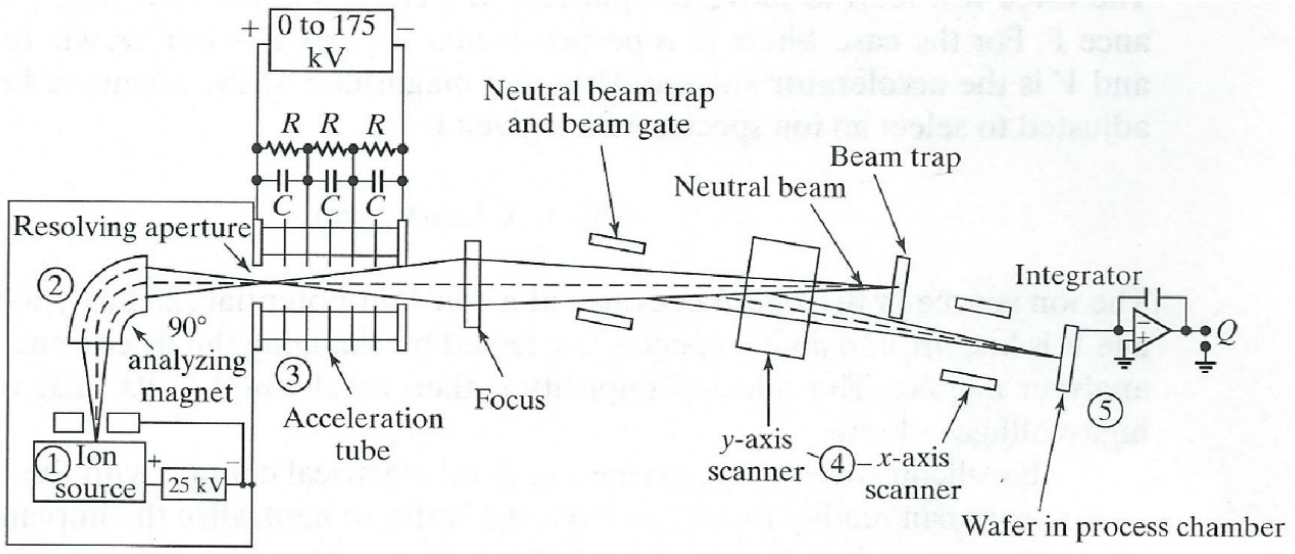
Dopant level	Designation	Dopant concentration (cm^{-3})	Resistivity n/p (ohm-cm)
Very lightly doped	n^{--}, p^{--}	$<10^{14}$	>100/>30
Lightly doped	n^{-}, p^{-}	$10^{14}-10^{16}$	1–100/0.3–30
Moderately doped	n, p	$10^{16}-10^{18}$	0.03–1/0.02–0.3
highly doped	n^{+}, p^{+}	$10^{18}-10^{19}$	0.01–0.03/0.005–0.02
Very highly doped	n^{++}, p^{++}	10^{19}	0.001 < 0.01/0.005

$A = w \cdot t \qquad R = \left(\frac{\rho}{t}\right)\left(\frac{L}{w}\right) = R_S\left(\frac{L}{w}\right) \qquad R_S = \frac{\rho}{t}\ [\Omega/\square]$

$R = \rho\frac{L}{A} \qquad \rho = \frac{1}{\sigma} \qquad \sigma = q(\mu_n n + \mu_p p) \qquad \left(\frac{L}{w}\right) = \text{number of squares material}$



We also need a minimum mask width to be able to absorb all those ions in the doping process.



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Ion Implantation

The source is at around $25kV$ and the high voltage accelerator goes above $> 5MeV$. There will be some undercut as the path traveled inside won't be straight and it will bounce. So th depth is a gaussian. Can have special behavior where the ion travels all the way through the lattice without bouncing.

$$N(x) = N_p exp\left(-\frac{(x-R_p)^2}{2\Delta R_p^2}\right) \qquad N_p = \frac{\phi}{\sqrt{2\pi}\Delta R_p}$$

ΔR_p being the *projected straggle* distance from the peak with concentration reduced by 40%.

Need some **rapid annealing** to repear the lattice after, will spread out the concentration sadly.

5 Etching, wet, dry, plasma, DRIE

Wet etching is cheaper **10k** while dry etching is **1M**. But wet etching is mostly isotropic meaning it goes into all direction which leads to al ot of undercut.

Wet etching is quite simple using a bath and a quick dump to stop precisely the etching and using some nozzle to stop any reaction. This limits the feature size as too close gaps can be bridged during the process $< 3\mu m$. We use **HF** for SiO2 **WATCH OUT** it will get through your skin without any pain but starts attacking your bones after.

Anisotropic

It has a prefered lattice orientation that will be etched faster. Dry etching is a combination of temperature and vacuum.

PHYSICAL ETCHING

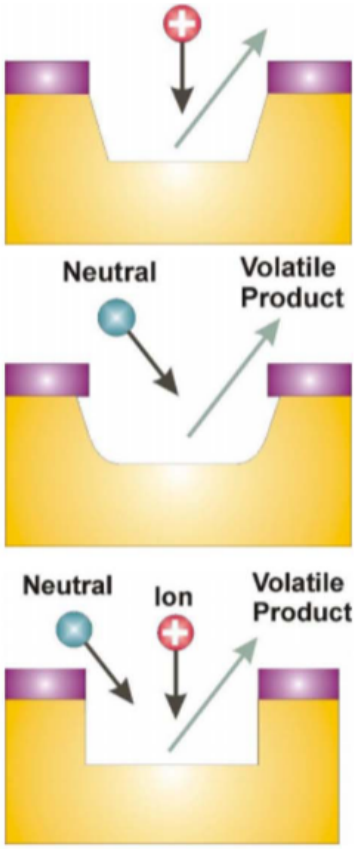
positive ions are accelerated and strike substrate with high kinetic energy, some energy is then transferred to surface atoms, which leads to material removal.

CHEMICAL ETCHING

neutral or/and ionized species interact with the material's surface to form volatile products. Chemical etching mechanisms typically etch in a isotropic fashion.

Combination of Chemical and Physical etching (Reactive Ion Etching - RIE)

An anisotropic profile is obtained



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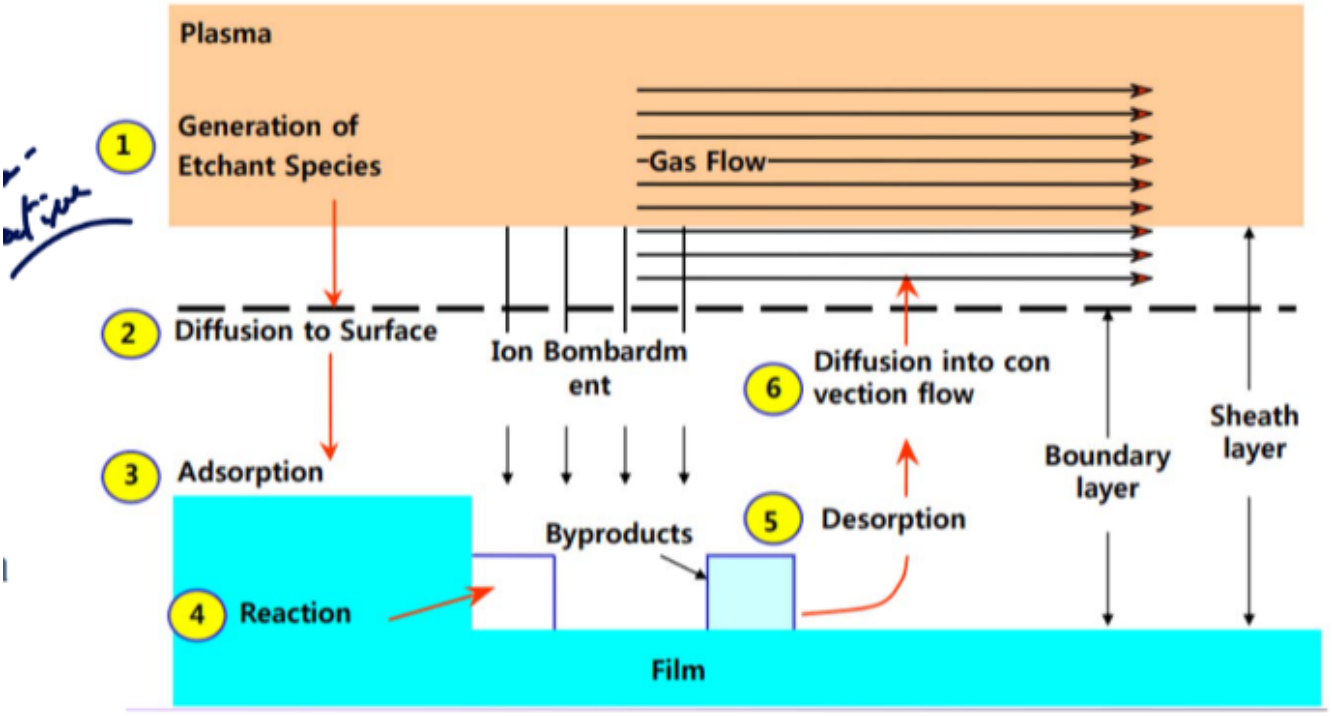
Plasma Etching Same amount of positive and negative charges but a different number of unionized molecules. Large electric field applied to a gas up to the **breakdown of the gas**.



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Needs **high kinetic energy and chemical reactions**. There are about $10^{15} cm^{-3}$ neutral species and $10^{8}-10^{12} cm^{-3}$. Ions go on the surface and strike it to remove some molecules.

TABLE 2.3 Etching Pressure Ranges

Etching Mode	Pressure (Torr)
Ion Milling	10^{-4}–10^{-3}
Reactive Ion Etching/Ion Milling	10^{-3}–10^{-1}
Plasma Etching	10^{-1}–5

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RIE will create a DC bias to accelerate the ions and add some extra kinetic energy towards the substrate. This is a combination of **chemical and sputter etching**. The chemical is purely isotropic and with little electrical damage while the sputtering is anisotropic and slower (this is ion milling).

	Plasma Etching		Reactive Etching		Physical Etching	
	Barrel Reactor	Planar Reactor	Ion	Ion Beam	Sputtering	Ion Beam Milling
Substrate Location	Surrounded by plasma	On grounded electrode in Plasma	On powered electrode in plasma	In beam, remote from plasma	On powered electrode in plasma	In beam, remote from plasma
Pressure (torr)	10^{-1} ~ 1	10^{-1} ~ 1	10^{-2} ~ 10^{-1}	10^{-4} ~ 10^{-3}	10^{-5} ~ 10^{-3}	10^{-4}
Ion energy(eV)	0	1 ~ 100	100 ~ 1000	100 ~ 1000	100 ~ 1000	100 ~ 1000
Active Species	Atoms. Radicals	Atoms, radicals, reactive ions	Radicals, reactive ions	Reactive ions	Ar^+ ions	Ar^+ ions
Products	Volatile	Volatile	Volatile	Volatile	Nonvolatile	Nonvolatile
Mechanism	Chemical	Chemical/ Chemical-Physical	Chemical/ Physical	Chemical/ Physical	Physical	Physical
Etch Profile	Isotropic	Isotropic/ Anisotropic	Isotropic/ Anisotropic	Anisotropic	Anisotropic	Anisotropic
Selectivity	30 : 1 – 10 : 1	10 : 1 – 5 : 1	30 : 1 – 5 : 1	10 : 1 – 3 : 1	1 : 1	1 : 1
Resist Compatibility	Excellent	Excellent	Good	Good	Poor	Poor
Device Damage	Little	Little	Some possible	Some possible	Very possible	Very possible
Etch Rate (um/min)	0.1 ~ 0.5	0.1 ~ 0.5	0.05 ~ 0.1	0.05 ~ 0.1	0.02 ~ 0.05	0.02 ~ 0.05
Resolution (um/min)	3	2	1 ~ 2	1 ~ 2	0.5 ~ 1	0.5 ~ 1

Ref: J. D. Lee, "Silicon Integrated Circuit microfabrication technology," 2nd edition {.width=50%

RIE is a sophisticated and complex process where changing a single parameters could impact the total chain of the reaction leading to issues.

DRIE With this method we can obtain an **aspect ratio of 20-50** and the etch rate is around $> 10\mu m/min$.

6 Interconnect

Aluminium has a fairly low melting point at around $577C$. The interconnect and contact Al is done during the same step. But Al has the tendency to fall into the crevices left by the Si that diffuses inside th Al. So add 1% of Si in Al or use barrier material like TiW.

We want to further reduce the contact resistance so we must employ some alloy mixed with Si. We are using the fact that Si diffuses into the metal so then we can remove the non-reacted metal and boom we got some nice salicide.

Electromigration

If the track is not made thick enough, the electrons can take with them some bits of the material and move them further. Creating gaps and increasing the resistance. One solution is to add 4% copper to the mix making the interconnect Al-Cu-Si, 95-4-1.

Interconnect

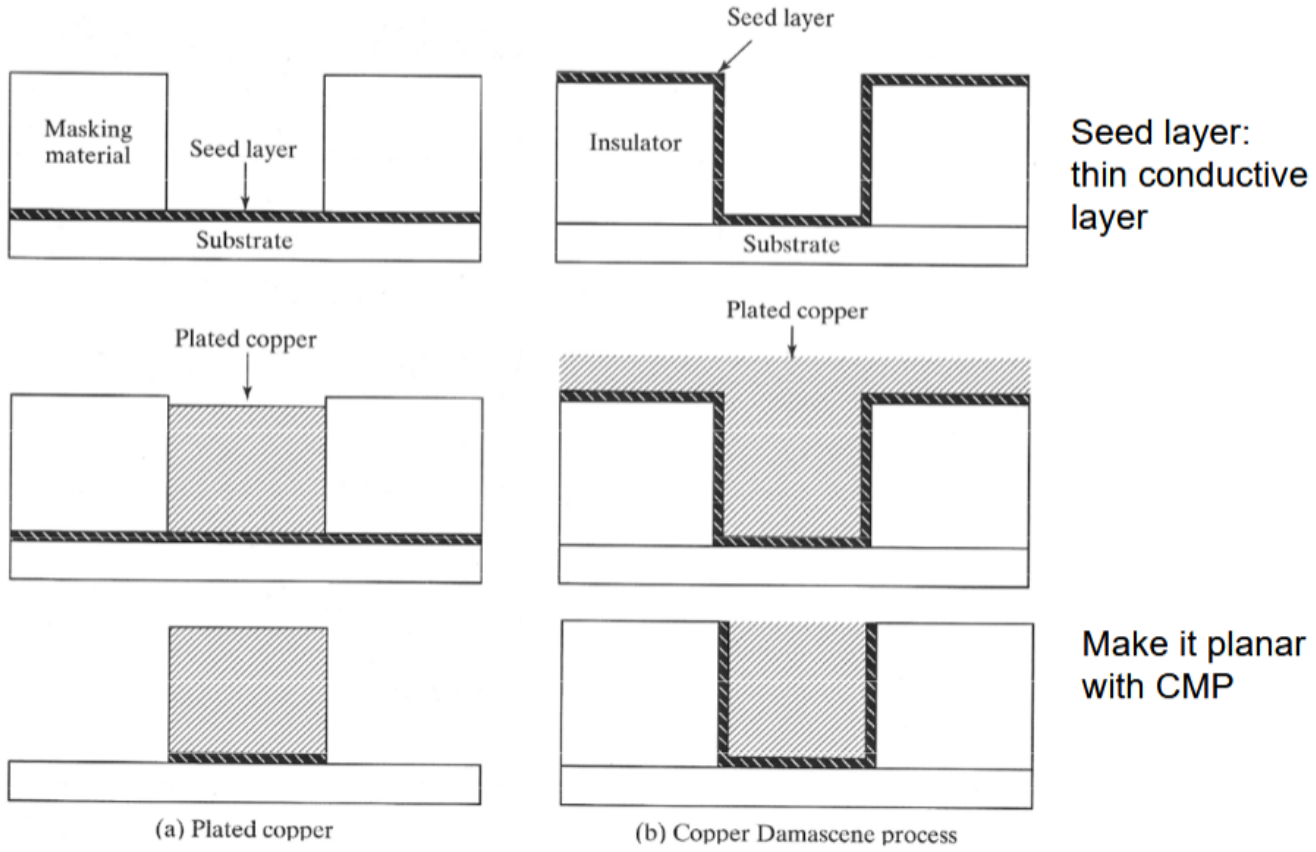
For stack up layer we may be misaligned so we must make the via wider each time as we go up or add some offset.

After making an interconnect we tend to planarize to have a fresh and flat surface to work on. So we will use some CMP process to make everything smooth. Damascene process is based on this idea.

We may need to add some dummy fill oxide to ensure a global planarity after the CMP. Or another technique is using some *reverse tone litho* and already pre-etch oxides that are on top of other stuff and are too wide.

But at some point, Al is not fast enough, too much delay for a small feature size. We had to go for Copper even though it has a high diffusivity. Issue with adhesion, ...

So we have to add a **seed layer** to avoid this diffusion. This seed layer is a thin conductive layer and then we can put the big chunk of copper.



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Dual damascene is used when creating those wider form of via. Good for vias and interconnect traces.

It is often hard to etch metal so we can use lift off where we first apply the photoresist and then the metal. Finally we simply need to etch the mask and everything should come off. Here we want a **bad step coverage**.

7 Ic Processing Overview

up to slide 47

The biggest issue currently is the non-aligning gate. With the Aluminium gate we **can't use some ion implantation** since it is happening above the melting point of the gate. So the process is trickier and same for etching, only low temp process –> mostly isotropic and wet. Good for $> 5\mu m$.

We ditched it to go for some nice polygate, can use fancier process and they are self aligning. Good for $< 10\mu m$.

Al vs poly

Here, we first need to dope the substrate before depositing the gate as we usually go into melting point order. From high to low.

For poly, we first deposit the gate and then dope the wafer. This will make sure that drain and source are already aligned !

Here, we still do some LOCOS operation to isolate our PMOS and NMOS. And then once the base is laid down we can start adding our poly-gate. We apply all the tips and informations we have seen in the course to build a good transistor.

1. *Starting wafer*
2. *Initial oxidation*
3. *N-well photolithography*
4. *Oxide and photoresist etch*
5. *N-well implant oxidation*
6. *N-well implant*
7. *N-well drive-in*
8. *Oxide etch*
9. *Pad oxidation*
10. *Nitride deposition*
11. *Active photolithography*
12. *Plasma nitride etch*
13. *Field implant photolithography*
14. *Field implant*
15. *Photoresist removal*
16. *Field (LOCOS) oxidation*
17. *Nitride and pad oxide etch*
18. *Sacrificial oxidation*
19. *Threshold implant*
20. *Sacrificial oxide etch*
21. *Gate oxidation*
22. *Poly-Si deposition*
23. *Gate definition*
24. *Plasma polysilicon etch*
25. *N^+ S/D photolithography*
26. *N^+ S/D implant*
27. *Photoresist removal*
28. *N^+ anneal*
29. *P^+ S/D photolithography*
30. *P^+ S/D implant*
31. *Photoresist removal*
32. *PSG deposition and densification*
33. *Contact photolithography*
34. *Contact etch*
35. *Metallization*
36. *Metal photolithography*
37. *Metal etch*
38. *Truncate/reflect Nmos*

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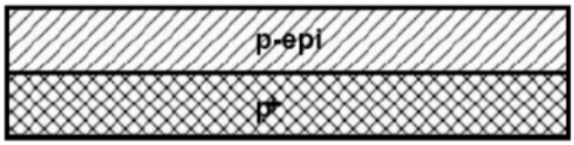
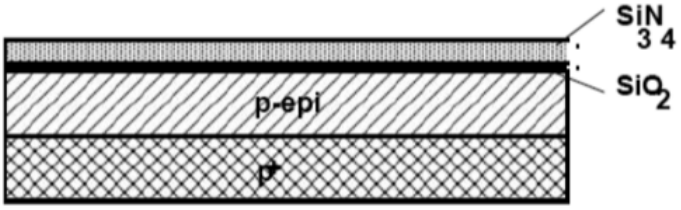
Latch-up issue

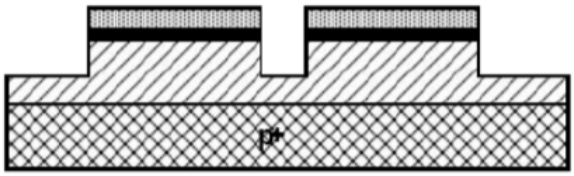
For this, it is important to use some good EPI and STI to avoid any cross connection resulting in a possible *thyristor*.



(a) Base material: p+ substrate with p-epi layer



(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)



(c) After plasma etch of insulating trenches using the inverse of the active area mask

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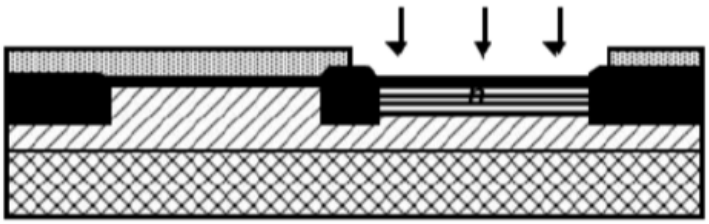
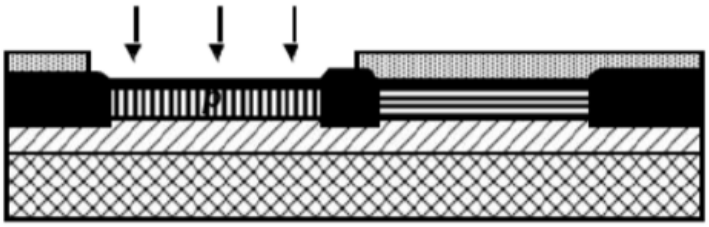
(d) After trench filling, CMP planarization, and removal of sacrificial nitride



(e) After n-well and V_{Tp} adjust implants



(f) After p-well and V_{Tn} adjust implants

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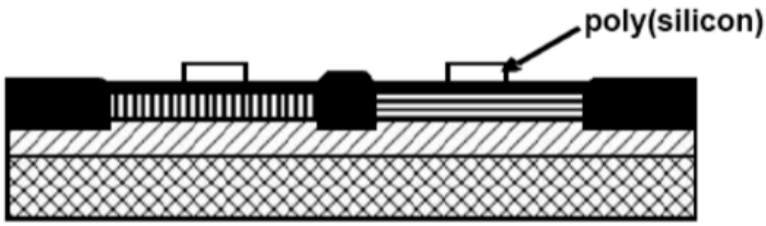
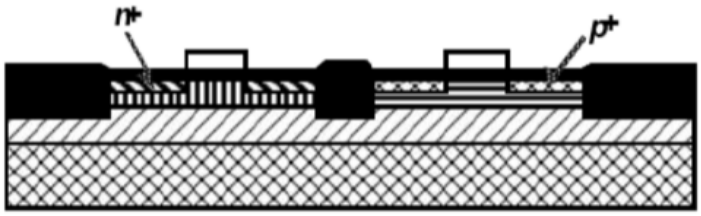
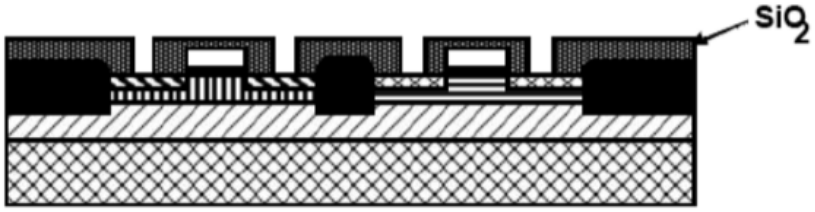


(g) After polysilicon deposition and etch



(h) After $n+$ source/drain and $p+$ source/drain implants. These steps also dope the polysilicon.



(i) After deposition of SiO_2 insulator and contact hole etch.

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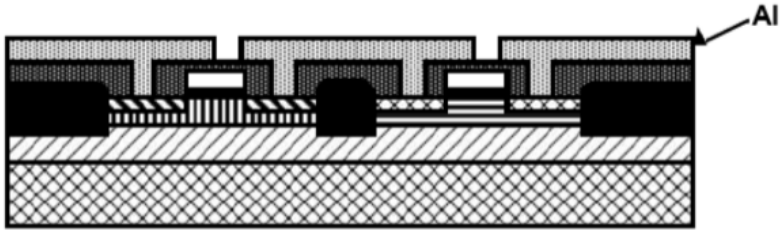
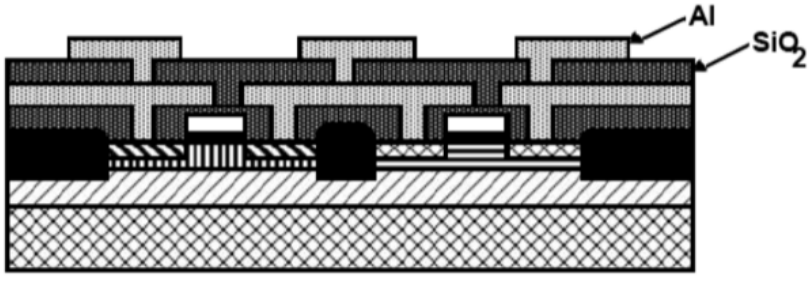


(j) After deposition and patterning of first Al layer.



(k) After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

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Hot carrier effect

TODO

Contacting issues

For this we again use some salacides, by blanket depositing, a bit of the metal will react and simply diffuse. The other non-reacted can be targeted and removed. Contact is now made easy. We usually do some **annealing** to improve the resistivity of the contact.

Gate last Here we first add a dummy gate and at the end att eh contact of the gate using some metal, replacement of poly-silicon.

8 Packaging

Not seen this year.