4.3.1

The latency for the main data path is determined by the blocks needed in every operation which are:

I-mem: 400

Mux * 2: 60ps

Reg: 200ps

Alu: 120ps

D-mem: 350ps

400+200+60+120+350+100=1130ps without the addition of the new alu

and 1430ps with the new alu

4.3.2

The speedup is (1/.95)*(1130/1430) = .832. There is a slowdown since the reduced instruction count is enough to compensate for the latency increase.

4.7

4.7.1

Sign extension: 0000 0000 0000 0000 0000 0000 0001 0100
SL 2 unit: 0001 1000 1000 0000 0000 0101 0000

4.7.2

The aluOp lines for this word instruction would be 00 and the ALU control line would be 0010.

4.7.3

The new pc is pc+4, the path taken is through the adder at the top, then it goes through two multiplexers, the first multiplexer has a control signal of 0 and so does the second multiplexer.

4.7.4

The regDst mux has the value 00010 meaning the register to be written to is $v0. The alusrc mux would output 00000000000000000000000000010100 Which is the offset that will be added to rs in order to calculate the memory address the data will be fetched from. The output of the memtoreg mux

would be the data from the memory address which was calculated from rs+sign ext of the immediate.

4.7.5

The input for the ALU is 1111 1111 1111 1111 1111 1111 1111 1101

and 0000 0000 0000 0000 0000 0000 0001 0100 which is the content of rs and the sign extension of the immediate field. The input for the first adder is pc and 4. The input for the second adder is pc+4 and

0000 0000 0000 0000 0000 0000 0101 0000 which is the result of the sign extension of the immediate field being shifted left twice.

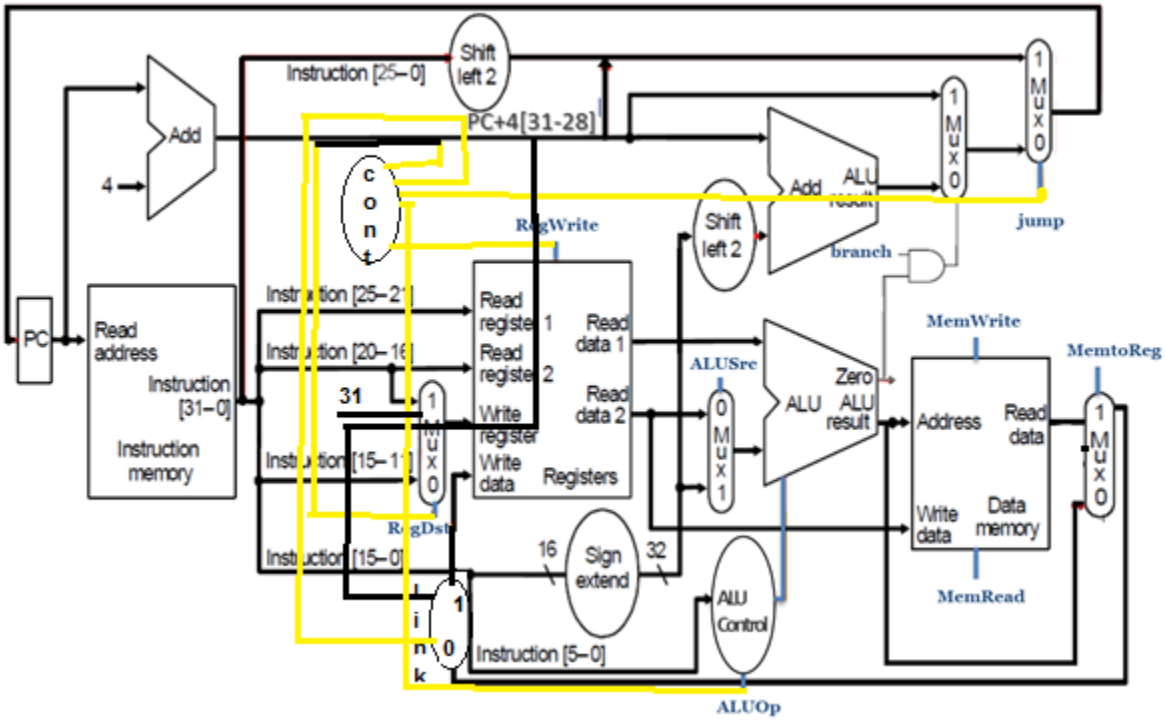
4.7.6

Read register one: 00011 which means read register r3

Read register two: 00010 which means read register r2

Write register: 00010 which means write to register r2

Extra problem:



A) We will use the original datapath and all that needs to be changed is expand the regdst control signal to two bits so that you can add a 3rd input which would be 31 so that the write register can be set to r31. Then a new multiplexer would need to be added in order to change the write data input from the output of the memtoreg mux to pc+4.

B)

RegDst	10
ALUSrc	0
ALUOp	1
MemRead	0
MemWrite	0
MemtoReg	0
RegWrite	1
Branch	0
Jump	1
Link	1

Only one new control signal is needed and that is to indicate the data being written should be pc+4 and not the output of the memtoreg mux. The control signal for RegDst needs to be expanded to two bits so that a 3rd input can be added which 31 which indicates that the write register should be register 31.