Homework Assignment 4 Solution

Exercise 4.3

4.3.1 ***(10 points)***

Clock cycle time is determined by the critical path, which for the given latencies happens to be to get the data value for the load instruction: I-Mem (read instruction), Regs (takes longer than Control), Mux (select ALU input), ALU, Data Memory, Mux (select value from memory to be written into Registers), and Regs.

The latency of this path is 400 ps + 200 ps + 30 ps + 120 ps + 350 ps + 30 ps + 200 ps = 1330 ps.

After improvement, we add 300 ps to the latency of ALU. Knowing that ALU is on the critical path, the overall latency = 1330 ps + 300 ps = 1630 ps.

4.3.2 ***(10 points)***

The speedup comes from changes in clock cycle time and changes to the number of clock cycles we need for the program:

We need 5% fewer cycles for a program, but cycle time is 1630 ps instead of 1330 ps, so we have a speedup of (1×1330)/(0.95×1630) = 0.86,

which means we actually have a slowdown.

Exercise 4.7

4.7.1 ***(5 points)***

Sign-Extend	Jump's shift-left-2
00000000000000000000000000010100	00011000100000000000001010000

4.7.2 ***(5 points)***

ALUOp [1-0]	Instruction[5-0]
00	010100

4.7.3 ***(5 points)***

New PC	Path
PC+4	PC to Add (PC+4) to branch Mux to jump Mux to PC

4.7.4 ***(12.5 points)***

WrReg Mux	ALU Mux	Mem/ALU Mux	Branch Mux	Jump Mux
2 or 0 (RegDst is X)	20	X	PC+4	PC+4

4.7.5 ***(15 points)***

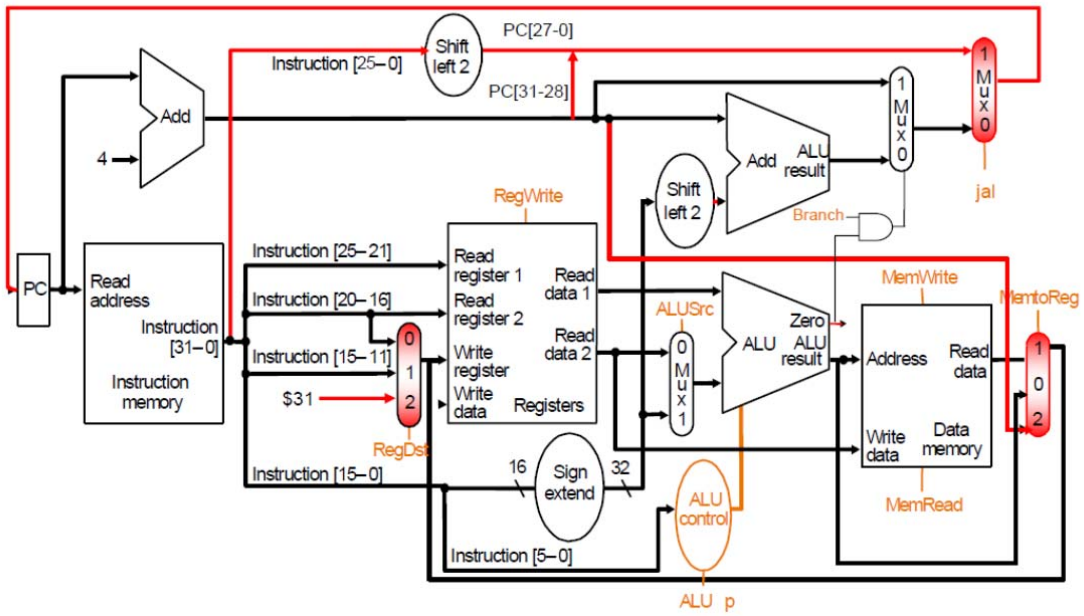
ALU	Add(PC+4)	Add (Branch)
-3 and 20	PC and 4	PC+4 and 20×4

4.7.6 ***(12.5 points)***

Read Register 1	Read Register 2	Write Register	Write Data	RegWrite
3	2	X (2 or 0)	X	0

<u>Extra Exercise</u> (15 points)

a) The additions are shown in the following figure.
- a new control signal (jal) will be added to the control unit.
- a new mux is added to the path that will control whether the PC is updated with the jump address or not.
- The mux that controls the write register address must be extended to include the hard coded value of 31 (the return address register). The control signal for this mux is increased by 1 bit.
- The result of PC+4 must be input to the mux that selects the data to write to the register. The control signal for this mux is increased by 1 bit.



b)

RegDst	10
ALUSrc	X
ALUOp	X
MemRead	0
MemWrite	0

MemtoReg	10
RegWrite	1
Branch	X
Jump or jal	1