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ECE 153A  
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## **Lab 1a - Starter Lab Report**

### **Purpose and expected goals of the lab**

The first portion of the lab helped us familiarize ourselves with the Vivado and Xilinx software. The coding portion helped us understand how to program software onto the FPGA board and run timed instructions with interrupts enabled.

### **Methodology**

Operating each of the following tasks in iterations of 5, 15, 25, and 40 loops. We assume that 1000 trials is sufficient to display the timing of each task described below.

1. Timing of addition using integers
2. Timing of addition using floating point
3. Timing of writing the LEDs to turn on or off
4. Timing of reading a word from the DDR2 memory at a random location
5. Timing of writing to the USB Port
  - a. Write a floating point number
  - b. Write a string of 10 characters

### **Results**

**Link to the video:**

**Graphs:** for the graphs the x-axis represents the number of events in the simulation, and the y axis is the timing given in the code.

## 1. Regression and Overhead

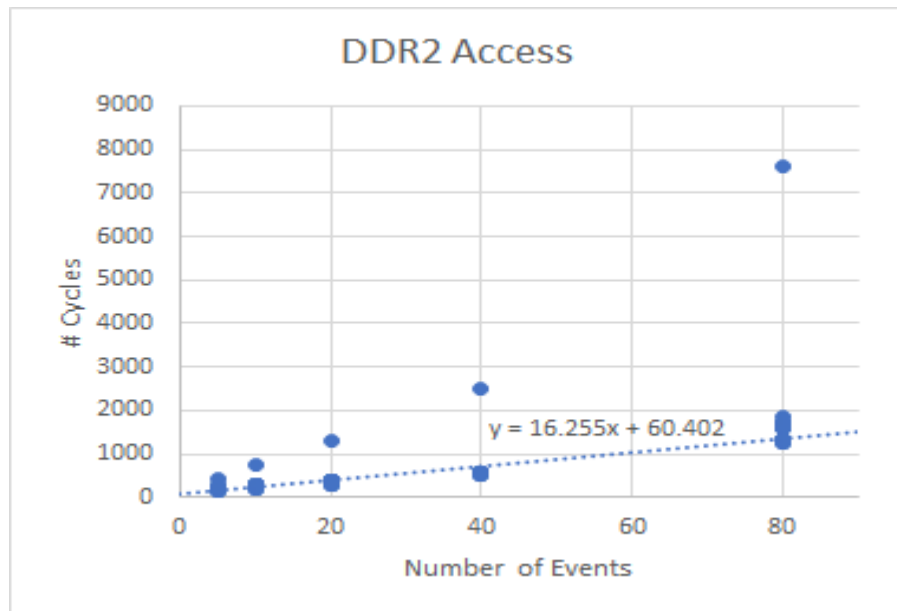


Figure 1. DDR2 linear regression with

## 2. Histograms of measurement data

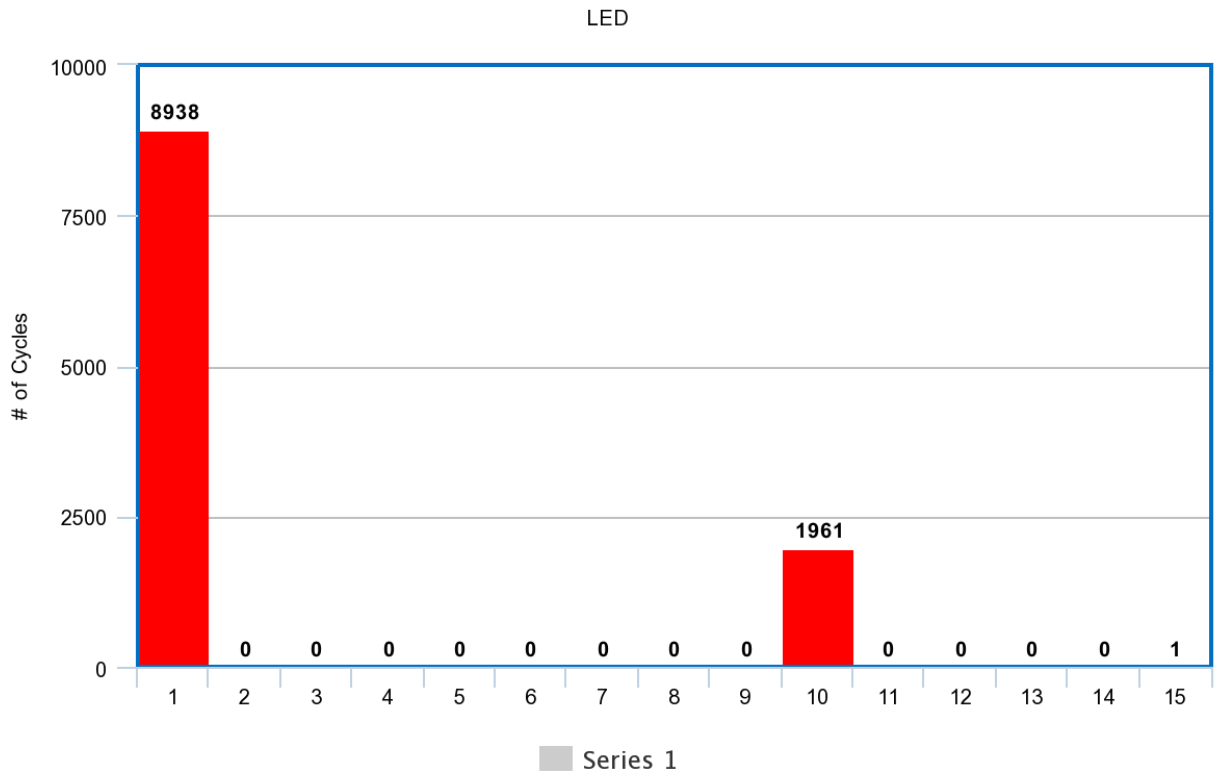


Figure 2. Histogram of LED (Min Bin: 75, Max Bin: 405, Bin Size:22 )

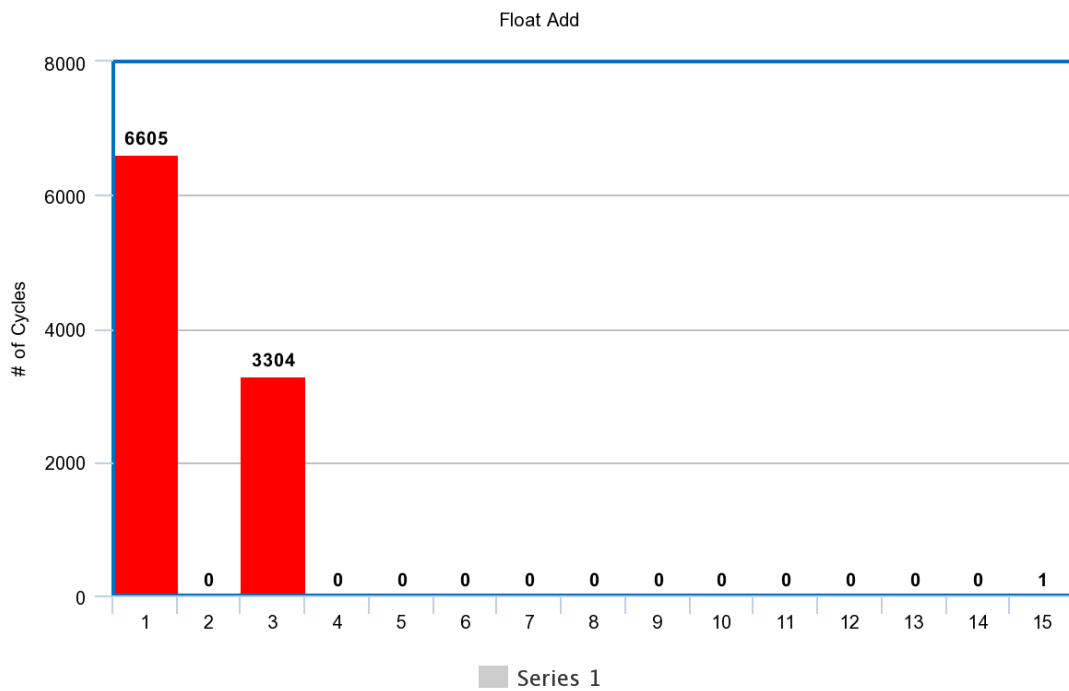


Figure 2. Float Add (Min Bin:219 , Max Bin:2132 , Bin Size: 127)

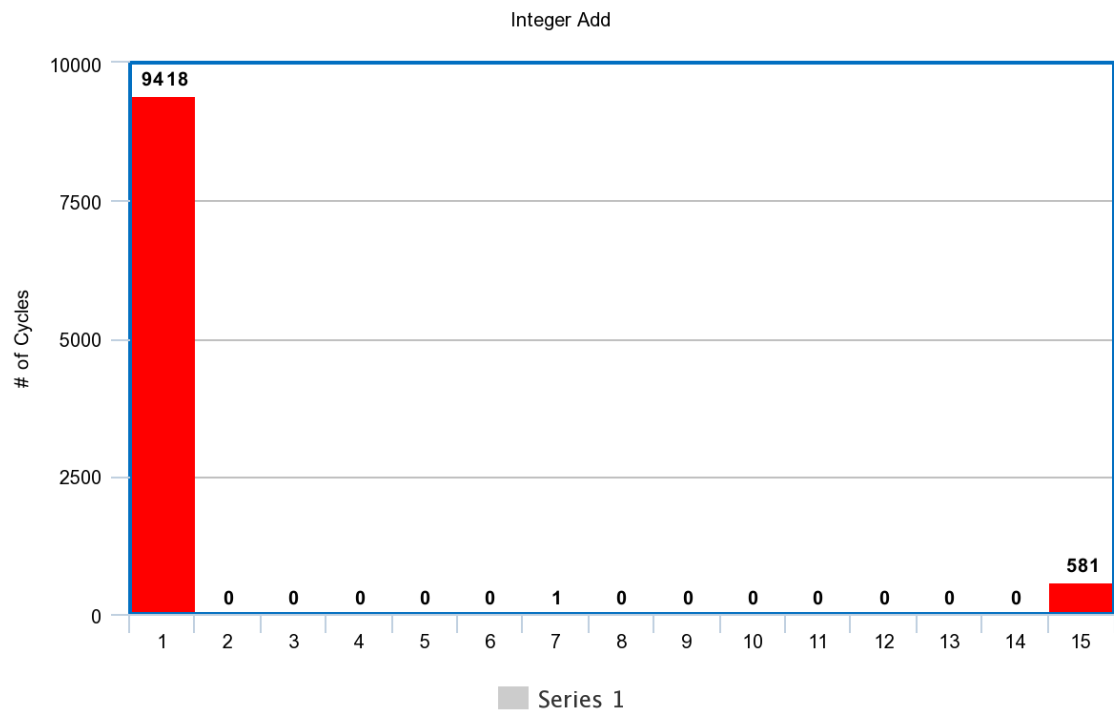


Figure 2. Integer Add (Min Bin: 39, Max Bin: 369, Bin Size: 22)

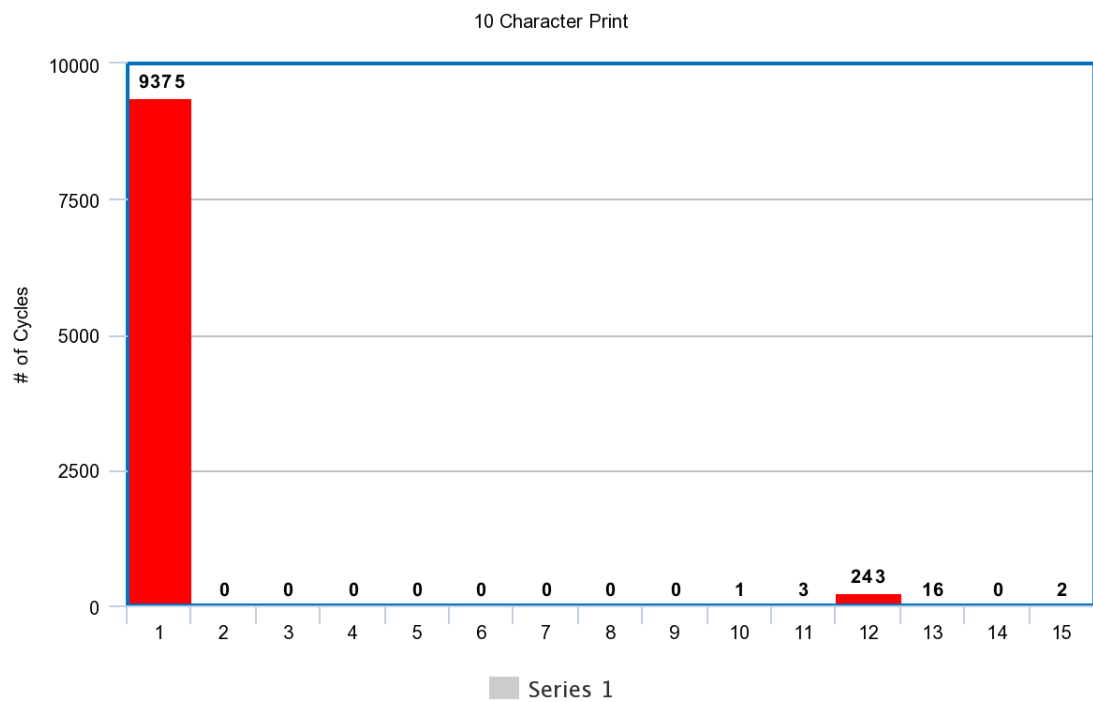


Figure 2. Histogram of 10 Character Print(Min Bin: 1053, Max Bin: 6773013, Bin Size:451464 )

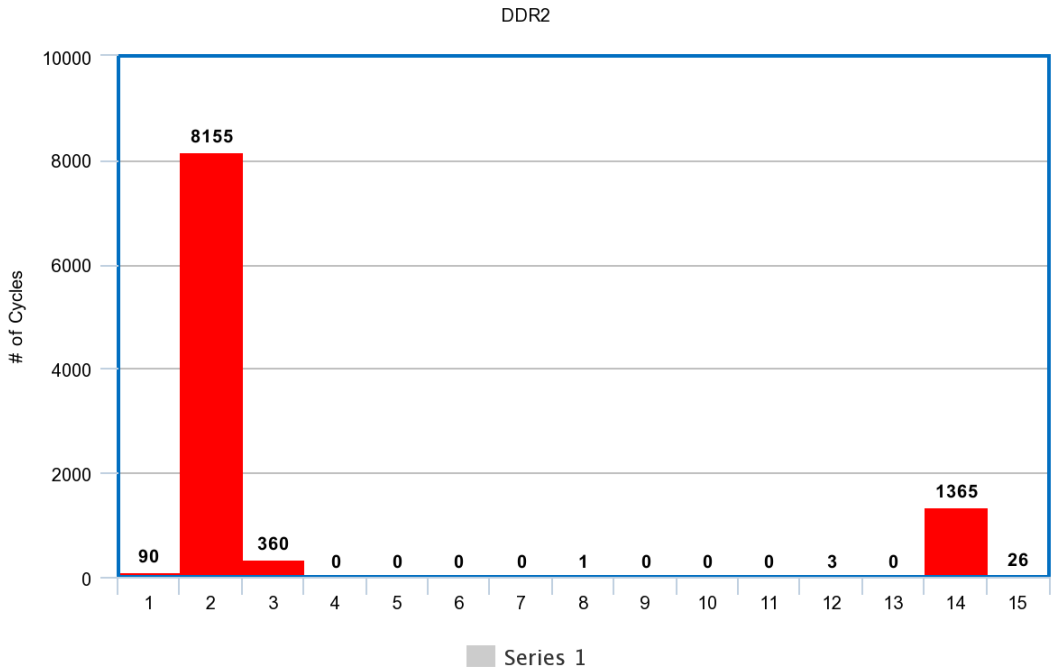


Figure 2. Histogram of LED (Min Bin: 43, Max Bin: 628, Bin Size: 39)

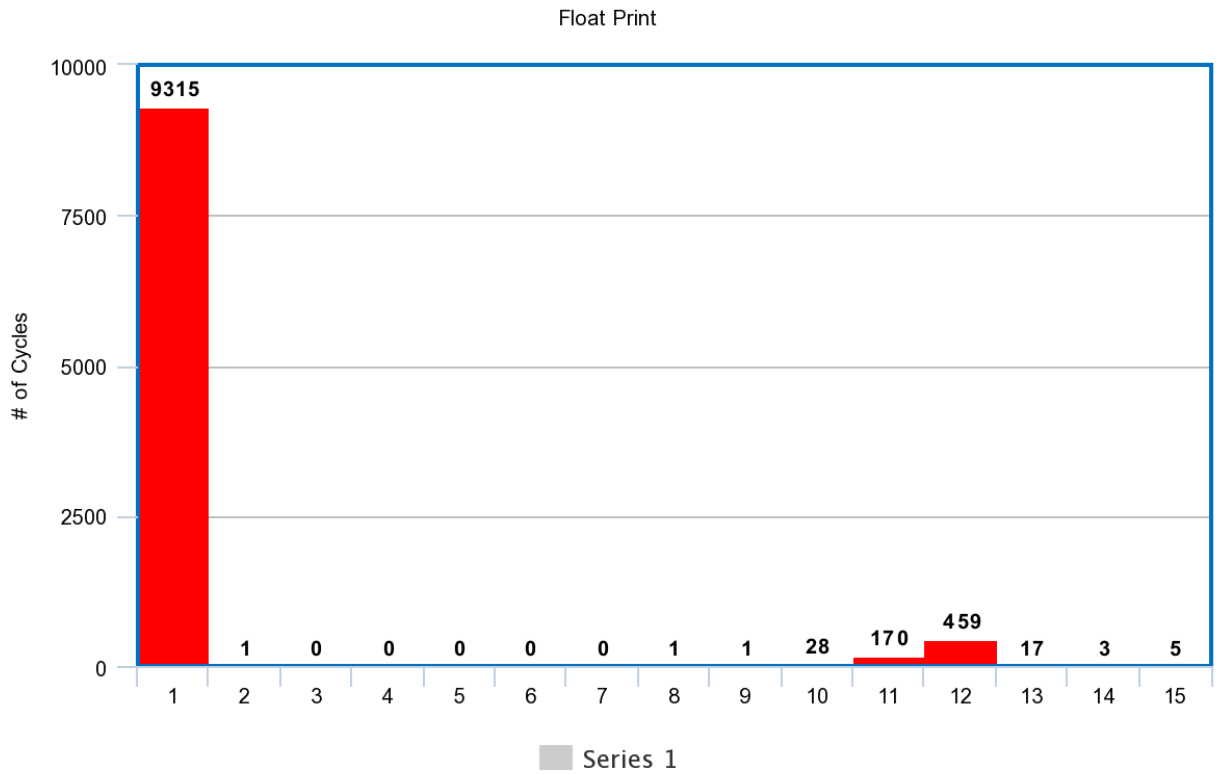
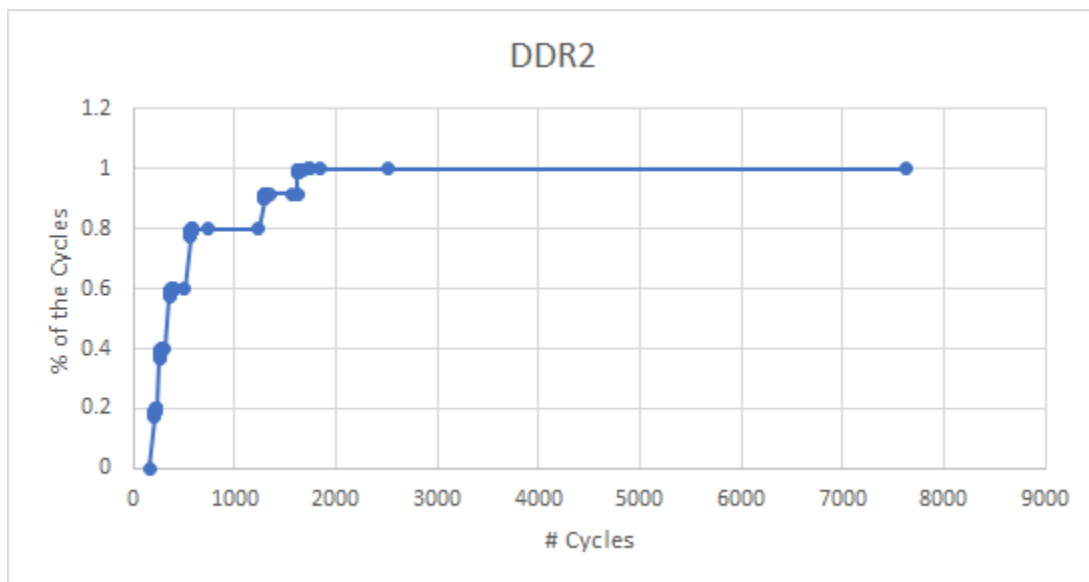
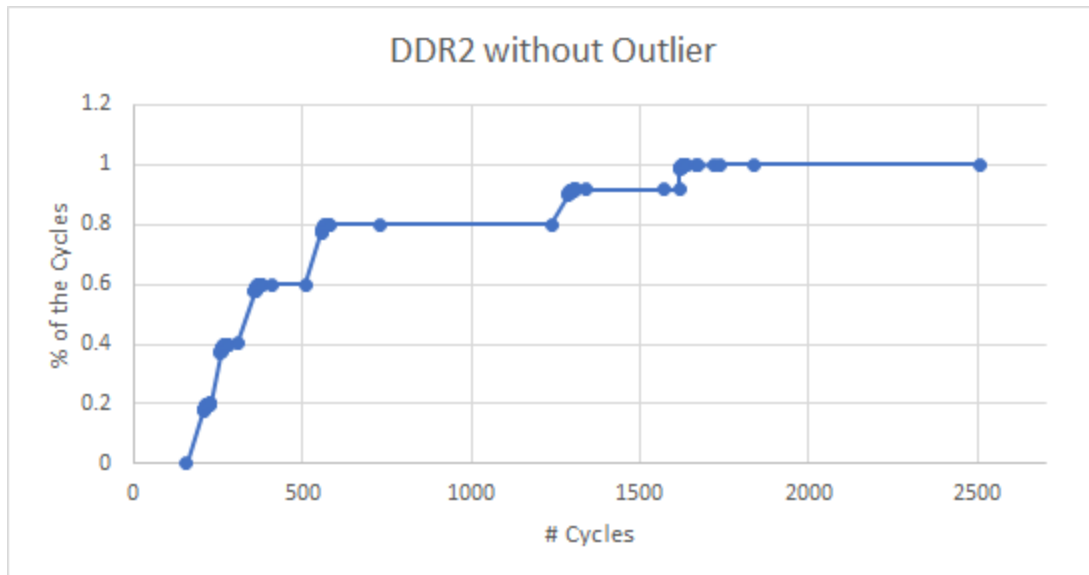


Figure 2. Histogram of LED (Min Bin: 36109, Max Bin: 7991238, Bin Size: 530341)

### 3. CDF for DDR access timing





The confidence interval can be estimated to be around 175 - 1500 cycles.

4. The magnitude of measured values and timing uncertainties can be viewed in the table below. Integer addition was the fast time per event task that was performed in this lab. LEDs took roughly 3 times longer than integer addition, and float addition was about 10 times longer. Printing float and integer addition to the terminal was by far the longest time.

Integer Addition			
N:	sum	avg	t per event
5	2060407	206	41
15	4899569	489	32
25	7738423	773	30
40	11977726	1197	29
Float Addition			
N:	sum	avg	t per event
5	16017298	1601	320

15	46705816	4670	311
25	77444117	7744	309
40	123509030	12350	308
<b>LED</b>			
N:	sum	avg	t per event
5	4734240	473	94
15	12949147	1294	86
25	21136341	2113	84
40	33451605	3345	83
<b>DDR2</b>			
N:	sum	avg	T per event
5	3113908	311	62
15	6563867	656	43
25	10018227	1001	40
40	15193116	1519	37

Note: We did not include the events, printing float and 10 character word due to high discrepancy.

5. We had a few outliers in our data. This can be easily viewed in figure 1, where some data points are magnitudes larger than the majority of the data points.