

Vulnerabilities in Test Infrastructures

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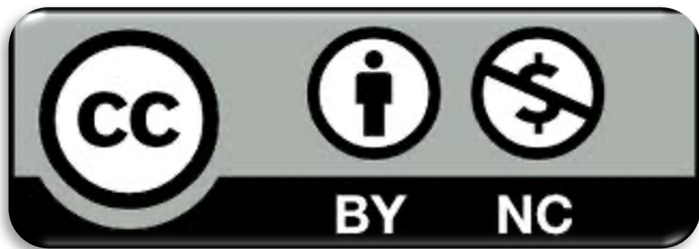
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Goal

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- Presenting:
 - some of most significant vulnerabilities introduced by test infrastructures
 - some possible attacks exploiting them.

Prerequisites

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➤ Lectures:

- *CS_1.4 – Vulnerabilities*
- *HS_1.1 – The role of Hardware in Security*
- *HW_S_0.7.1 – Hardware Testing -- Basic concepts*

Outline

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- Introduction
- Test Infrastructure based attacks
 - Scan chains
 - Standard IEEE 1149.1
- Fault attacks
 - ATPG

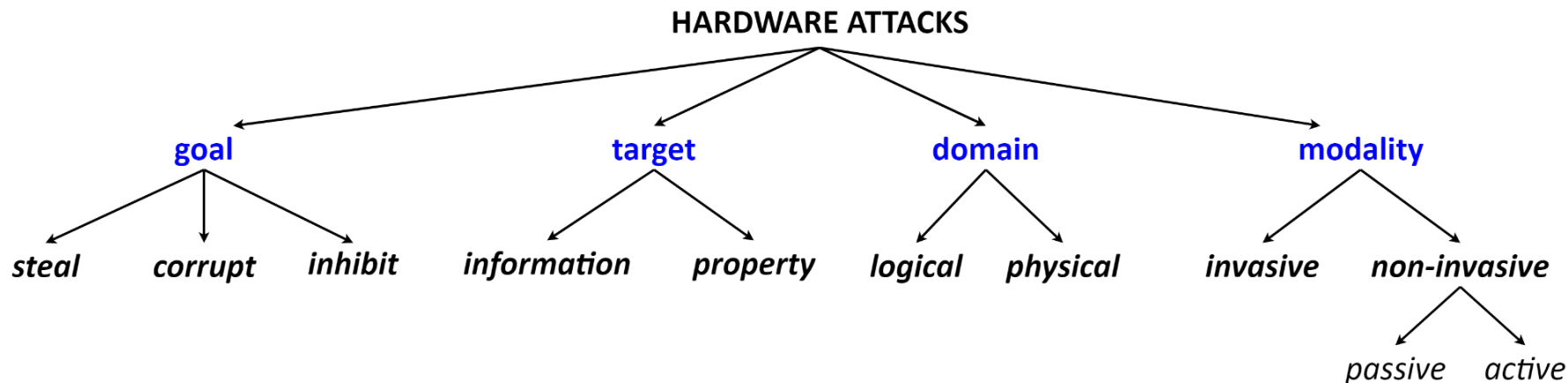
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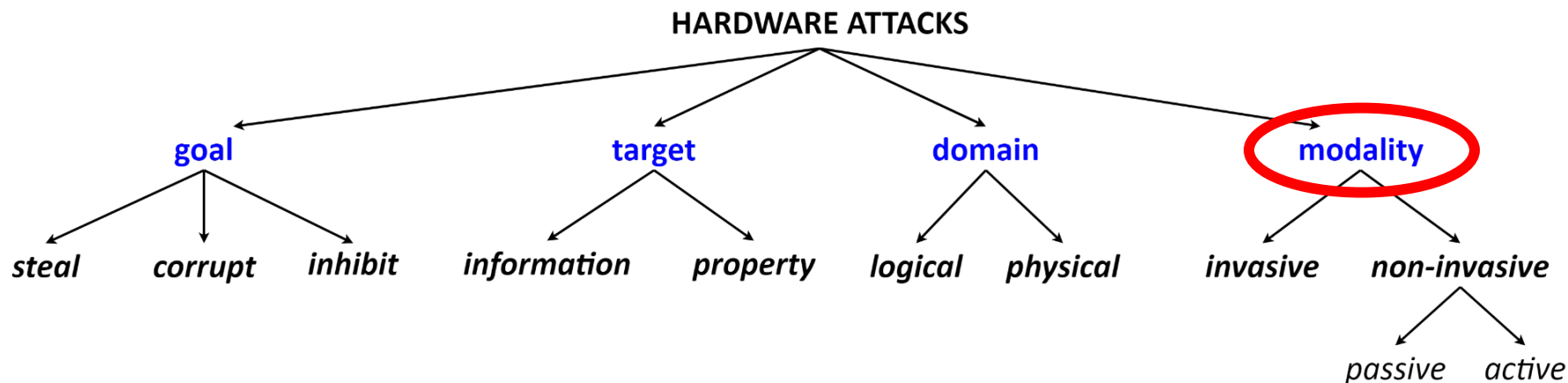
Hardware Attacks Taxonomy

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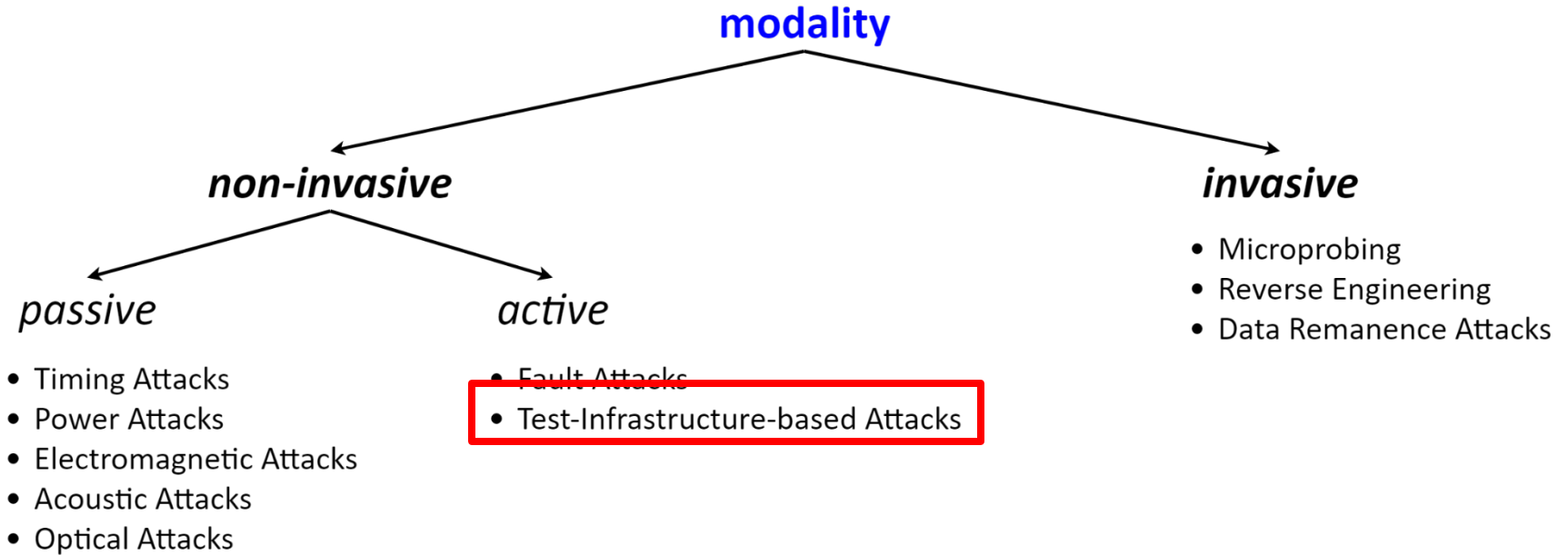
Hardware Attacks Taxonomy

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Hardware Attacks Modalities

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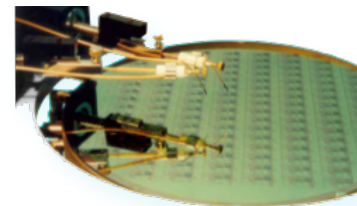
Unprotected Test Infrastructures can Jeopardize
the Security of the Entire System

Test vs Security



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- Testing is mandatory to guarantee high quality of digital ICs
 - Increase controllability and observability
- On the contrary, security fears testability
 - Test infrastructures used for attacks



Do we need to test secure circuits?

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- Of course, yes!
- In general, we have to guarantee high quality
- In particular, a defective secure device may jeopardize the overall security

Potential Avenues of Attack

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- Among the plethora of test infrastructures, in the sequel we focus on
 - Scan chains
 - Standard IEEE 1149.1
 - JTAG infrastructures
 - ATPG

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Issues

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- In scan-based devices, the scan chains could provide a natural way to access the content of ALL the storage devices (flip-flops and registers) connected to a scan chain
- Thus, potentially scan chains can contain a secret (directly or indirectly):
 - Directly: the secret key itself
 - Indirectly: a value that is a function of the secret key (e.g., an intermediate value during the encryption process)

Scan-based attacks

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- Goal: Retrieve embedded secret data
- HOW: Exploit observability and controllability offered by scan chains
- Principle: toggle the circuit between functional and scan modes

Red Teaming

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- In some architectures, scan chains could:
 - Be hidden
 - Be accessible just via additional infrastructures, such as 1149.1 cells
 - Be managed via complex Scan compression Codec

<https://www.youtube.com/watch?v=BTm9ExW5cLg>

<https://semiengineering.com/scan-compression-is-no-longer-about-compression/>

Red Teaming – Vulnerability exploitations

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1. Identify the target FFs that contain the secret to be stolen
2. Identify the scan chain SC to which the target FFs belong
3. Identify the precise time instant T in which the target FFs contain the secret.

Red Teaming – Vulnerability expl

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1. Identify the target FFs that are stolen
2. Identify the scan channels that belong
3. Identify the precise time when target FFs contain the

CAVEAT

All these tasks could be made harder by the introduction of obfuscation solutions during the design phase

Red Teaming – Vulnerability exploitations

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4. Run the circuit in *Normal mode* until the time T
5. Stop the circuit and switch it to *Test mode*
6. Scan out the content of the scan chain SC until the content of all the target FFs reach an output point you can observe

Red Teaming – Vulnerability expl

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4. Run the circuit in No
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content of all the targ
you can observe

CAVEAT

*In recent full-scan
designs, test
decompressors and
compressors are
very often exploited*

Red Teaming – Vulnerability exploitations

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4. Run the circuit in *Normal mode* until the time T
5. Stop the circuit and switch it to *Test mode*
6. Scan out the content of the scan chain SC until the content of all the target FFs reach an output point you can observe
7. If Test decompressors and compressors are present, you have to previously reverse them.

Blue Teaming

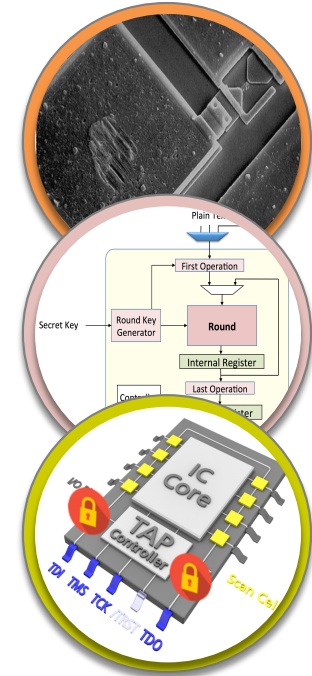
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- *Never let the scan chains freely accessible from the circuit pins !!*

Blue Teaming

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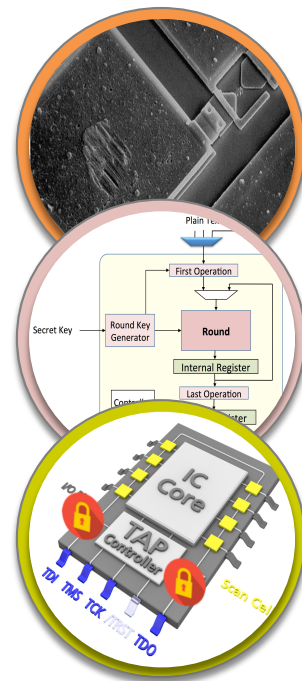
- Several countermeasures have been proposed, including:
 - Leave the scan chain unbound
 - Built-In Self-Test
 - Secure Test Access Mechanism
 - Scan Chain Encryption



Blue Teaming

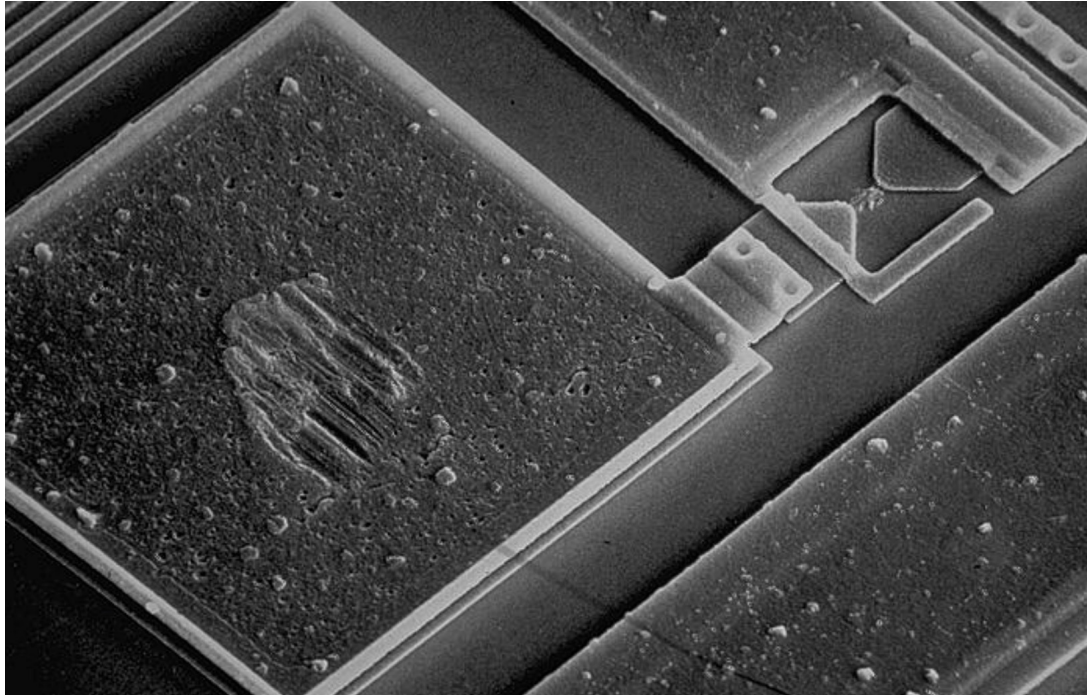
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Fuses

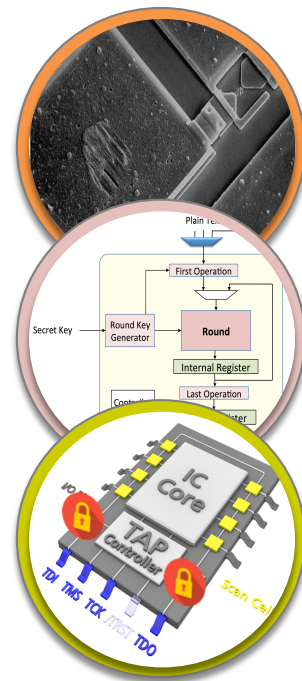
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Blue Teaming

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- Several countermeasures have been proposed, including:
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Built-In Self-Test (BIST)

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- When possible, replace Scan Chains by BIST solutions.

Built-In Self-Test (BIST)

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Pro's

- Avoid scan-based testing
- Allow at-speed testing
- Reduced ATE costs

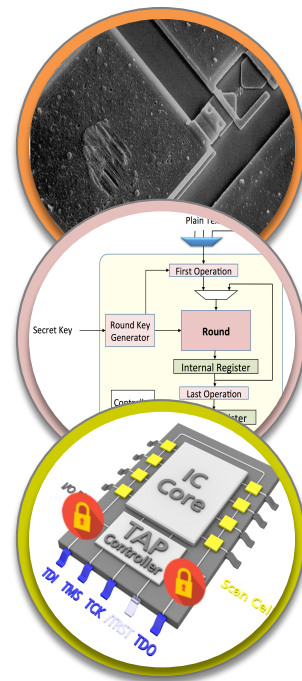
Con's

- Area overhead
- Fault coverage
- Diagnosis

Blue Teaming

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- Several countermeasures have been proposed, including:
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Secure Test Access Mechanism

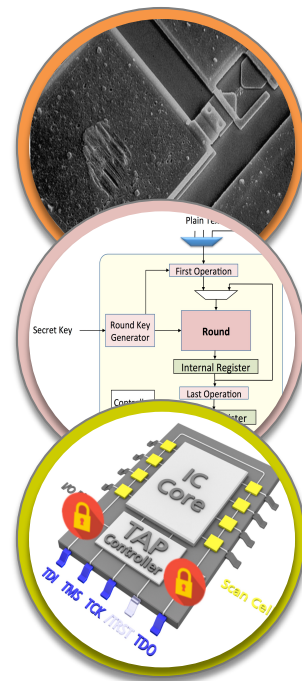
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- Drawbacks:
 - Authentication (expensive)
 - No in-field debug/diagnosis
 - Not easy to integrate in design flow

Blue Teaming

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- Several countermeasures have been proposed, including:
 - Leave the scan chain unbound
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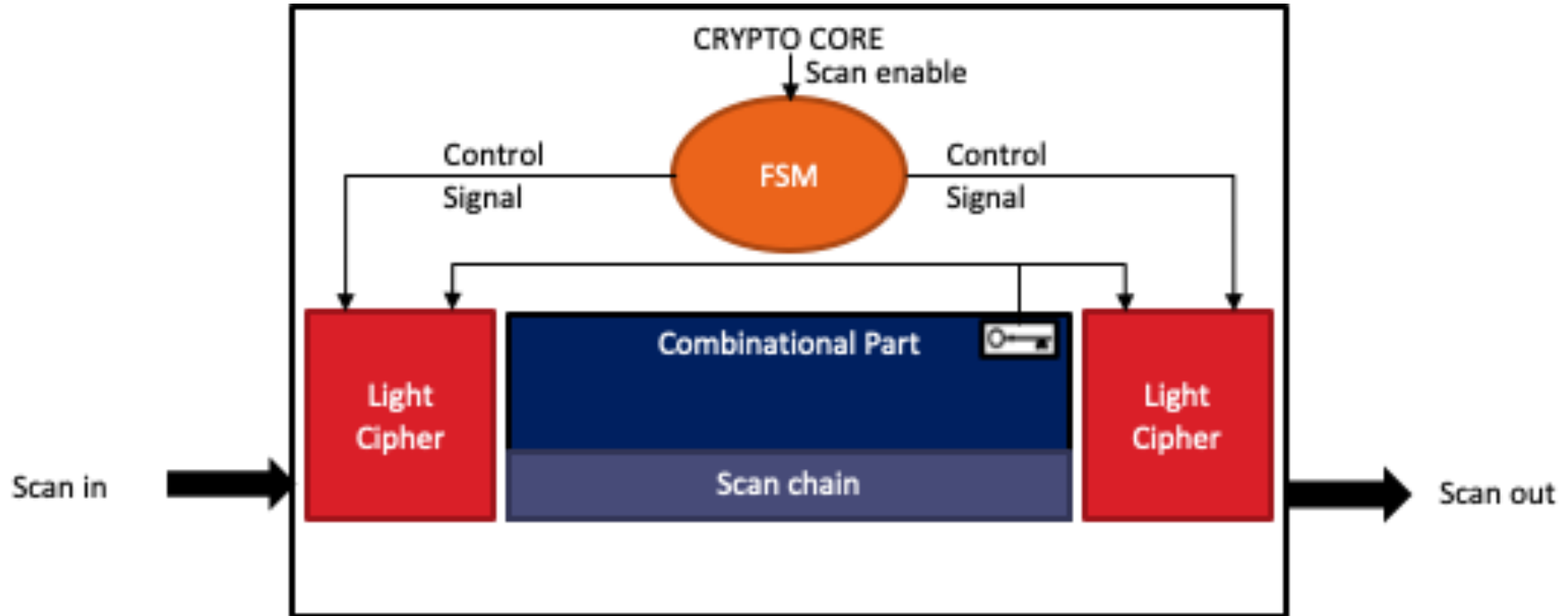
Scan Chain Encryption

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- Encrypting scan chain content with a secret key
- Controllability and the observability:
 - Untouched if the secret key is known
 - Impossible to control or observe otherwise
- Constraints:
 - To modify the test vector and response offline

Architecture of a Scan Chain Encryptor

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Red Teaming

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- In 1149.1 compliant architectures, the Boundary Scan infrastructure may implement proprietary (or hidden) instruction(s) whose execution could enable you to access the internal scan chains.

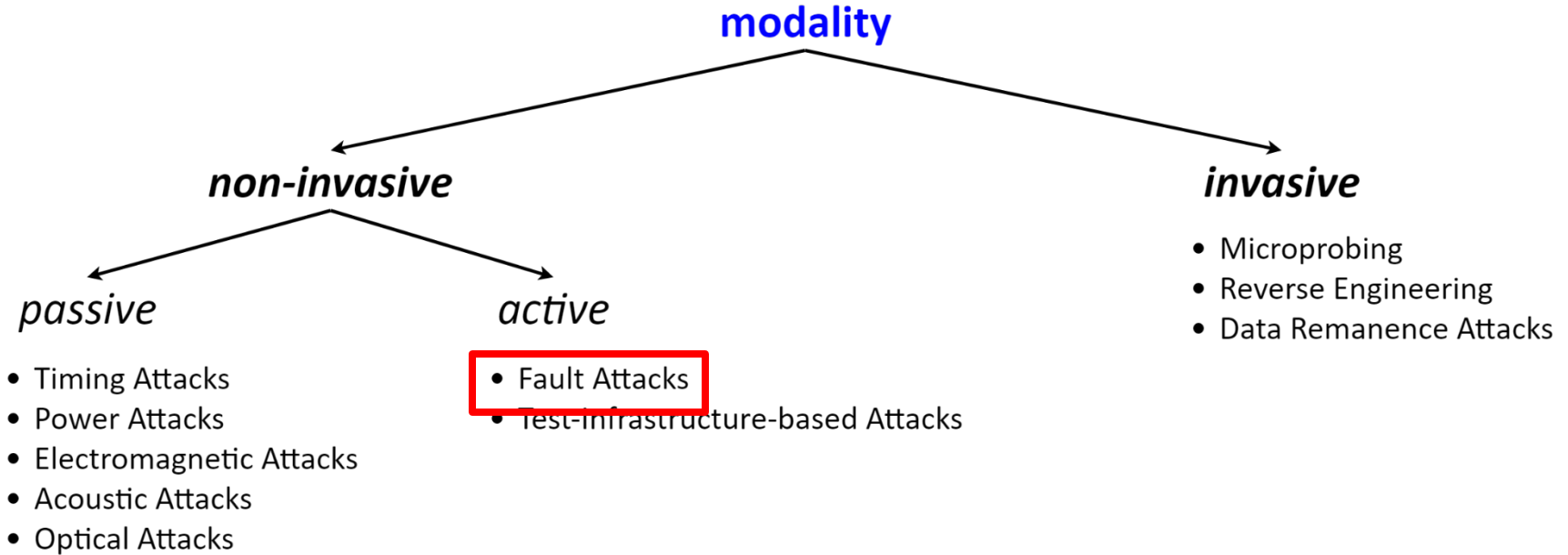
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- **Fault attacks**
 - **ATPG**

Hardware Attacks Modalities

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Conclusions on Testing

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- Test of Secure devices is critical
- Test of Secure devices is possible (at higher costs)
- Nothing is perfect, solutions should be improved based on coming attacks!

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