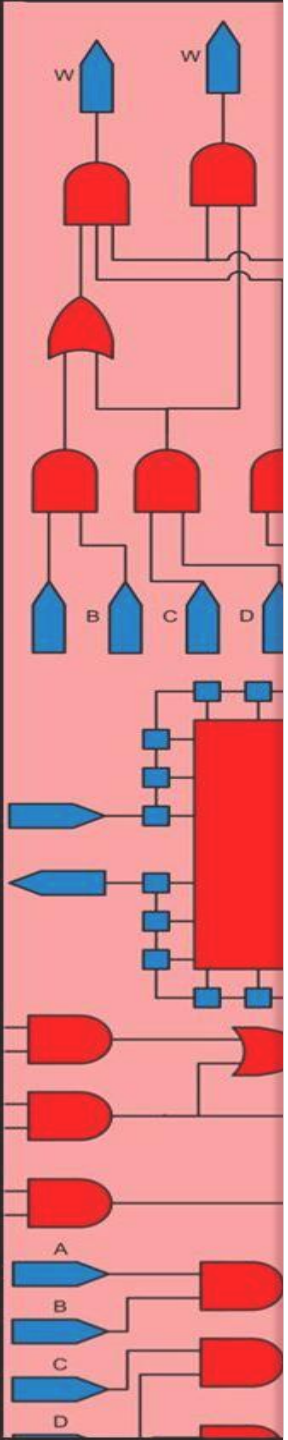
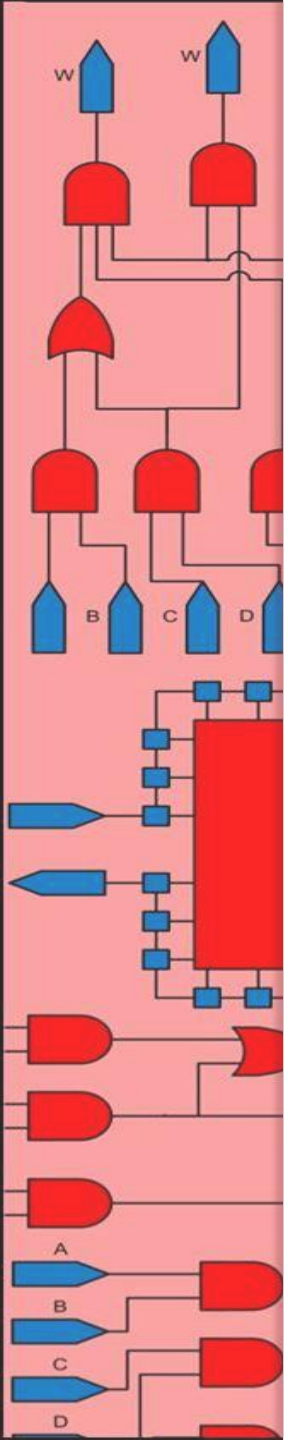


Course on Details of Hardware of Processors (Processors)

VHDL Design and Implementation of an Instruction Set Architecture

Zain Navabi

Slides prepared by Katayoon Basharkhah



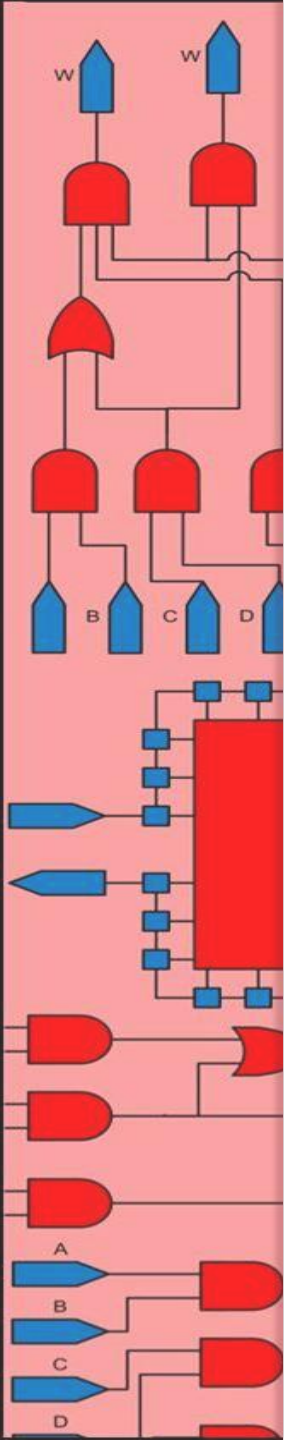
Topic 2

Memory Models

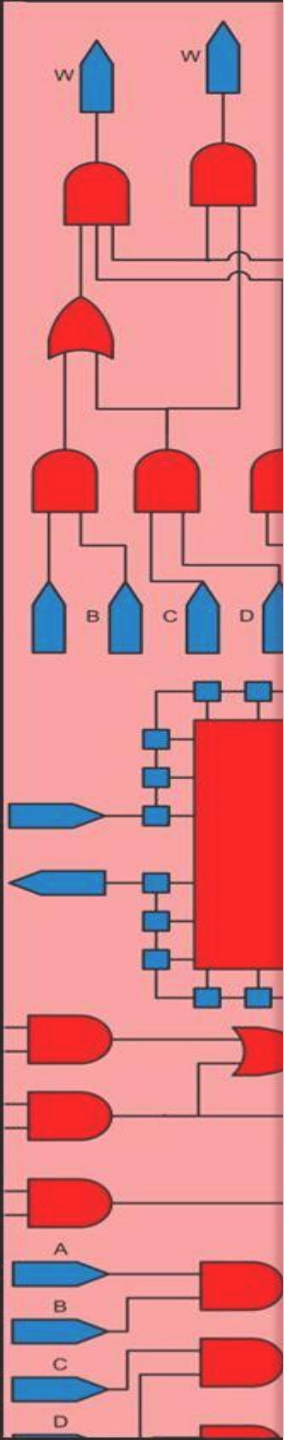
Zain Navabi

Slides prepared by Katayoon Basharkhah

Course Roadmap



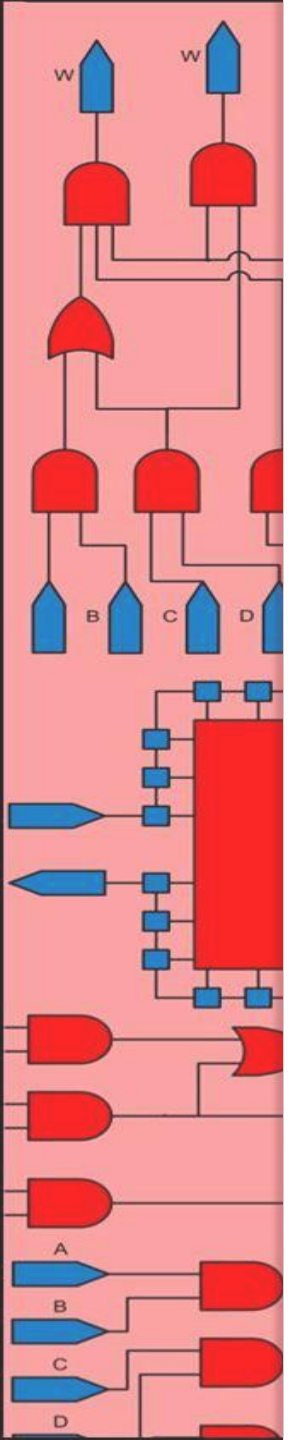
	Topic 1	Topic2	Topic 3	Topic 4
Goals	A Processing System	Memory Model	Processor Devices	Processor Architecture
	Embedded System Introduction	Peripheral Hardware		Show Case ISA
Contents	•CPU •Instructions •Memory-Map •Memory •I/O device	Different memory structures Memory mapping in the bussing and devices' communications.	• Address Logic • Data Registers • Handshaking • Interrupt	• SAYAC Instructions • Datapath Design • Controller Design • Simulation and FPGA Synhesis
	Introduction to processor-based system, general concepts and different components of the system	•SDRAM •ROM •SRAM		A sample processor named SAYAC. Processor internal architecture starting form the processor instruction set and coming down to the all RTL components of the processor datapath and controller.



Memory Models

Learning Outcomes:

- *Learn* different types of memory
- *Learn* memory stages in embedded system
- *Learn* memory interface



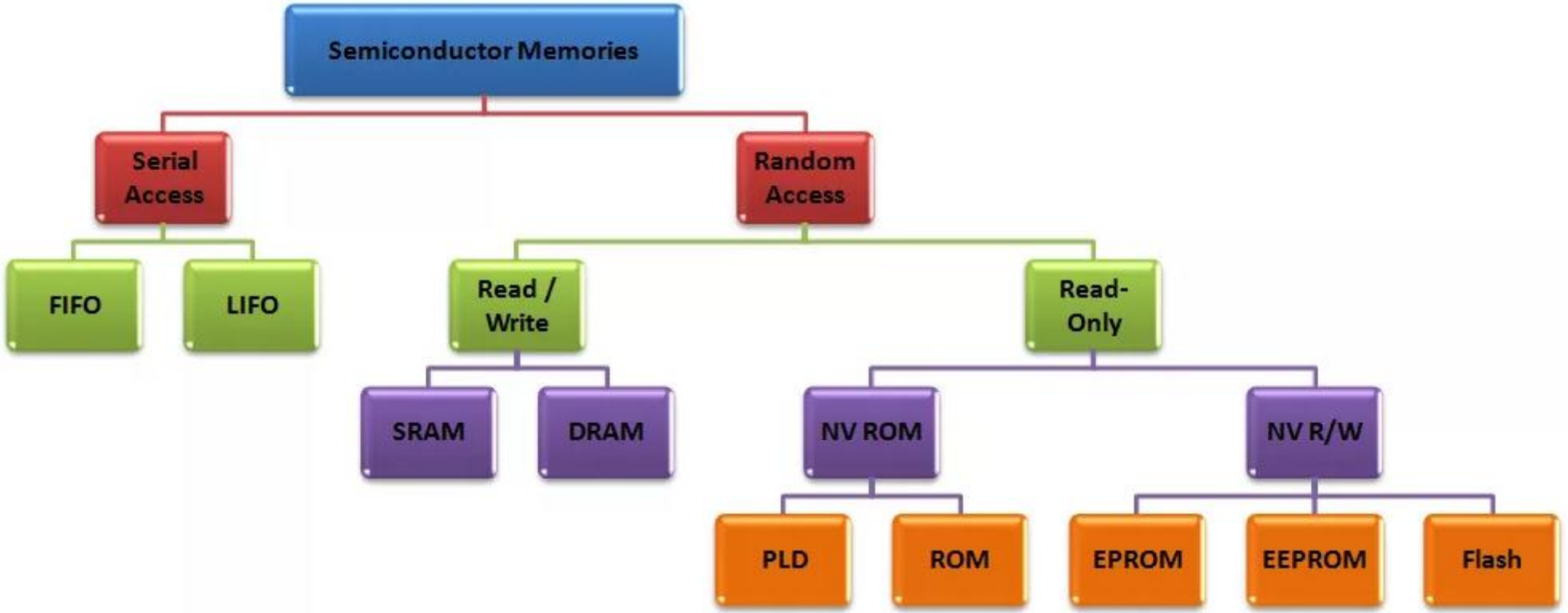
Memory Models

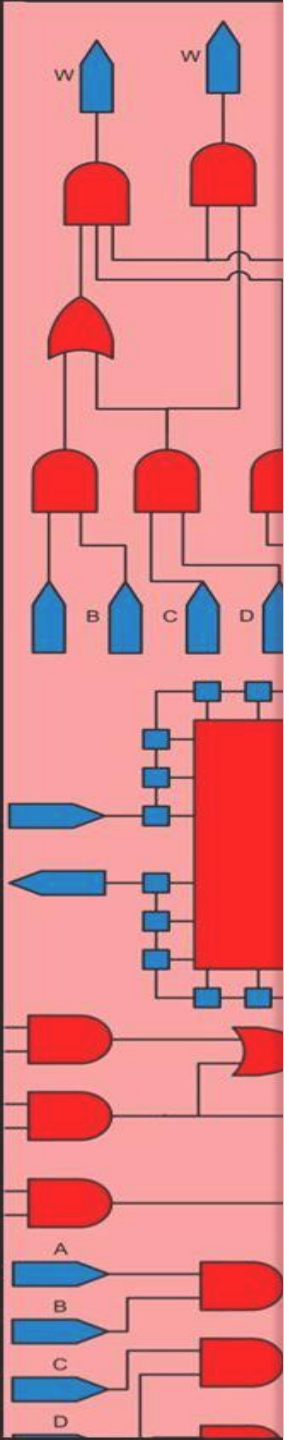
Outline:

- Memory Types
- Memory Stages in Embedded Systems
- Memory Handshaking
- Memory Mapping

Memory Models

Memory Types





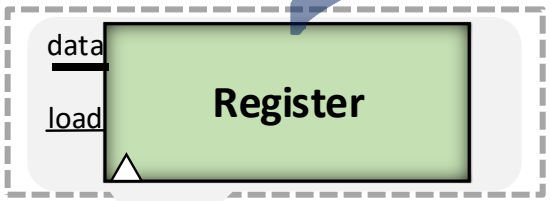
Memory Models

Memory Stages in Embedded Systems

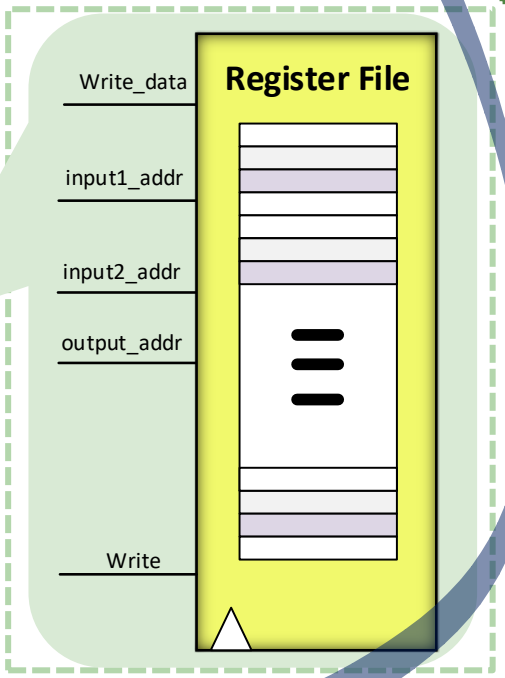
- Discrete Registers
- Register File
- On-chip / Closely-Coupled / Scratch Pad Memory
  - SRAM
- Main Memory
  - DRAM

Memory Models

Memory Hierarchy in Embedded Systems



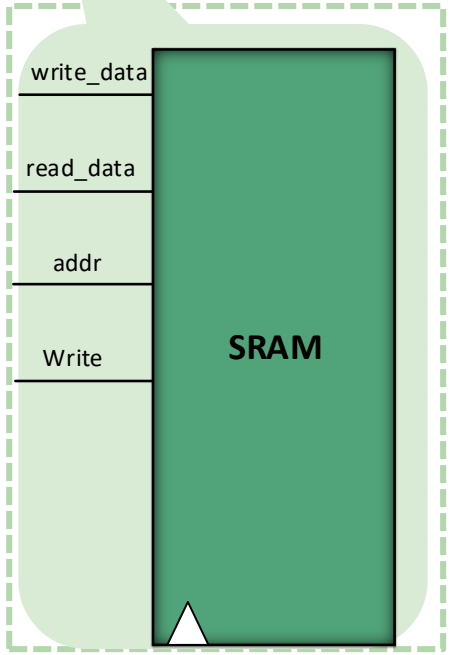
Does not scale well as we deal with larger amounts of data



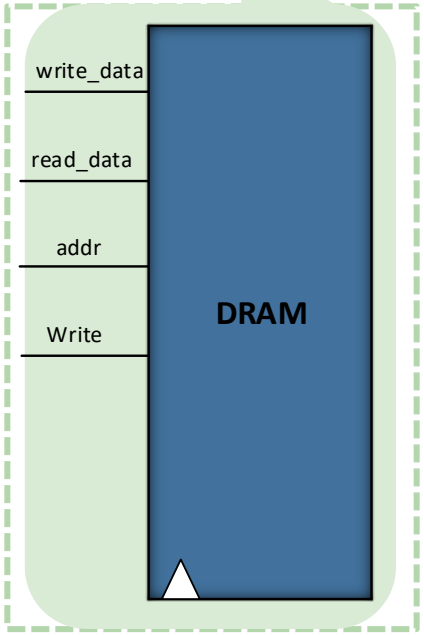
handling the complexity involving the storage and retrieval of large amounts of data

Unable to simultaneously access all data

SRAMs can accommodate hundreds of kilobytes of on-chip storage



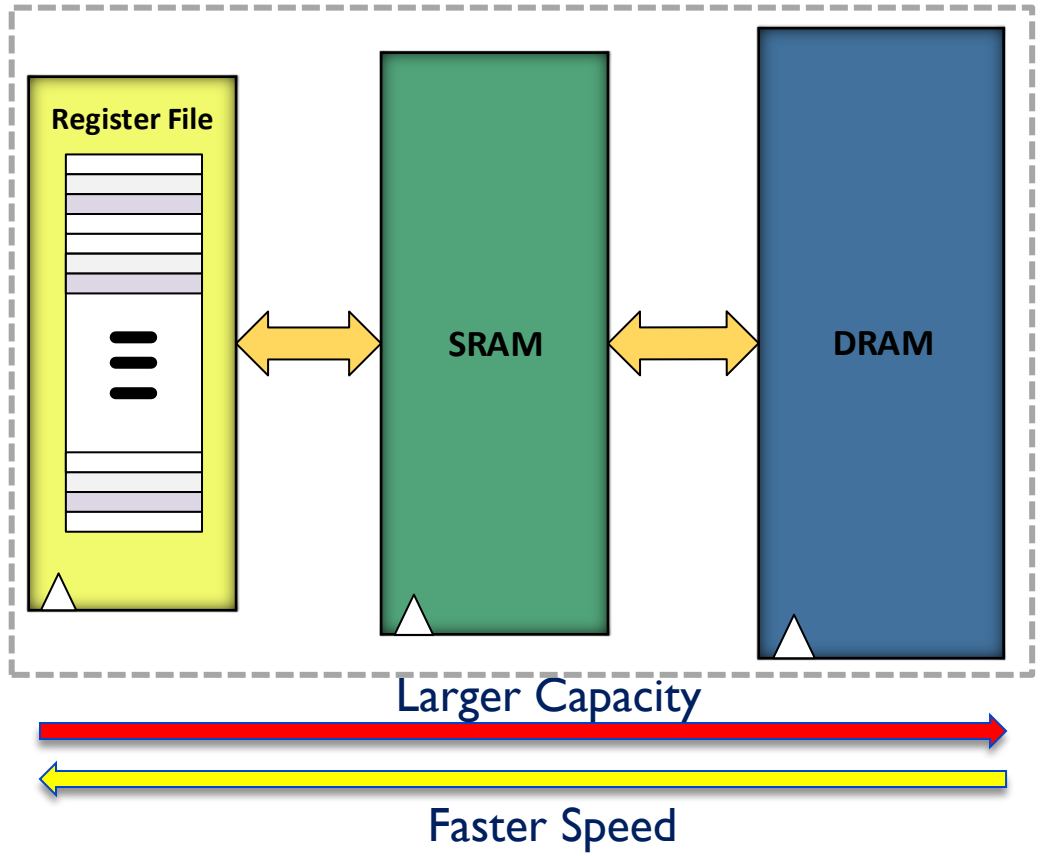
Higher capacity and correspondingly higher access times



Memory Models

Memory Stages in Embedded Systems

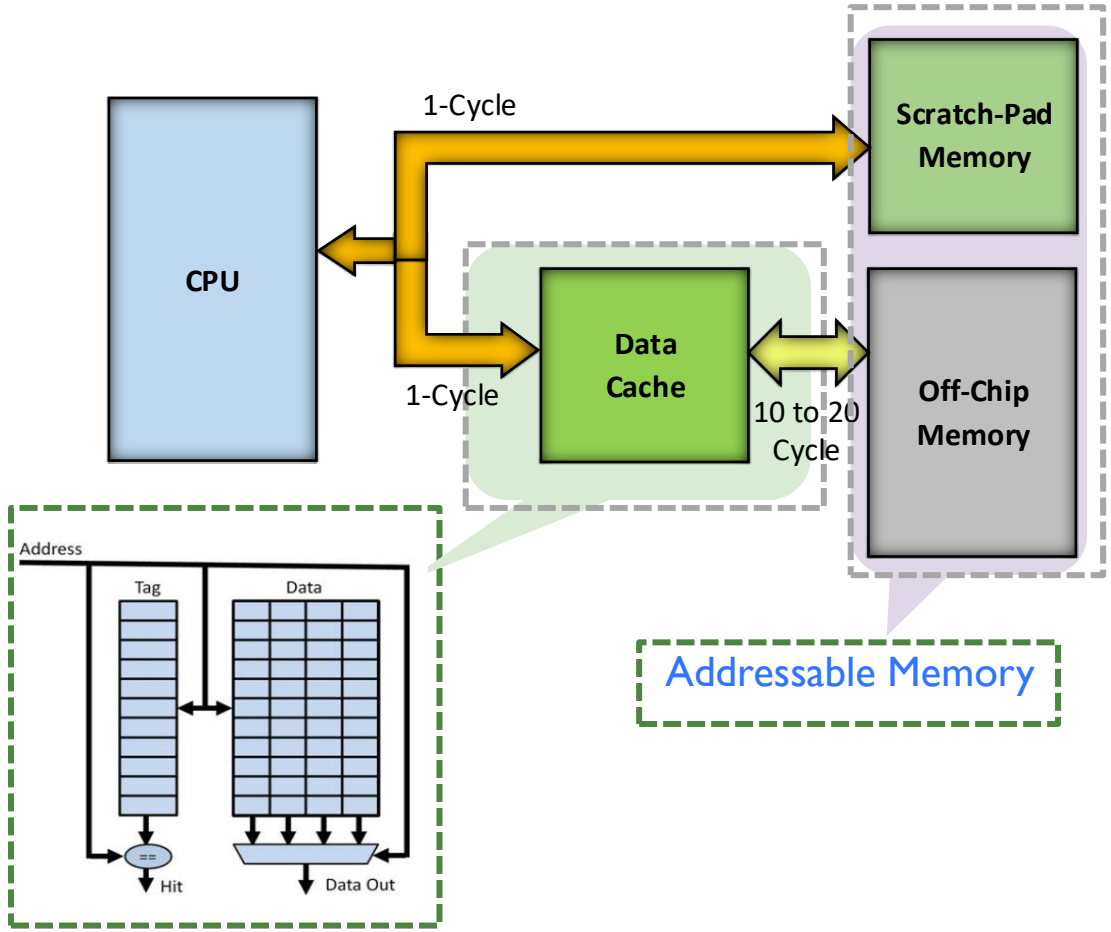
- Smaller memories are faster, whereas larger memories are slower.
- The common method is to architect the memory system as a hierarchy of memories with increasing capacities
- The smallest memory (registers and register files) located closest to the processing units and the largest memory (DRAM) lying farthest.
- Processor fetch the data from the closest memory very fast.
- Performance should not be overwhelmed by excessive accesses to the large memories.



Memory Models

Memory Stages in Embedded Systems

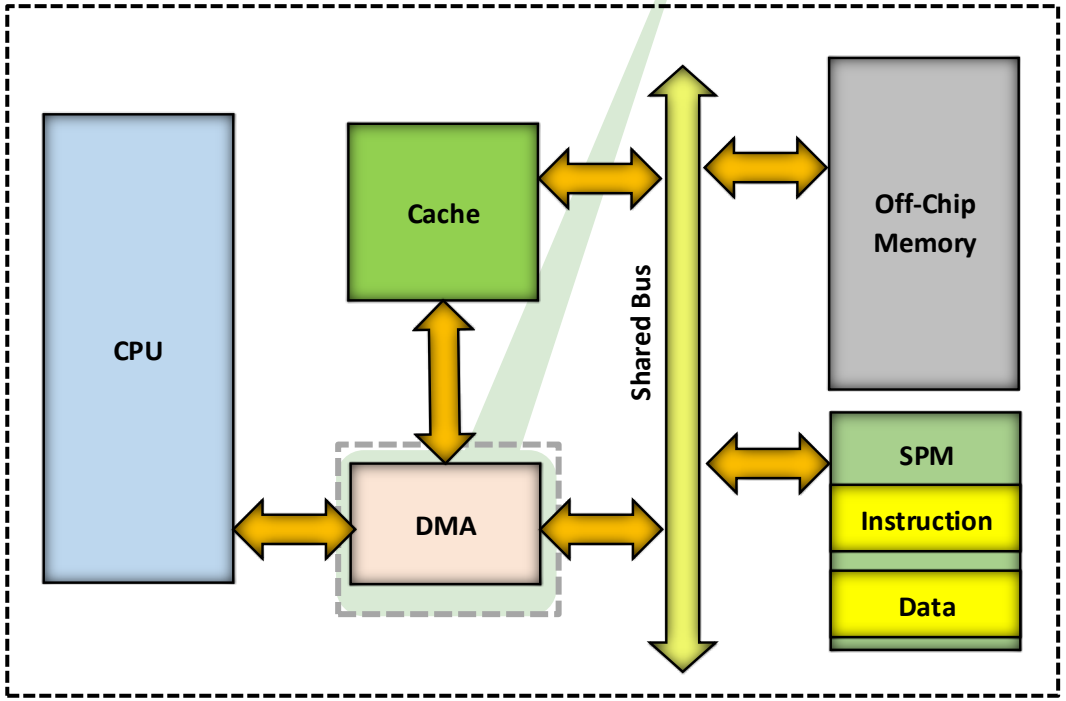
- SRAM (On-chip Memory)
  - Scratch-Pad Memory
  - Cache

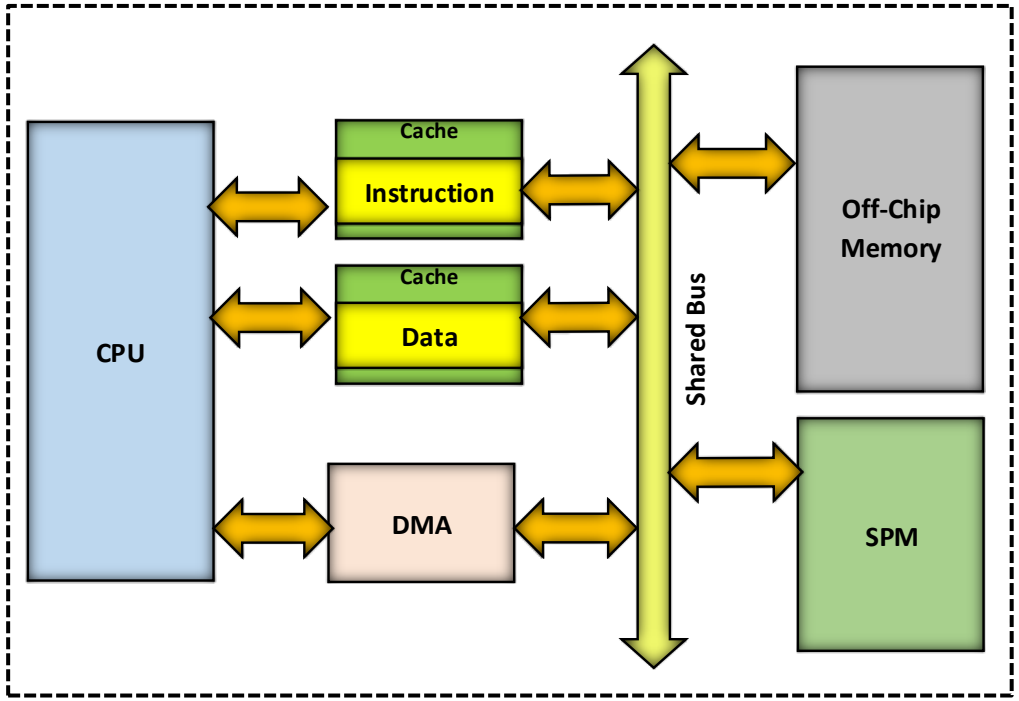


Memory Models

Memory Stages in Embedded Systems

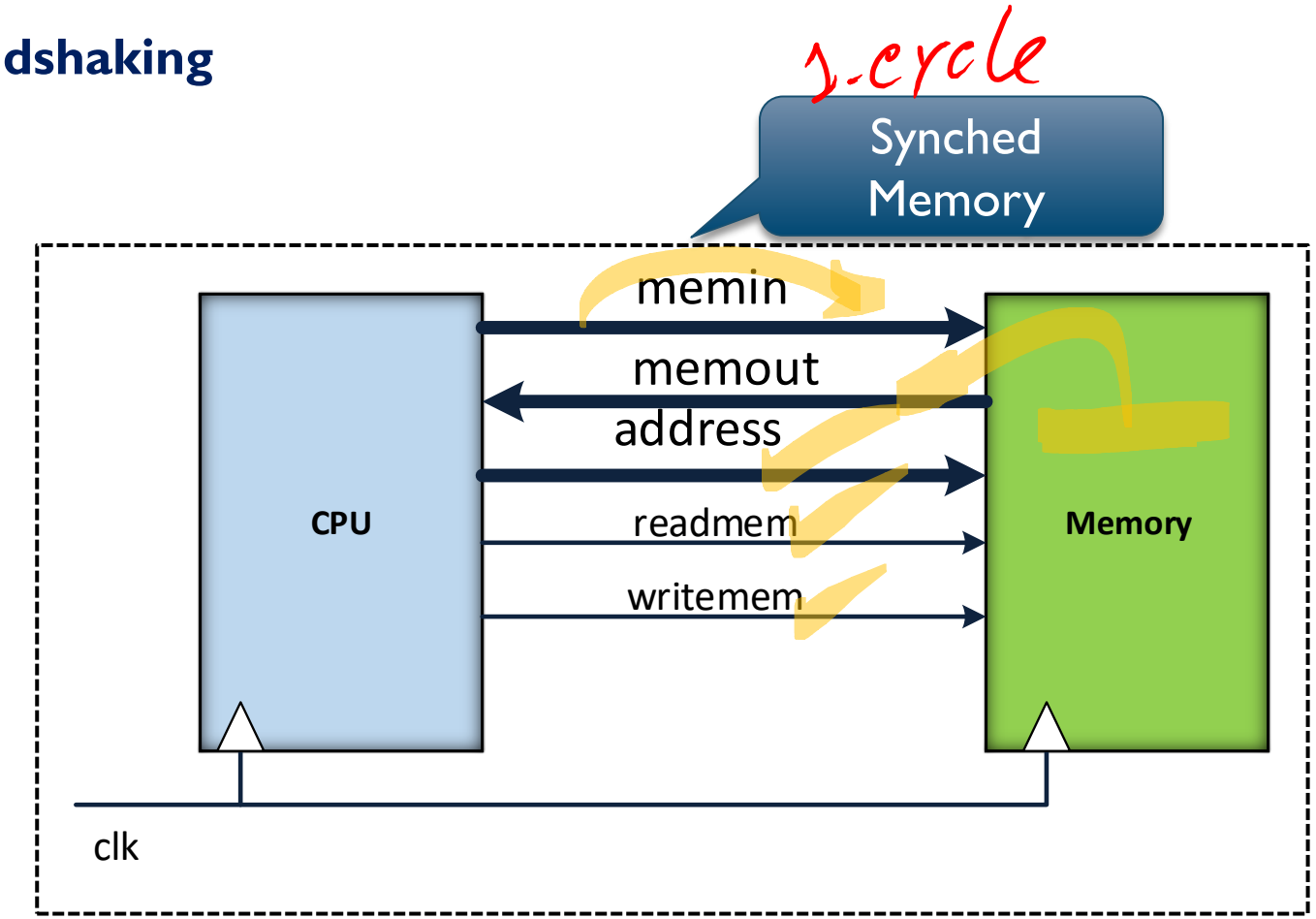
- Different ways of integrating scratchpad memory
  - DMA: Interface between external memory and on-chip memories





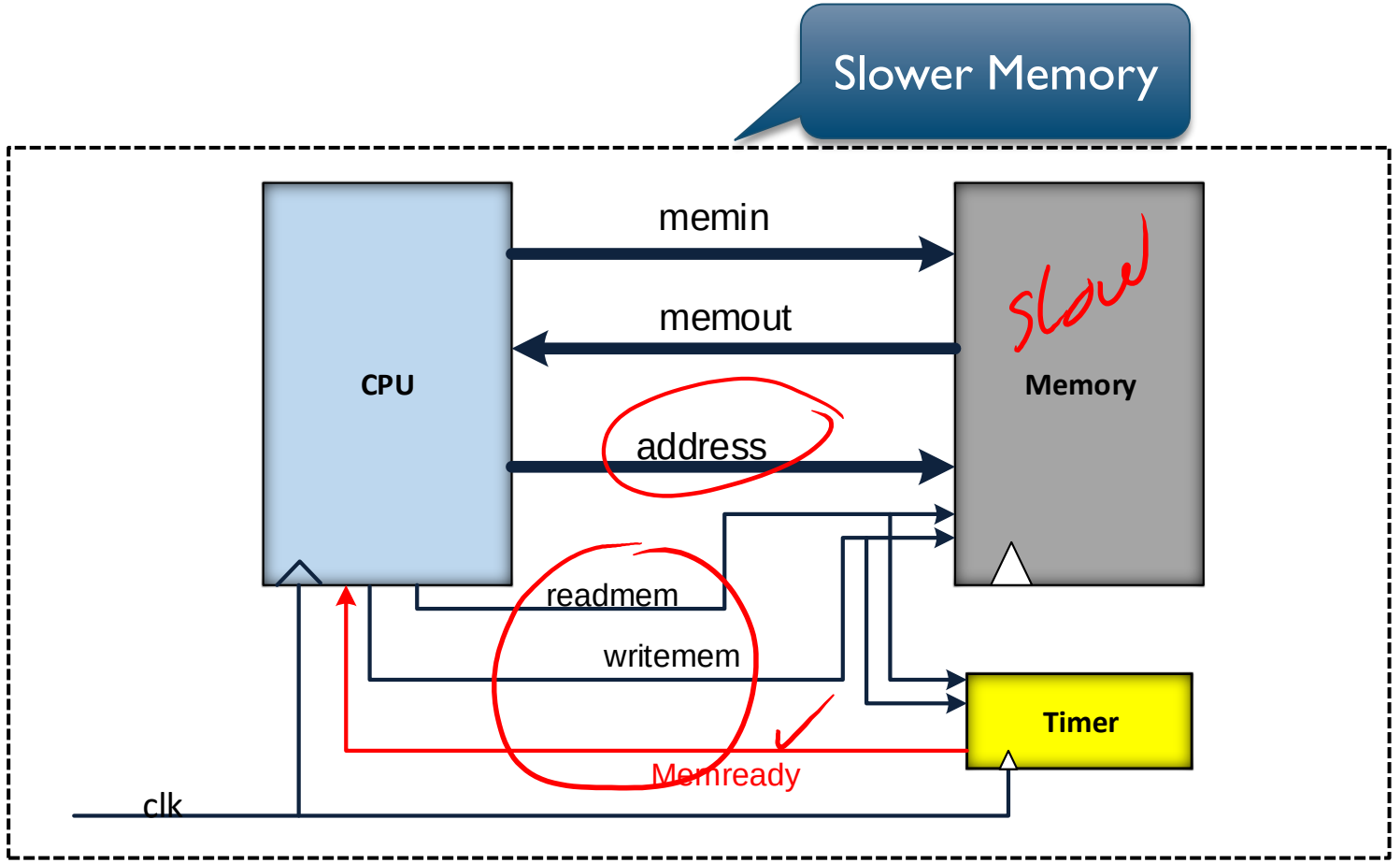
Memory Models

Memory Handshaking



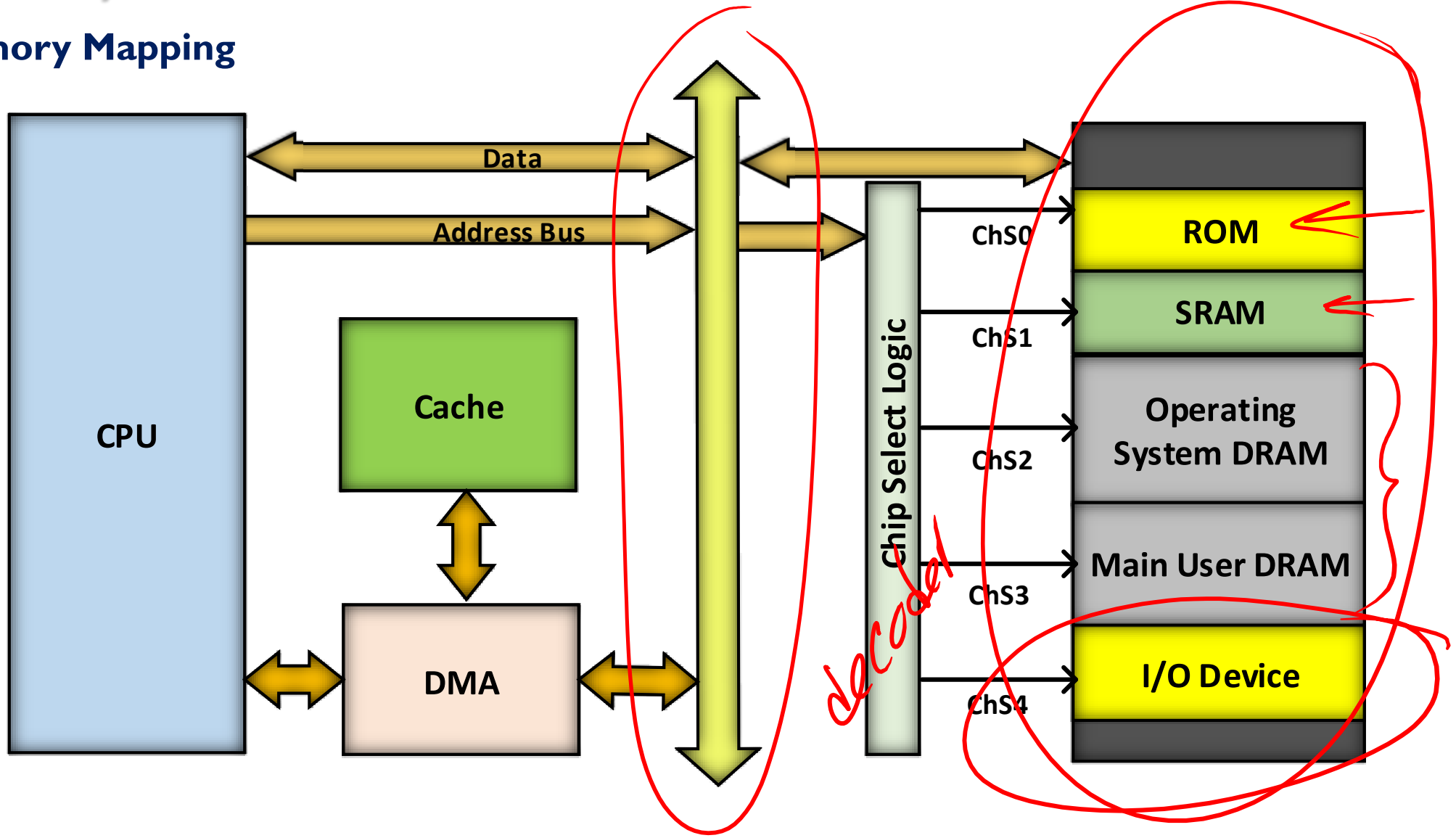
Memory Models

Memory Handshaking



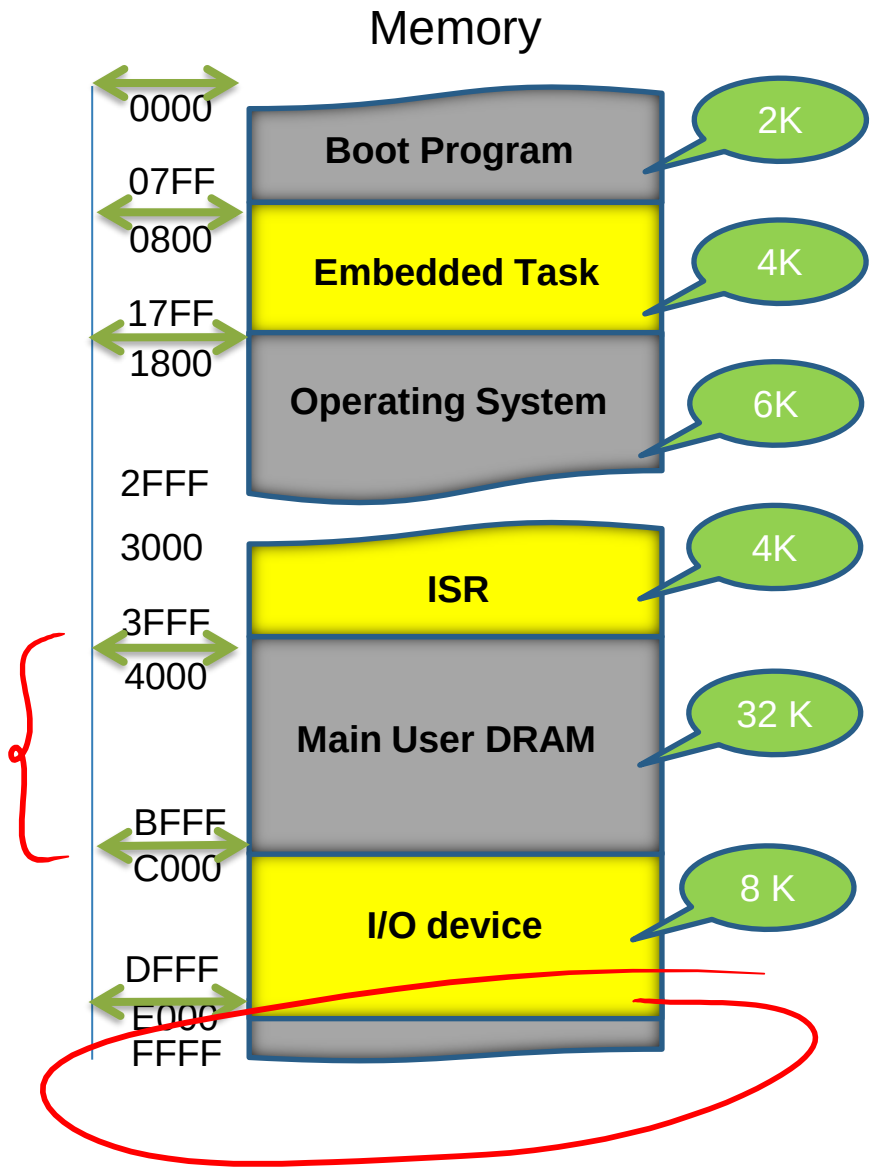
Memory Models

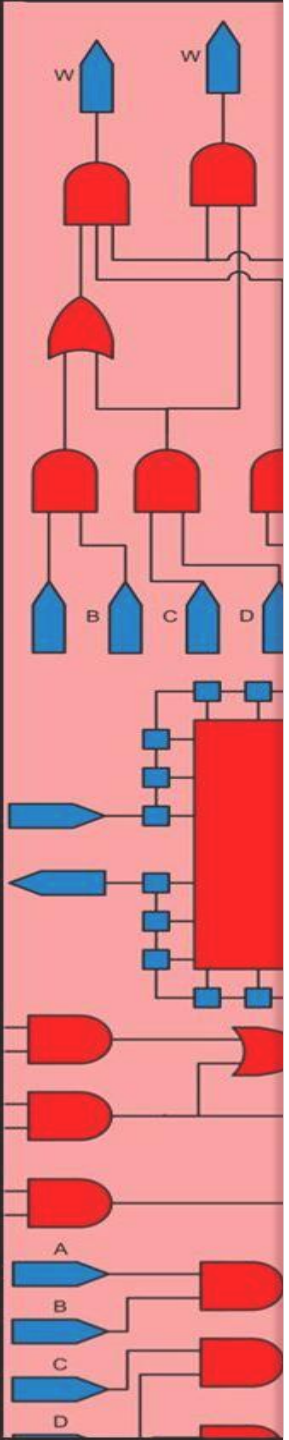
Memory Mapping



Memory Models

Memory Mapping





Conclusion

In this topic we have learned:

- Memory types
- Memories in embedded system
- Memory mapped structure
- Processor-Memory handshaking

example memory map