# VHDL for Modeling, Simulation and Synthesis of RT- and Gate-Level Descriptions

**Zainalabedin Navabi**

**VHDL per modellazione, simulazione e sintesi di descrizioni a livello di RT e Gate**

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# Information


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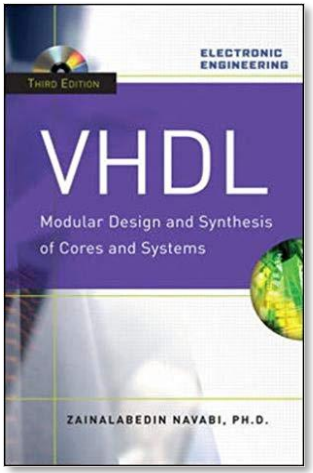
# Information

- Course materials **based on the book**: "*Zainalabedin Navabi, "VHDL: Modular Design and Synthesis of Cores and Systems." McGraw Hill, 2007.*
- Components used for illustrations and examples are chosen according to **current technology trends**.
- All **codes for hardware descriptions**, simulation models, and testbenches are made available to course participants.
- **Simulation and synthesis** of designs have been performed on ModelSim and Intel's Quartus.
- Course name for short: "*RTL VHDL, MSS*"
- Video file format "*RTL VHDL, MSS - #a.mp4*"




Zainalabedin Navabi, "VHDL: Modular Design and Synthesis of Cores and Systems." McGraw Hill, 2007.

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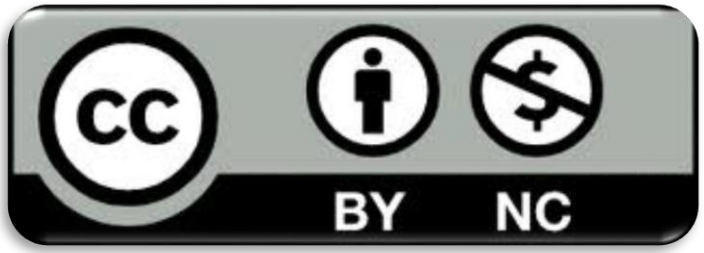


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1- Introduction

2- Basic Structures of VHDL

3- Combinational Circuits

4- Sequential Circuits

5- Memory

6- Writing Testbenches

7- Synthesis Issues

8- RTL Cores