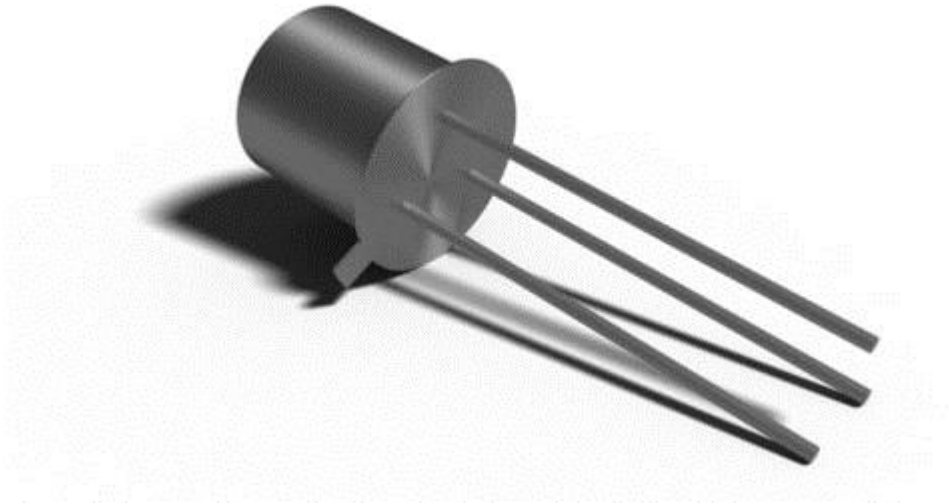
Chapter 3

Metal-Oxyde Semiconductor Field Effect Transistors (MOSFET)



Chapter 3: MOSFET

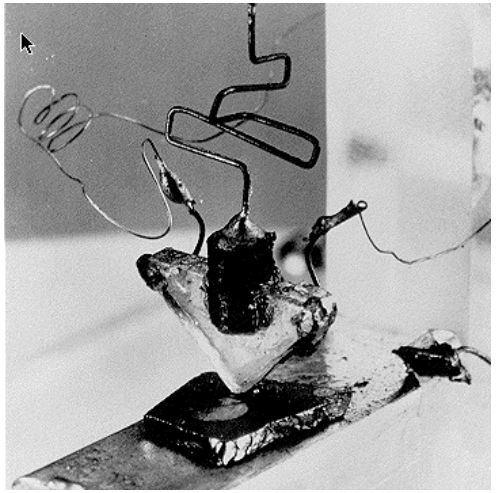
Outline

- Introduction to the MOSFET characteristics
- NMOS device structure
- NMOS detailled I-V characteristics
- PMOS and CMOS technology
- Complements on NMOS technology
- Depletion-type MOSFETs

Introduction to transistors

- Transistors are *the* component that allowed the electronic industry to really take off
  - Transistors are usefull for analog electronics, but even more so for digital electronics
  - Extreme miniaturization possible

1 transistor (1948)



2,600,000,000 transistors (2008)

Introduction to transistors

Field-effect transistors or FET are the most commonly used transistors

- Used in analog and digital electronics
- High imput resistance, small size

$\Rightarrow$ Ideal for applications that require low consumption

- Used a lot in VLSI (very large scale integraiton)
  - i.e. putting a lot of transistors in a small chip
- Two basic forms
  - Metal Oxyde Semiconductor FET (**MOSFET**)
  - Junction gate FET (**JFET**)

high current
⇓
very high chance of burning something (small area, ...)

Introduction to transistors

The basic principle of a transistor is very simple: it is an **electronic switch**

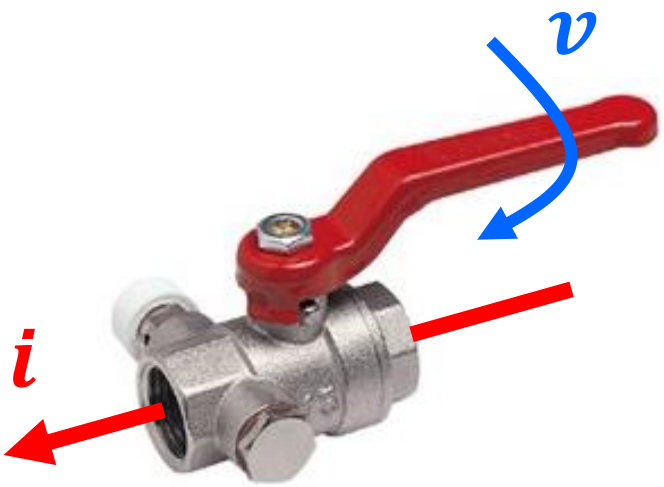
Diode: voltage reaches a threshold
$\Rightarrow$ Current flows
Similar to a pressure valve

Transistor: when we apply a voltage
$\Rightarrow$ current flows
similar to a water tap

Introduction to transistors

The basic principle of a transistor is very simple: it is an **electronic switch**

- MOSFET = voltage-controlled current source



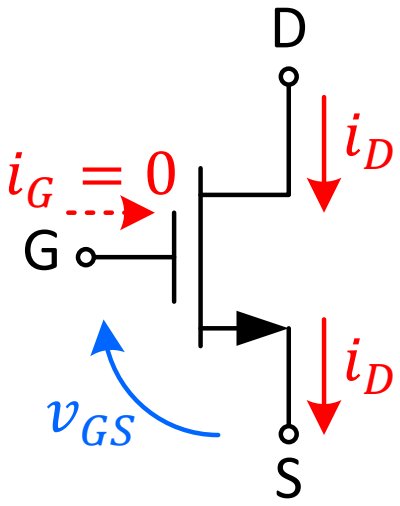
The voltage applied at the input will determine the amount of current that flows through the transistor

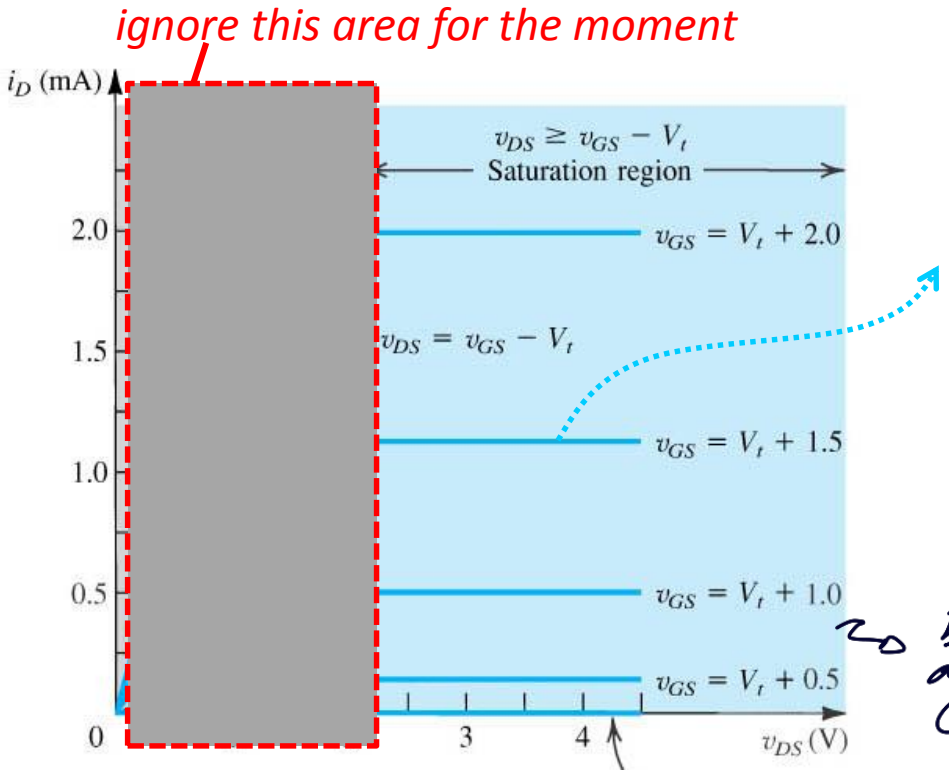
Introduction to transistors

NMOS I-V characteristics

Idealized model of a NMOS transistor

- NMOS is a three-port component*
- Infinite input resistance*
- Current source controlled through input voltage v_{GS} *





1/ Electronic switch

2/ Transconductance amplifier

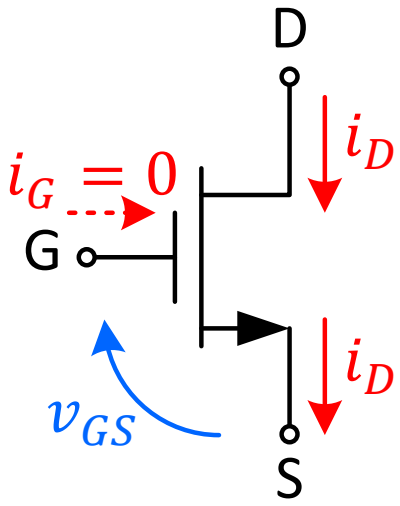
to behave like a current source (same i_D for $\neq v_{DS}$)

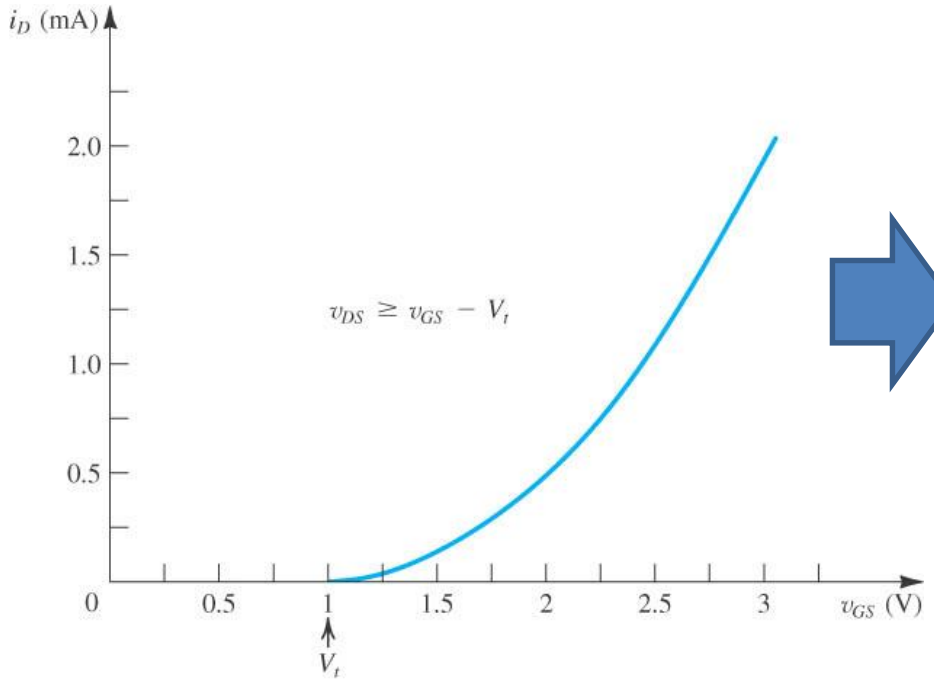
* Not entirely true !

Introduction to transistors

NMOS I-V characteristics

- Transconductance characteristic
- Magnitude of current source controlled through input voltage





1/ Electronic switch

2/ Transcon-ductance amplifier

Introduction to transistors

NMOS I-V characteristics

Idealized model of a NMOS transistor

- NMOS is a three-port component*
- Infinite input resistance*
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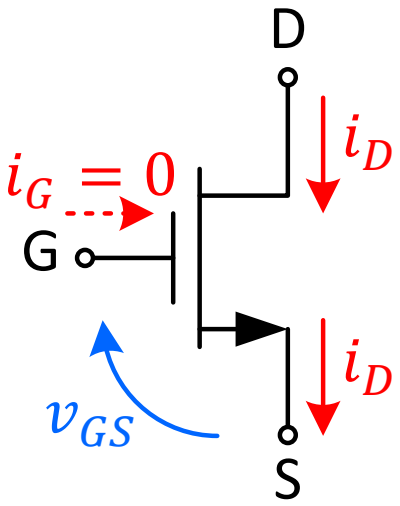


1/ Electronic switch

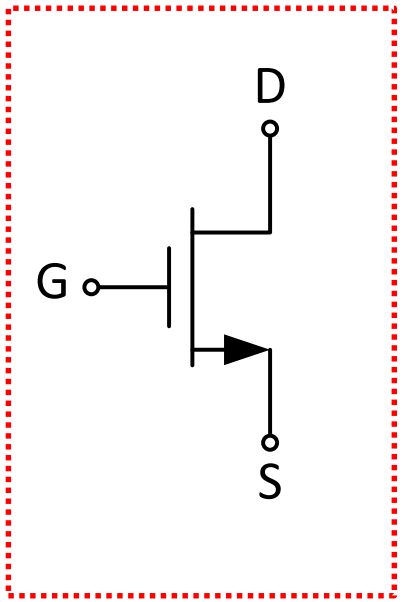
2/ Transcon-ductance amplifier

Introduction to transistors

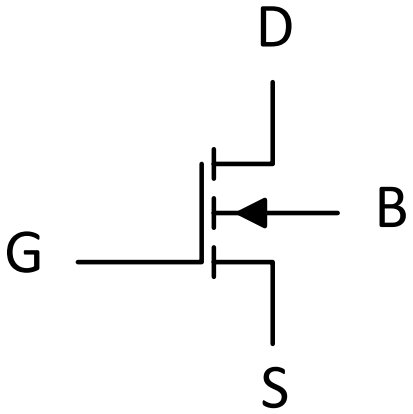
NMOS I-V characteristics

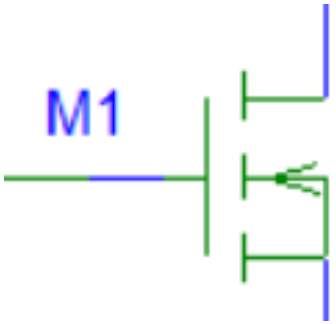
Symbols for NMOS transistor

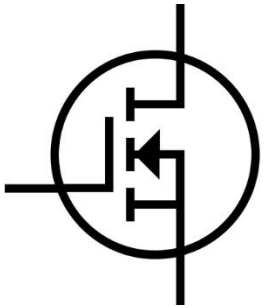
- Poorly standardized for MOSFET



Symbol mostly used in lectures







Chapter 3: MOSFET

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- Introduction to the MOSFET characteristics
- NMOS device structure
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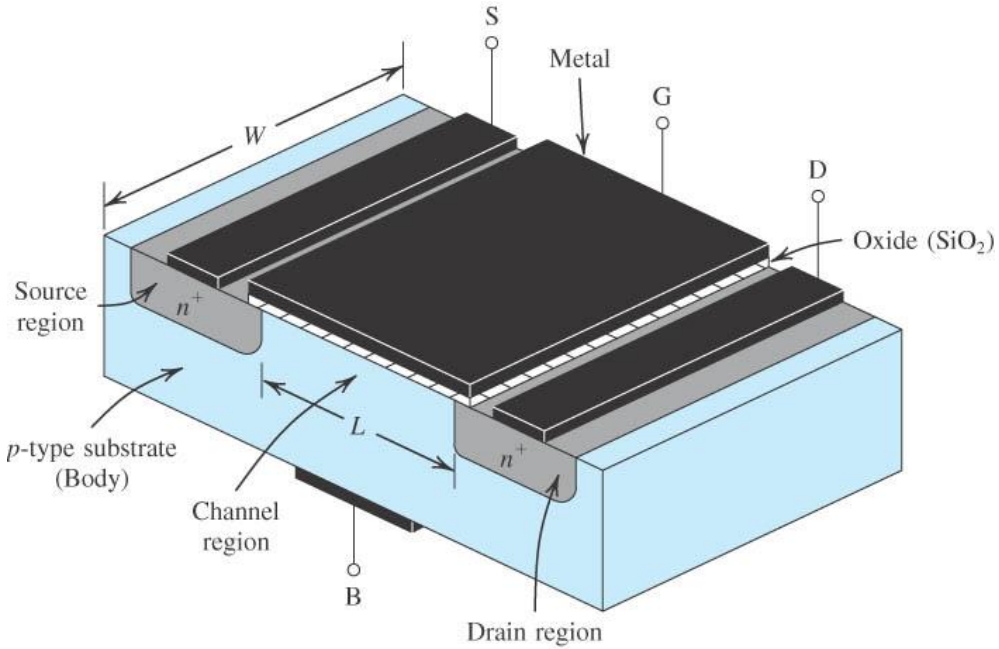
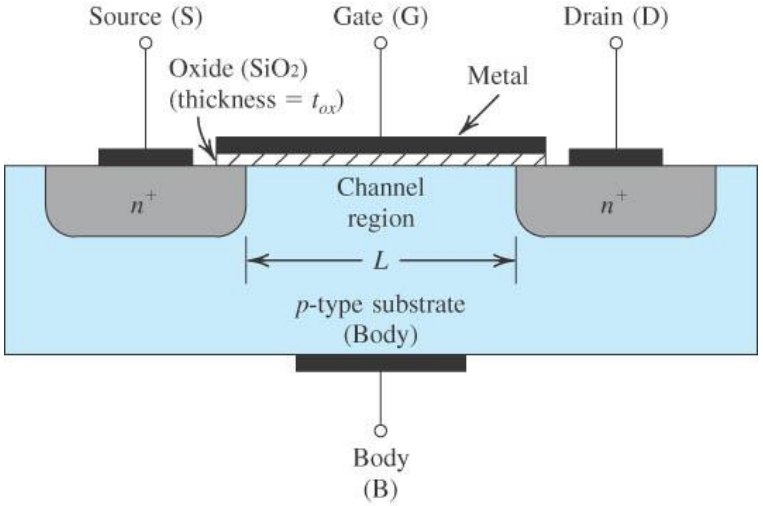
NMOS device structure

Three semiconductors (N-P-N)

- Example of a NPN MOSFET (NMOS transistor)
  - gate electrode is electrically insulated from the body
  - NMOS has 4 terminals (but B often connected to S)
  - n-region heavily doped (n^+)





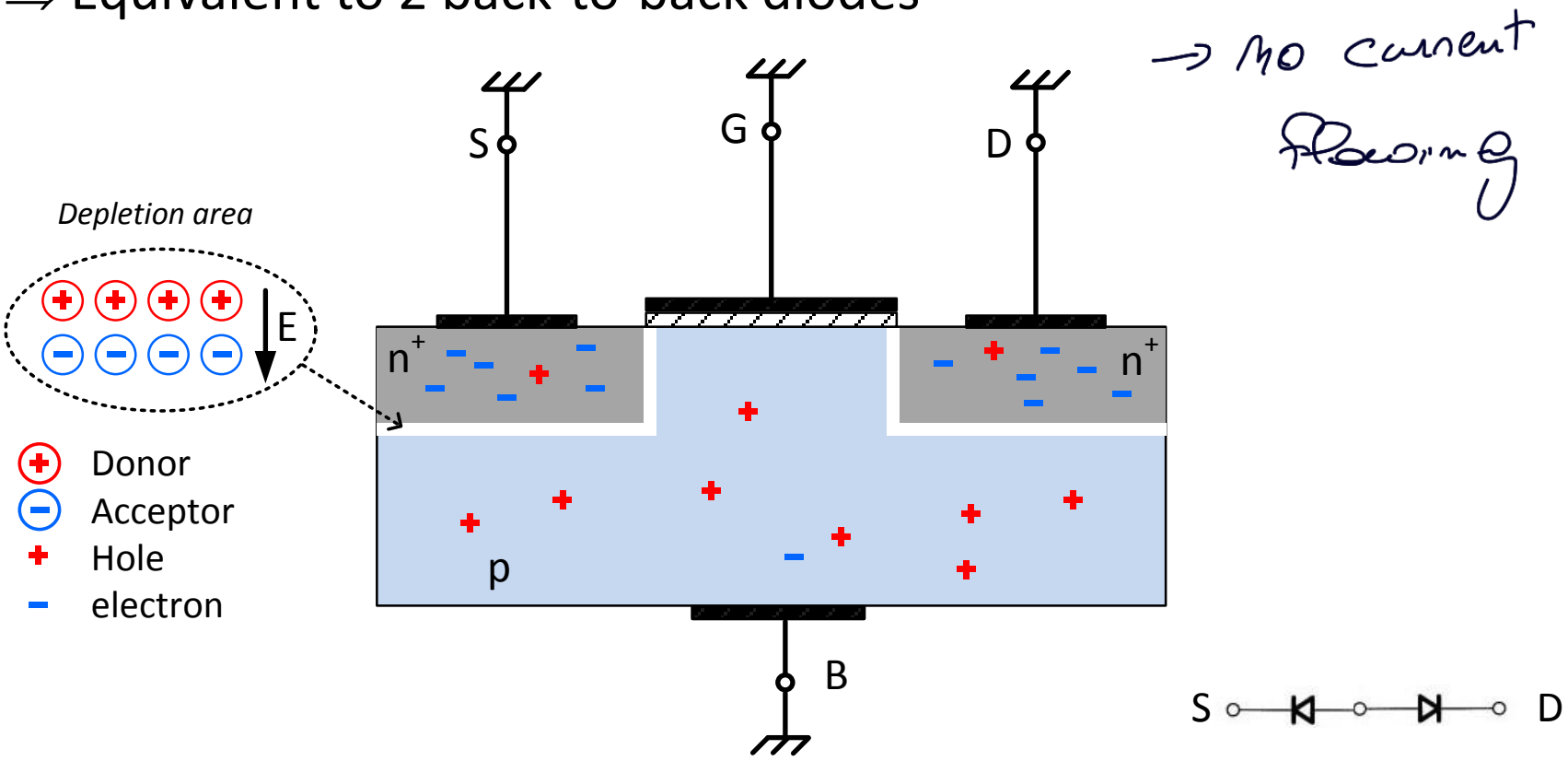
NMOS device structure

No voltage at gate

Two depletion areas appear at both PN junctions

⇒ If no voltage is aplied, no current flows

⇒ Equivalent to 2 back-to-back diodes



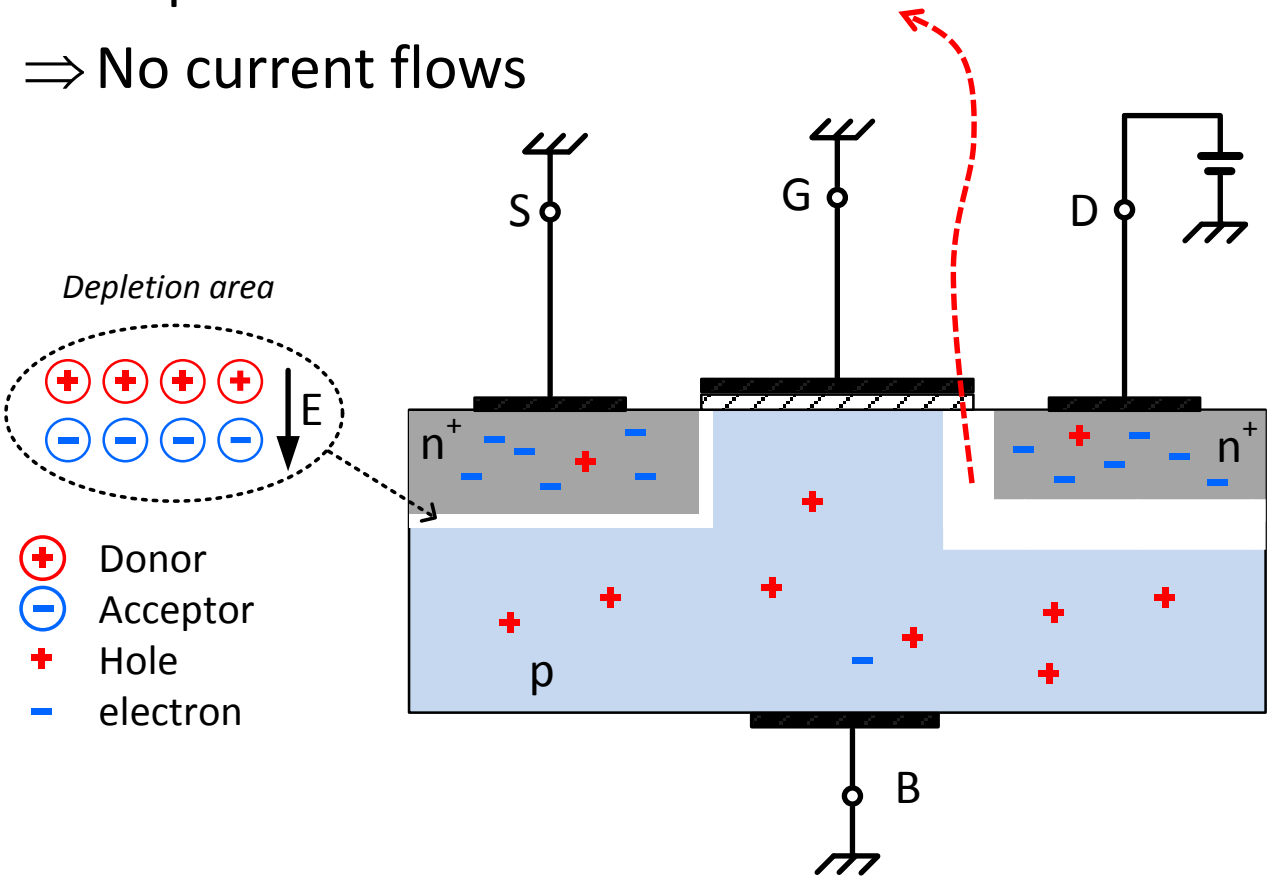
NMOS device structure

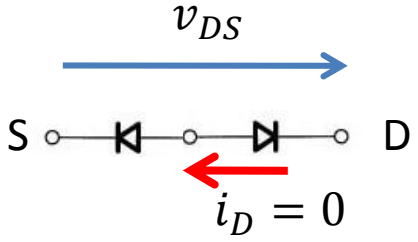
No voltage at gate

When a voltage is applied at the drain (but not at the gate)

$\Rightarrow$ Depletion area widens

$\Rightarrow$ No current flows



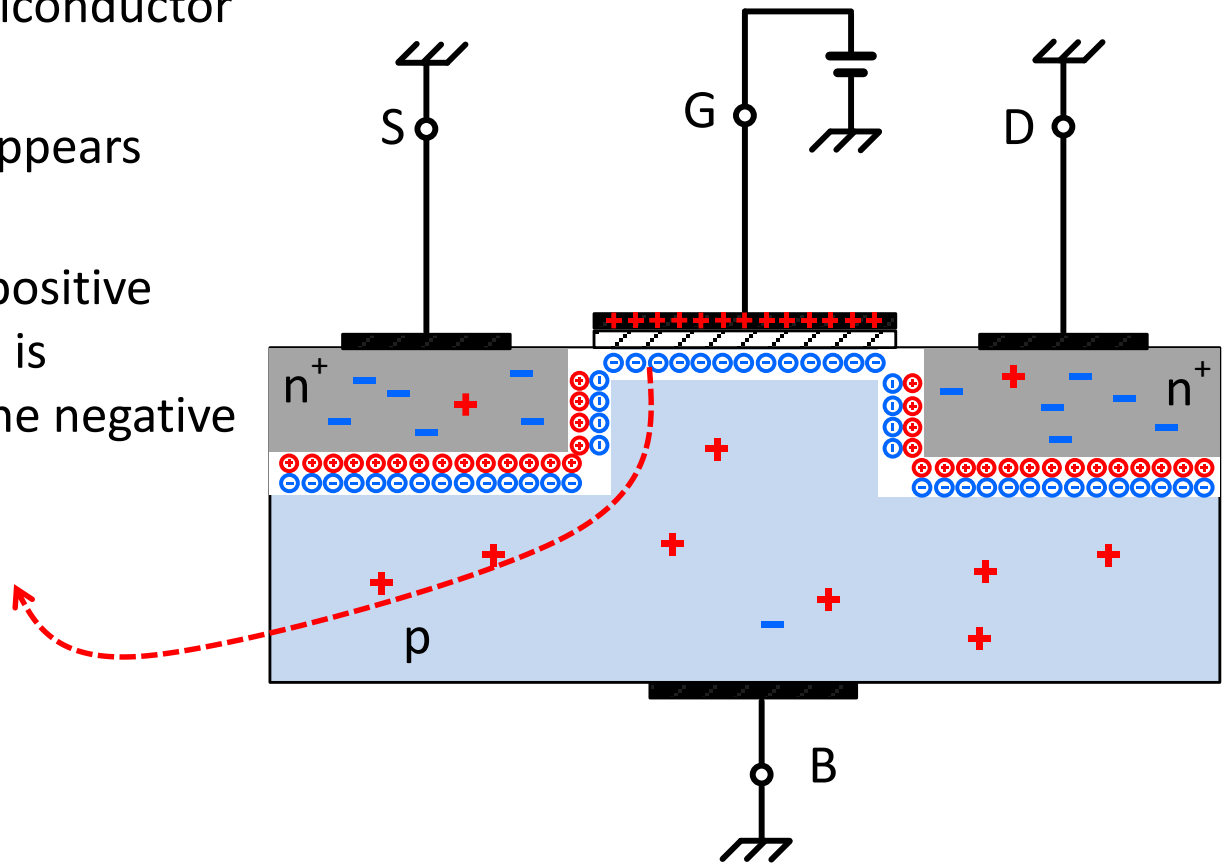


NMOS device structure

Voltage at the gate ($v_{GS} < V_{TH}$)

If a positive voltage is applied at the gate ($v_{GS} < V_{TH}$)

- Holes in the P semiconductor are repelled
- A depletion area appears along the gate
- If $v_{GS} < V_{TH}$, the positive charge on the gate is compensated by the negative bound charges



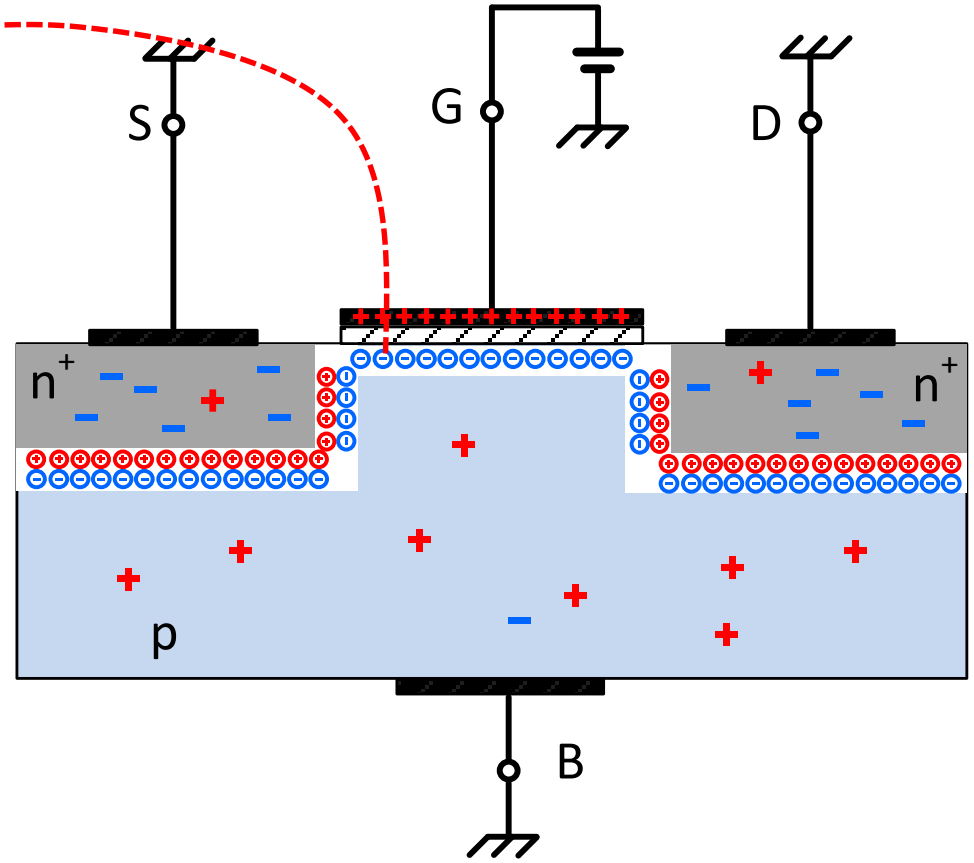
NMOS device structure

Voltage at the gate ($v_{GS} < V_{TH}$)

If a positive voltage is applied at the gate ($v_{GS} < V_{TH}$)

- The charges along the gate are **bound charges** (fixed)

$\Rightarrow$ Even if a voltage is applied at the drain, no current will flow between drain and source



NMOS device structure

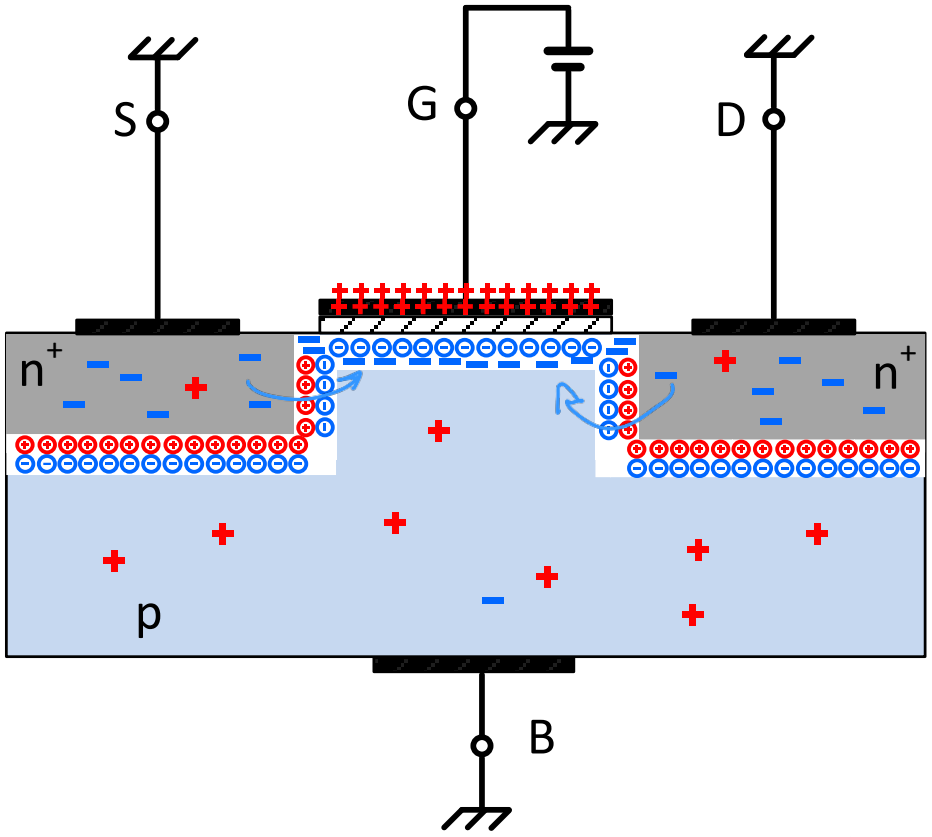
Voltage at the gate ($v_{GS} > V_{TH}$)

When the positive voltage at the gate increases ($v_{GS} > V_{TH}$)

- The charges on the gate will attract electrons from the N-type semiconductors (as well as minority carriers from the P-side)

$\Rightarrow$ A N-type channel is created, connecting source and drain

  - The channel is composed of **mobile carriers**

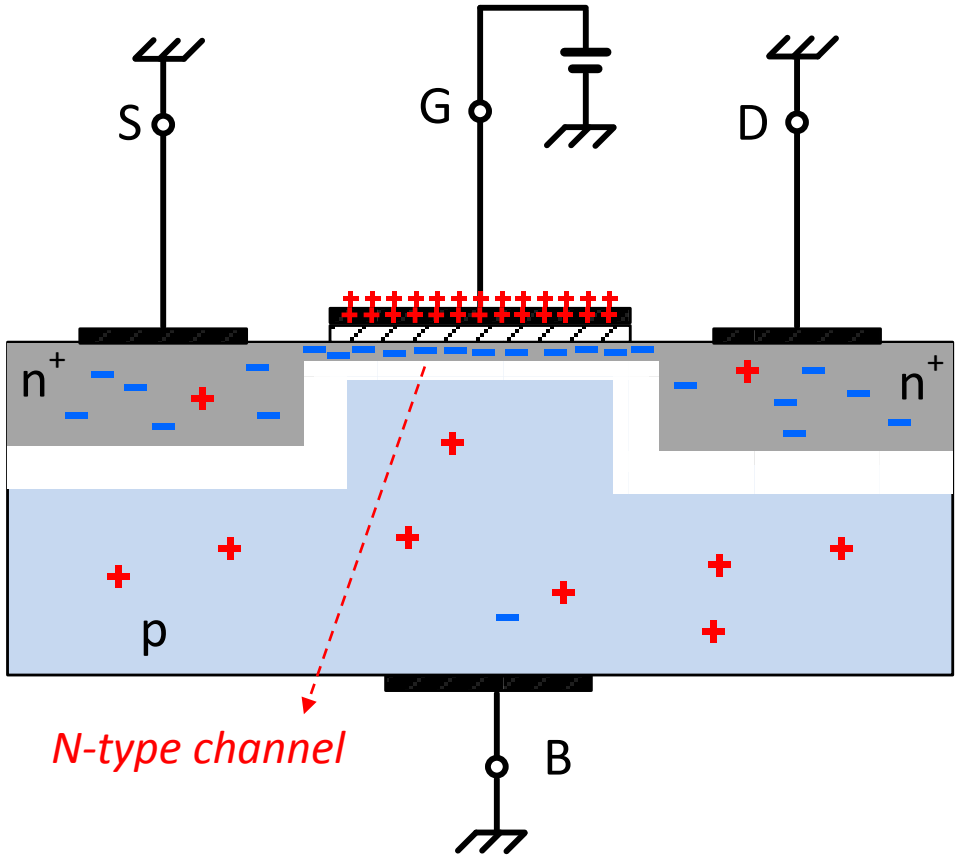


NMOS device structure

Voltage at the gate ($v_{GS} > V_{TH}$)

When the positive voltage at the gate increases ($v_{GS} > V_{TH}$)

- the higher v_{GS}, the larger the induced channel



NMOS device structure

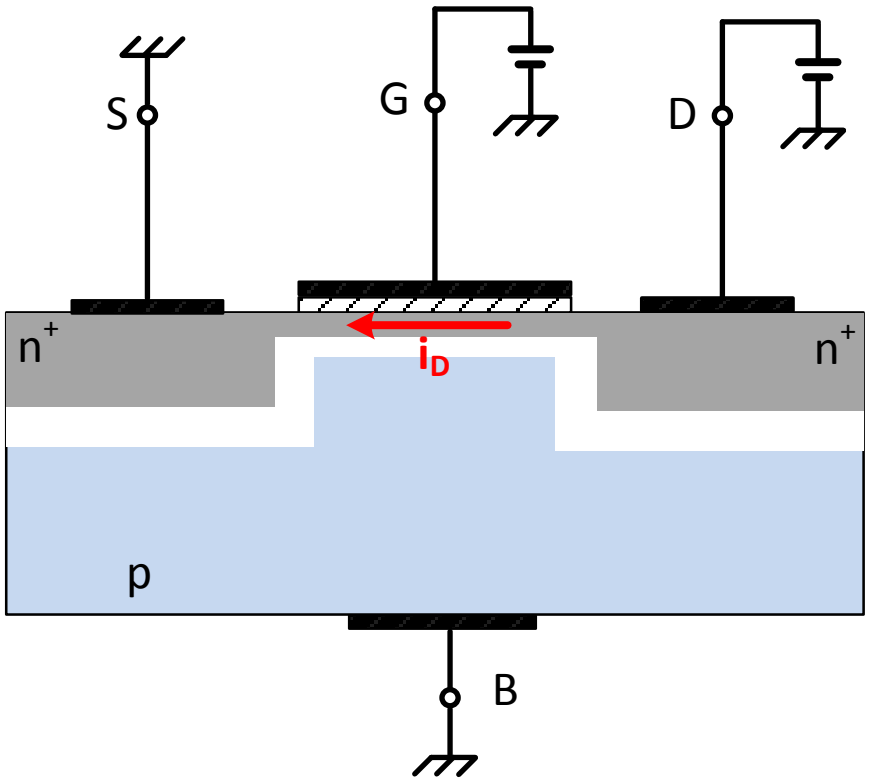
Voltage at the gate ($v_{GS} > V_{TH}$)

When the positive voltage at the gate increases ($v_{GS} > V_{TH}$)

- If a positive voltage is applied at the drain, a current will flow from drain to source

$\Rightarrow$ The gate voltage allows to establish a channel

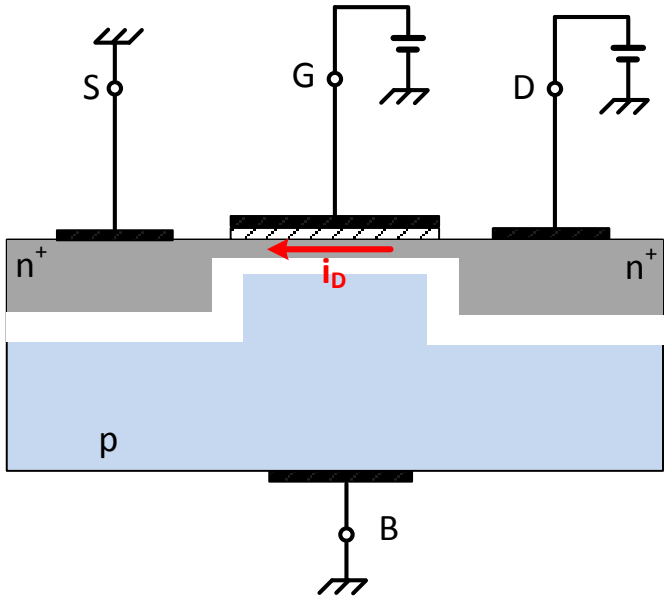
$\Rightarrow$ The drain voltage allows make the current flow

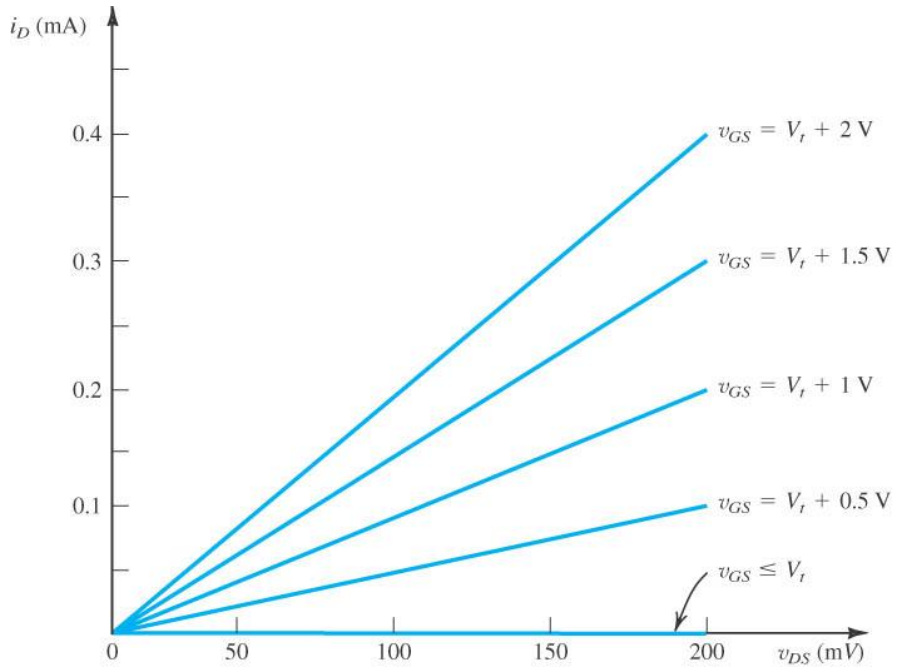


NMOS device structure

Voltage at the gate ($v_{GS} > V_{TH}$)

- If v_{DS} increases
  - $\Rightarrow$ Mobile carriers move faster
  - $\Rightarrow$ current i_D increases
- If v_{GS} increases
  - $\Rightarrow$ Channel becomes wider
  - $\Rightarrow$ current i_D increases





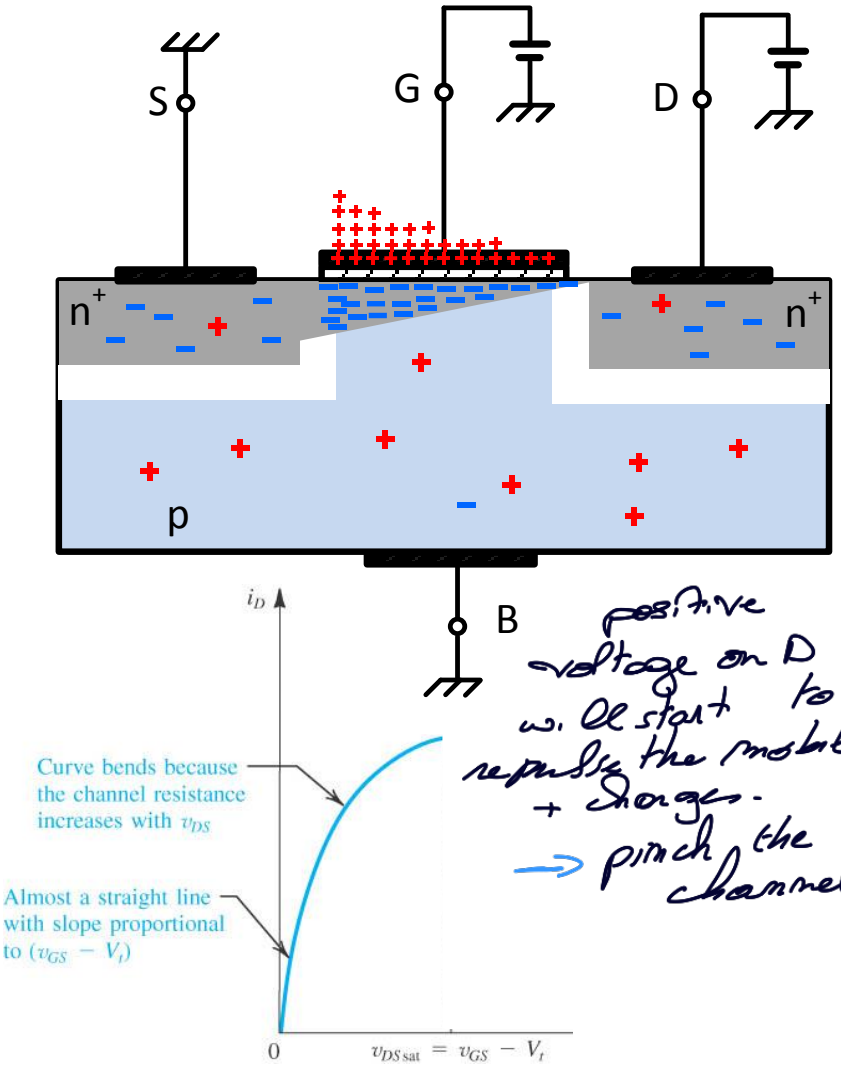
NMOS device structure

Voltage at the gate (higher values of v_{DS})

Higher values of v_{DS}

- Gate-substrate voltage is not uniform
  - Gate-substrate voltage is lower close to drain

  $\Rightarrow$ Channel takes tapered form
- Tapered channel => increased resistance
  - The $i_D = f(v_{DS})$ curve bends



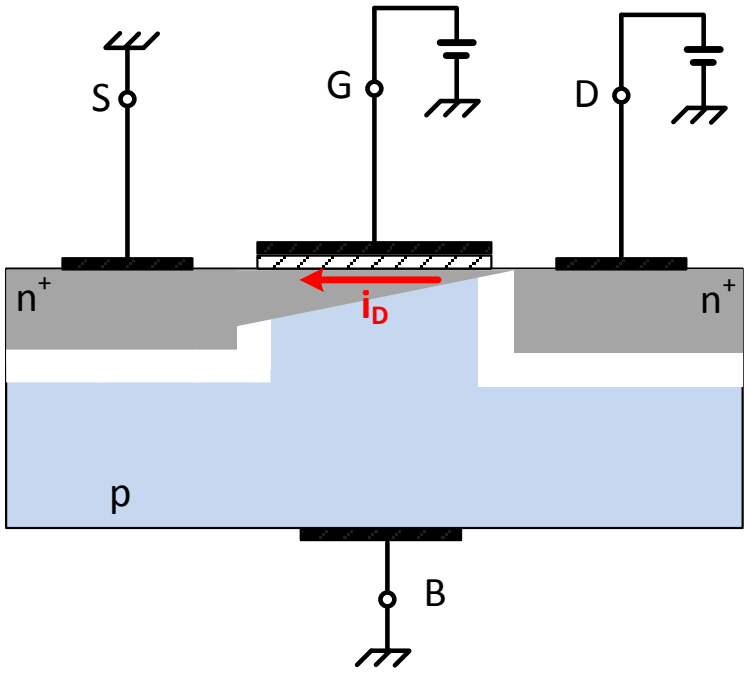
NMOS device structure

Voltage at the gate (higher values of v_{DS})

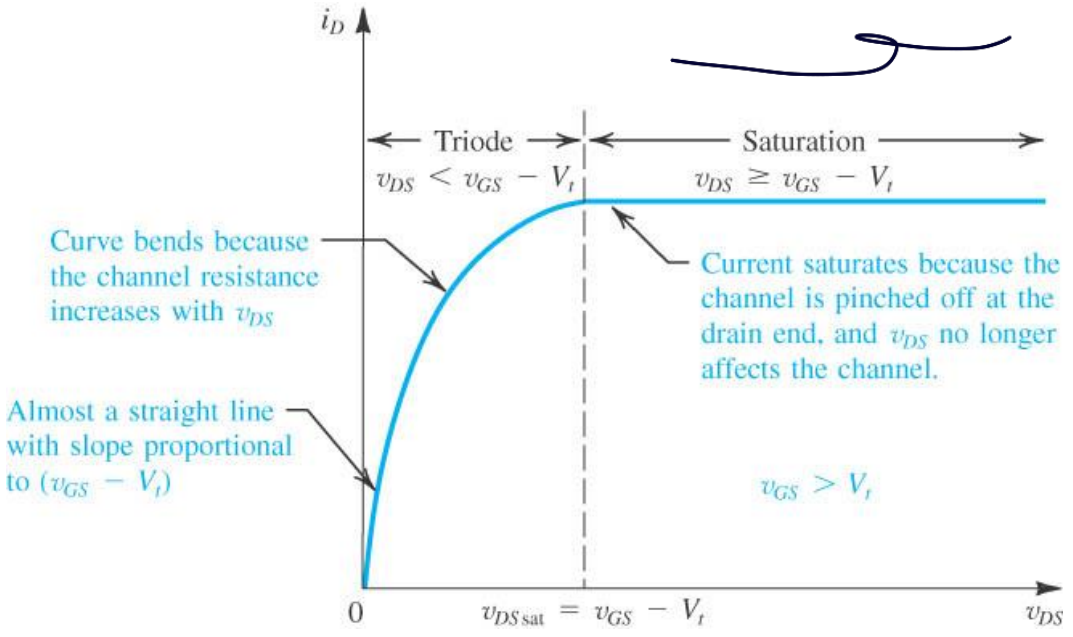
Eventually, when $v_{DS} \geq v_{GS} - V_{TH}$

- Channel is completely pinched off
- Increase in v_{DS} no longer increases current

$\Rightarrow$ Saturation region



where we want to operate them



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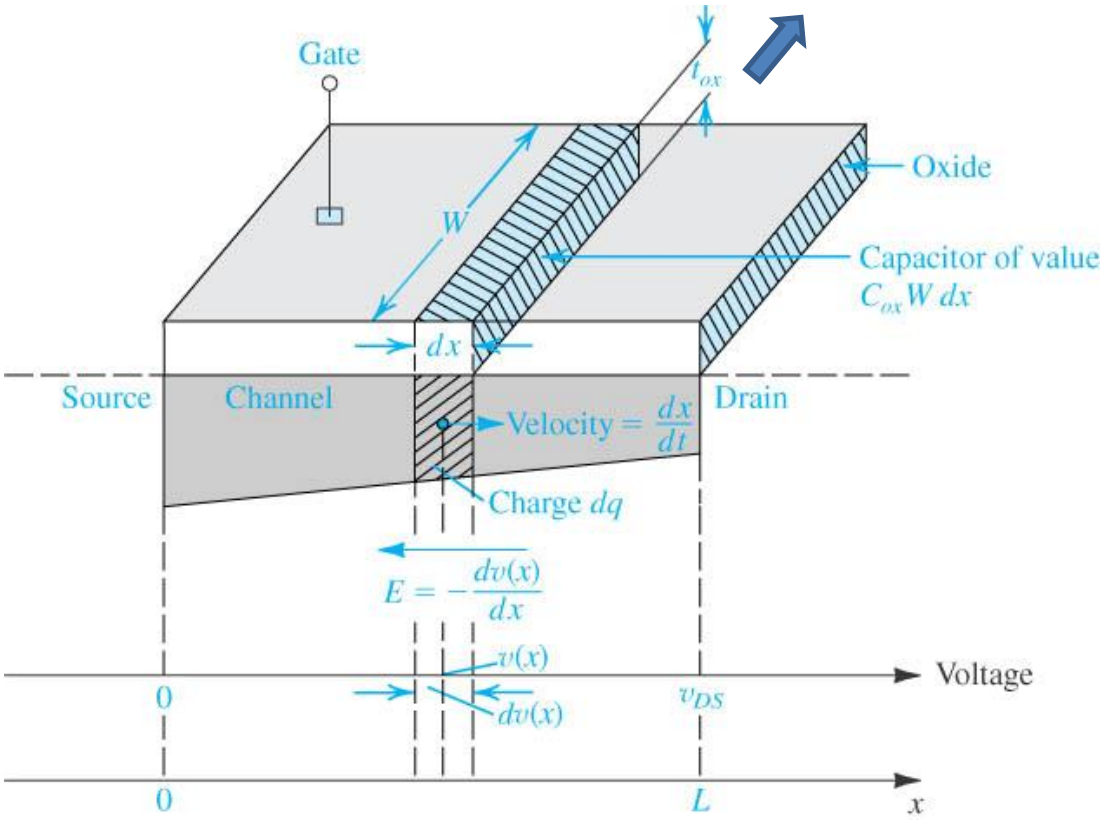
NMOS detailled I-V characteristics

Derivation of i_D-v_{DS}

$$C_{ox} = \varepsilon_{ox}/t_{ox}$$



Strip dx: $C = C_{ox}Wdx$

$$dq = -C\big(v_{GS} - V_T - v(x)\big)$$

$$\Leftrightarrow \boxed{dq = -C_{ox}W\big(v_{GS} - V_T - v(x)\big)dx}$$

$$E(x) = -\frac{dv(x)}{dx}$$

$$v_{drift} = \frac{dx}{dt} = -\mu_n E(x)$$

$$\frac{dx}{dt} = \mu_n \frac{dv(x)}{dx}$$

NMOS detailled I-V characteristics

Derivation of i_D-v_{DS}

$$\frac{dq}{dx} = -C_{ox}W\left(v_{GS} - V_T - v(x)\right)$$

$$\frac{dx}{dt} = \mu_n \frac{dv(x)}{dx}$$

$$i = \frac{dq}{dt} = \frac{dq}{dx}\frac{dx}{dt}$$

$$i_D = -i = C_{ox}W\mu_n\left(v_{GS} - V_T - v(x)\right)\frac{dv(x)}{dx}$$

$$\Rightarrow \quad i_D dx = C_{ox}W\mu_n\left(v_{GS} - V_T - v(x)\right)dv(x)$$

$$\Rightarrow \quad \int_0^L i_D dx = \int_0^{v_{DS}} C_{ox}W\mu_n\left(v_{GS} - V_T - v(x)\right)dv(x)$$

$$\Rightarrow \quad \boxed{i_D = k'_n \frac{W}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{1}{2}v_{DS}^2\right]}$$

with $k'_n = \mu_n C_{ox}$

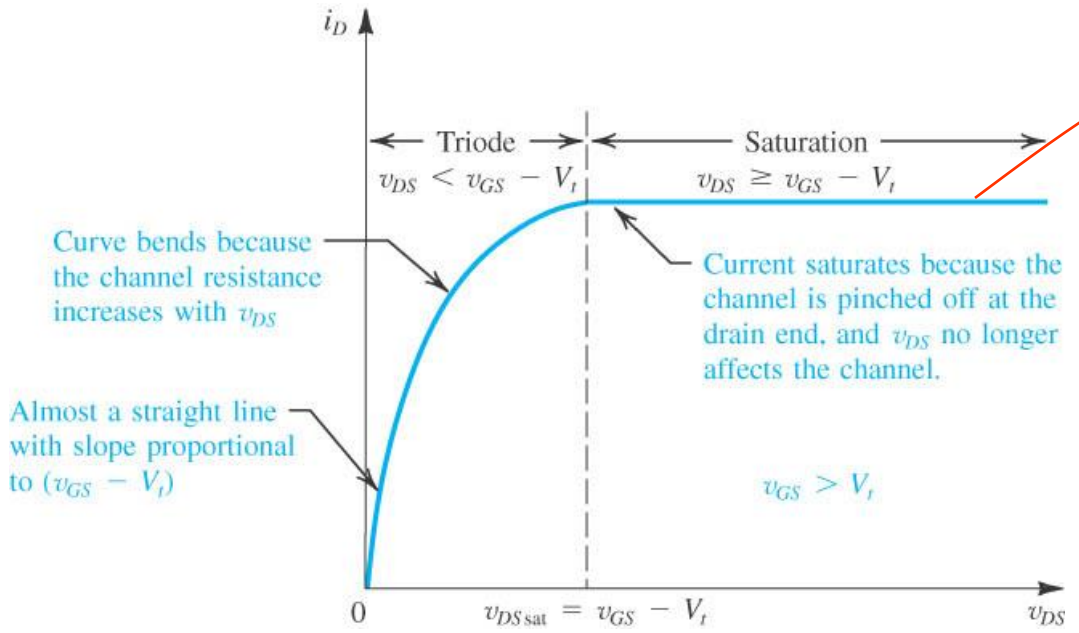
NMOS detailled I-V characteristics

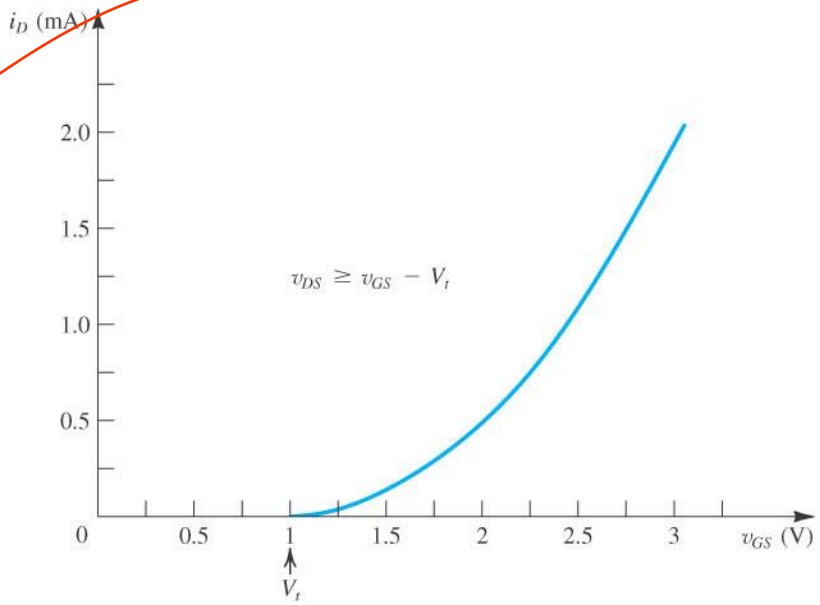
Derivation of i_D-v_{DS}

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

Saturation: $v_{DS} = v_{GS} - V_T$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_T)^2$$





NMOS detailled I-V characteristics

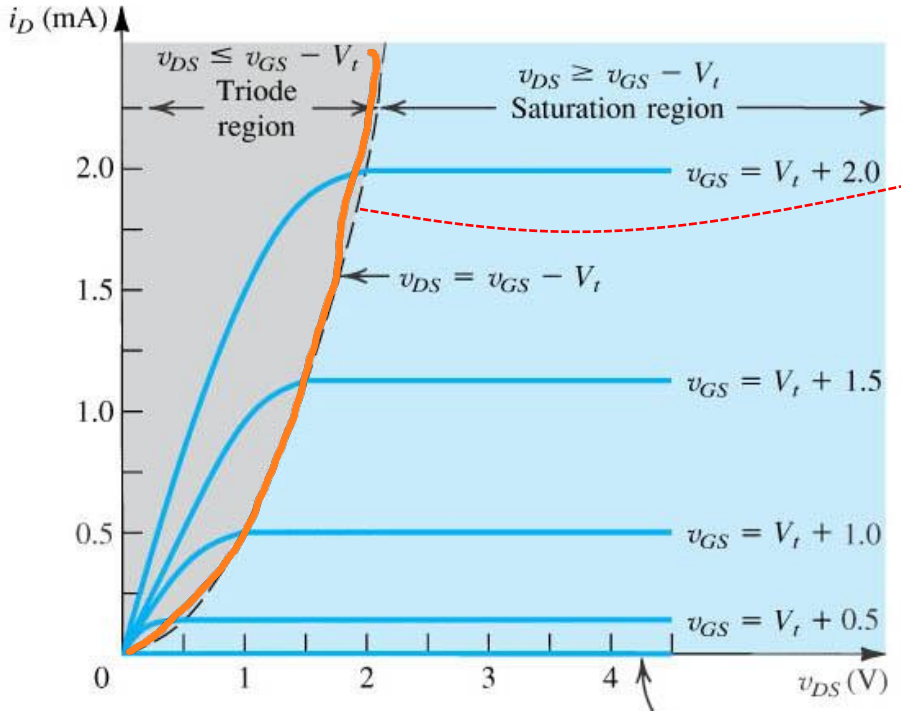
Derivation of i_D-v_{DS}

Triode region:

$$i_D = k'_n \frac{W}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

Saturation region:

$$i_D = \frac{1}{2}k'_n \frac{W}{L}(v_{GS} - V_T)^2$$



Limit between triode and saturation region:

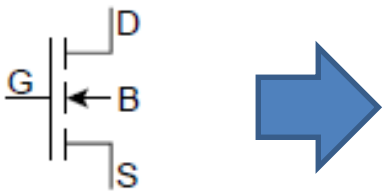
$$v_{DS} = v_{GS} - V_T$$

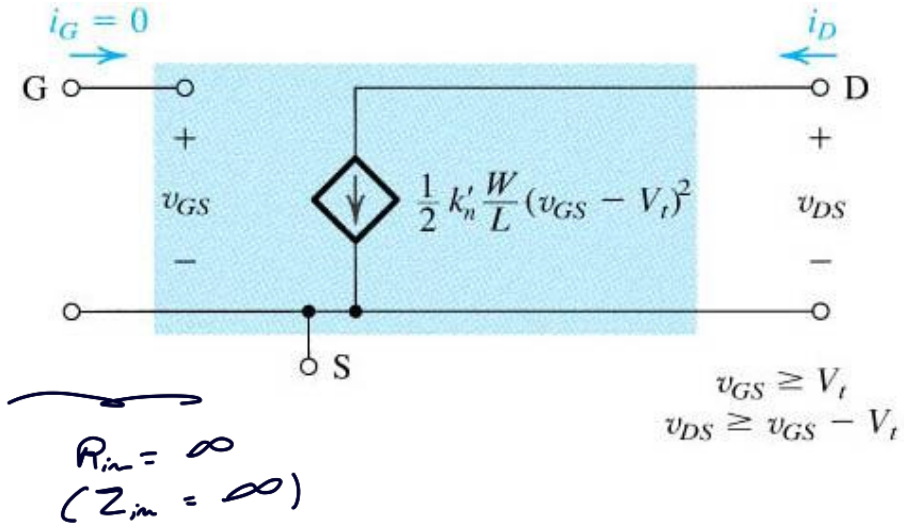
$$\Leftrightarrow i_D = \frac{1}{2}k'_n \frac{W}{L}v_{DS}^2$$

NMOS detailled I-V characteristics

In saturation region…

- large-scale equivalent circuit
  - NMOS operates as a perfect current source
  - Input on gate: very high (infinite) input impedance
  - Valid for $v_{DS} \geq v_{GS} - V_T$

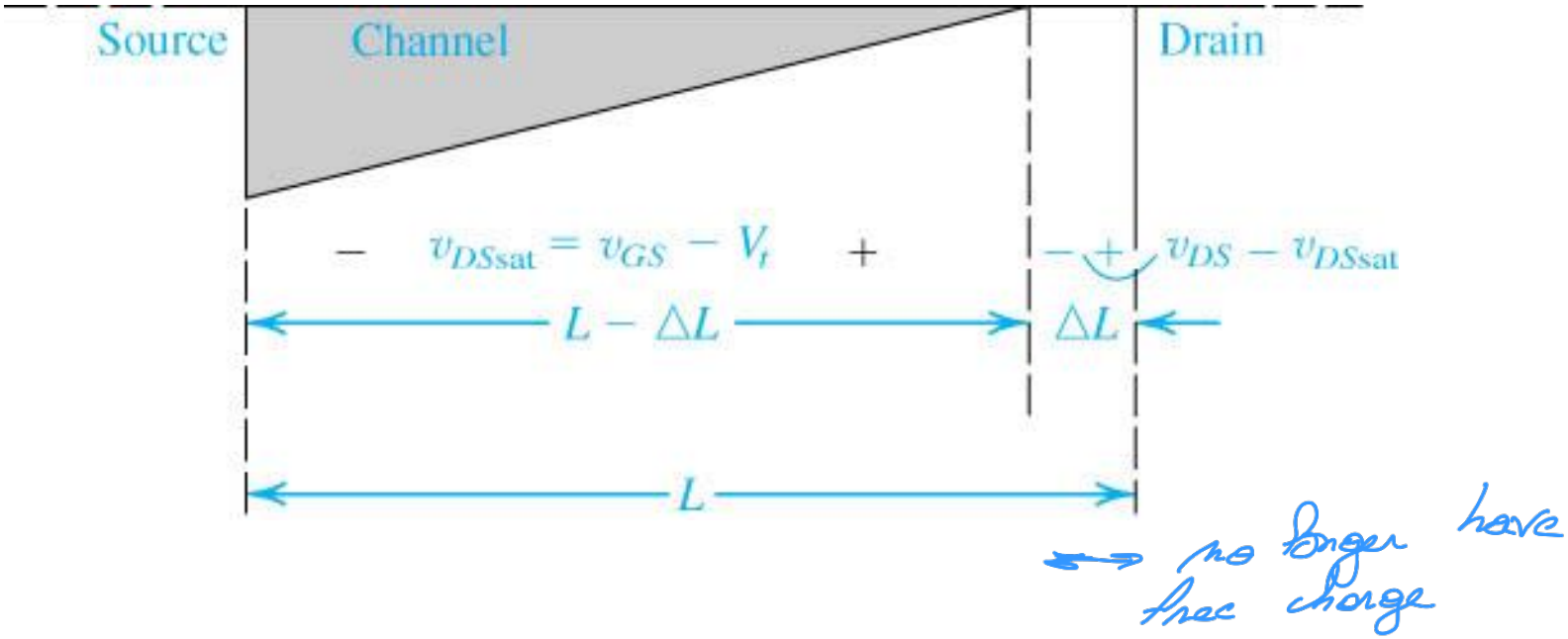




NMOS detailled I-V characteristics

Saturation region: effect of channel pinching

- Increasing v_{DS} reduces the channel length
  - Voltage accross actual channel remains $v_{GS} - V_T = V_{D,sat}$
  - Electrons are accelerated through depletion region by additional voltage drop



NMOS detailled I-V characteristics

Saturation region: effect of channel pinching

- Quantitative analysis:

$$i_D = \frac{1}{2} k'_n \frac{W}{L - \Delta L} (v_{GS} - V_T)^2$$

$$\Rightarrow i_D = \frac{1}{2} k'_n \frac{W}{L} \left(\frac{1}{1 - \Delta L / L} \right) (v_{GS} - V_T)^2$$

$$\Rightarrow i_D = \frac{1}{2} k'_n \frac{W}{L} \left(1 + \frac{\Delta L}{L} \right) (v_{GS} - V_T)^2$$

1st order approx.

- Let us assume: $\frac{\Delta L}{L} = \frac{\lambda'}{L} v_{DS} = \lambda v_{DS}$

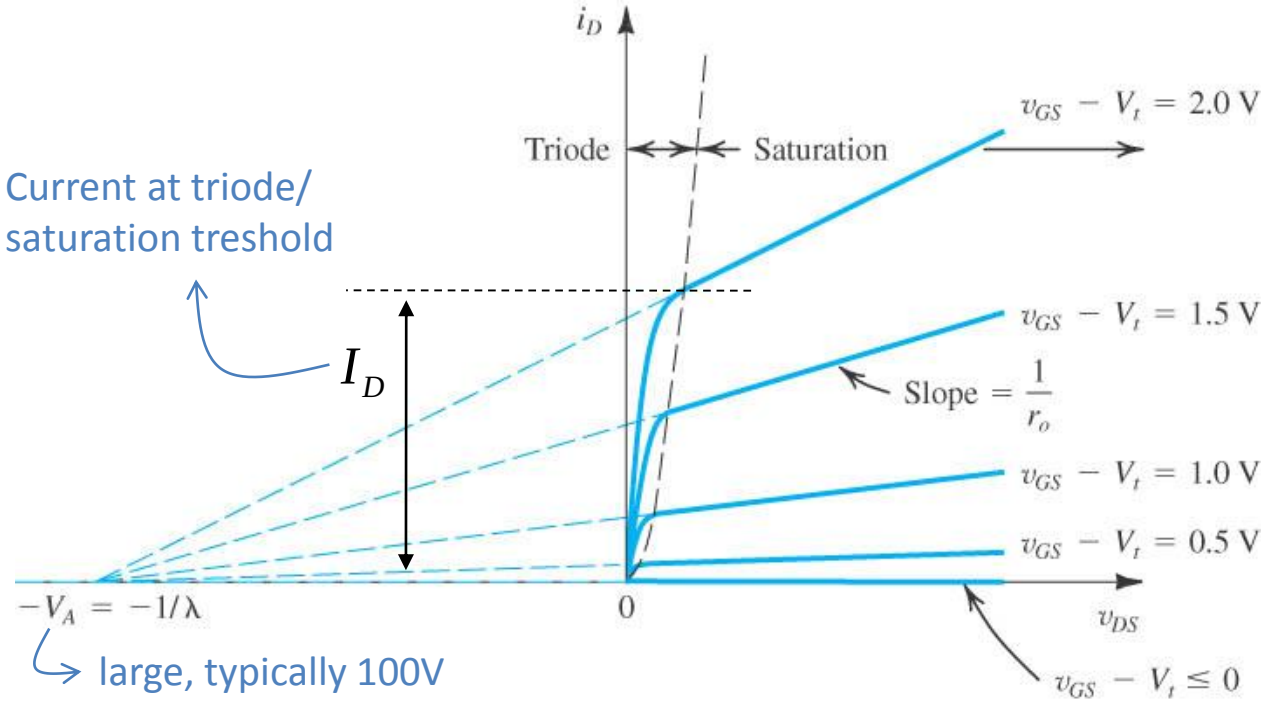
the higher the V_{DS}, the shorter the channel

$$\Rightarrow i_D = \frac{1}{2} k'_n \frac{W}{L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$

NMOS detailled I-V characteristics

Saturation region: effect of channel pinching

$$i_D = \frac{1}{2} k'_n \frac{W}{L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$



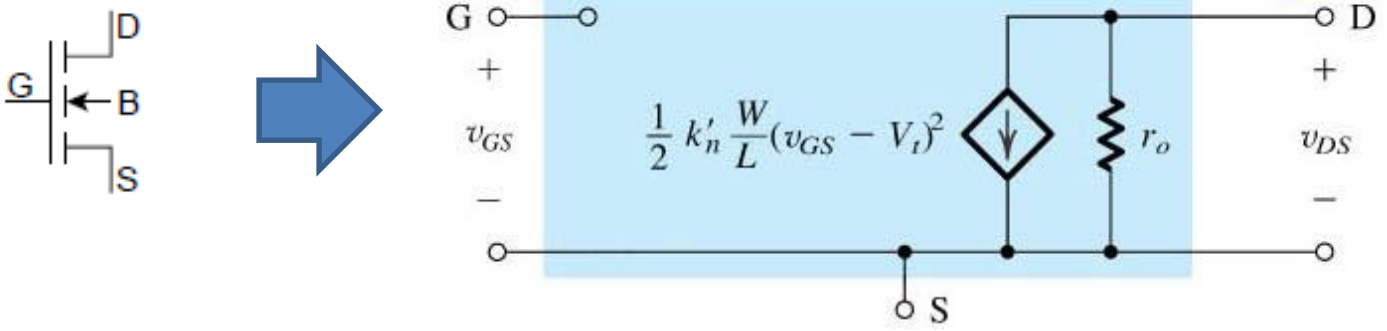
=> Output impedance of current source: $r_o = \left[\frac{di_D}{dv_{DS}}\right]^{-1} \approx \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$

with $I_D = k'_n \frac{W}{L} (v_{GS} - V_T)^2$

NMOS detailled I-V characteristics

Saturation region: effect of channel pinching

- large-scale equivalent circuit
  - Current source has output impedance r_o
  - Valid for $v_{DS} \geq v_{GS} - V_T$



internal resistance can be exploited

Chapter 3: MOSFET

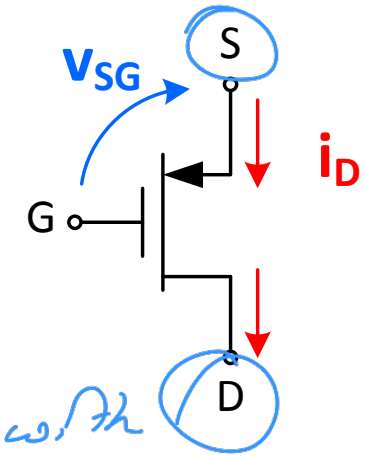
Outline

- Introduction to the MOSFET characteristics
- NMOS device structure
- NMOS detailled I-V characteristics
- PMOS and CMOS technology
- Complements on NMOS technology
- Depletion-type MOSFETs

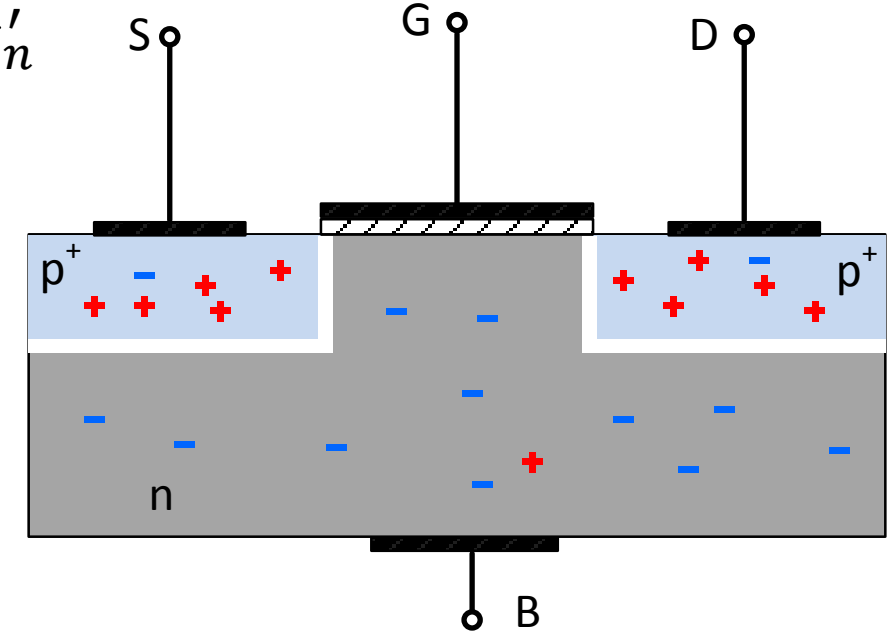
PMOS and CMOS technology

PMOS transistors

- Mobile charge carriers in the channel => holes
- A channel is created when $v_{SG} \geq V_{TH}$
- Saturation when $v_{SD} \geq v_{SG} - V_{TH}$
- The drain current (from source to drain) when saturating is $i_D = \frac{1}{2} k'_p \frac{W}{L} (v_{SG} - V_{TH})^2$
- Note that $k'_p \approx 0.25 k'_n$ to $0.5 k'_n$



inversed with NMOS



PMOS and CMOS technology

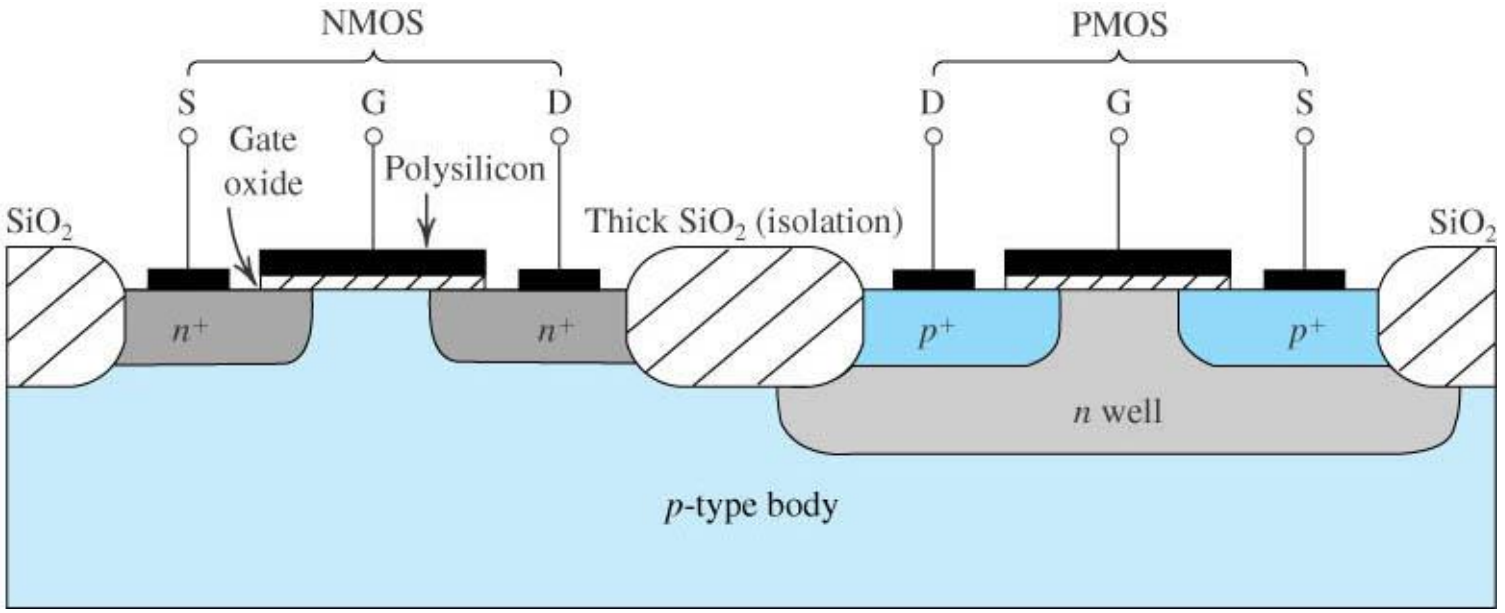
Complementary MOS (CMOS) transistors

Both NMOS and PMOS and same substrate

$\Rightarrow$ Many powerful circuit-design possibilities

$\Rightarrow$ Most widely used IC technology

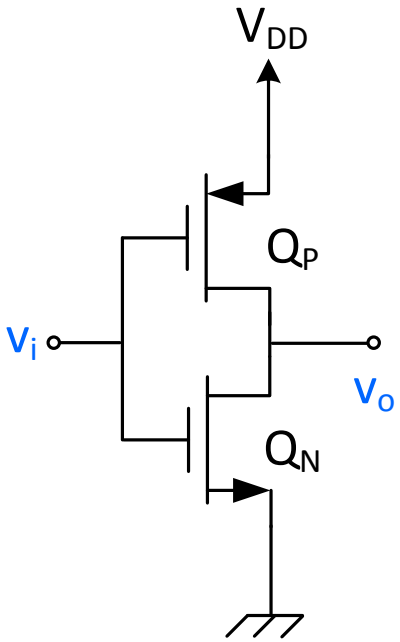
$\Rightarrow$ Many BJT applications now possible with CMOS



PMOS and CMOS technology

CMOS transistors

- CMOS = Combination of NMOS and PMOS
- Example: a CMOS inverter



If $\boldsymbol{v_i = V_{DD}}$

$\Rightarrow v_{SGP} = 0$ and $i_{DP} = 0$

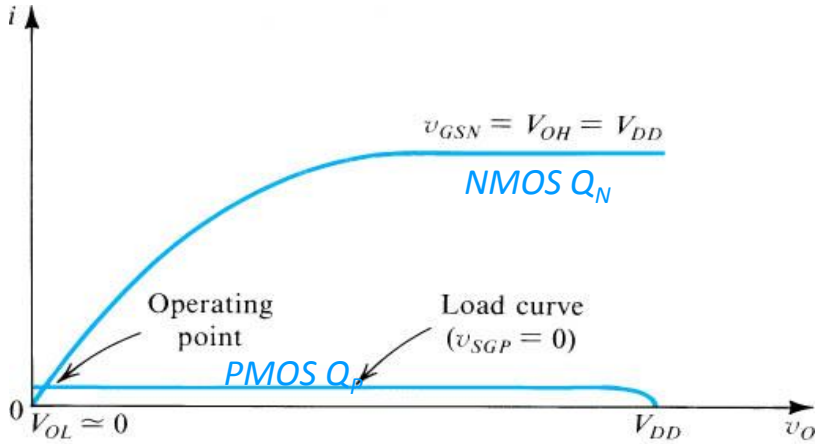
$\Rightarrow$ Transistor Q_P closed

$\Rightarrow i_{DN} = 0$ and $v_{GSN} = V_{DD}$

$\Rightarrow$ Only possible for $v_{DSN} = 0$

$\Rightarrow v_o = vDSN$

$\Rightarrow \boldsymbol{v_o = 0}$



PMOS and CMOS technology

CMOS transistors

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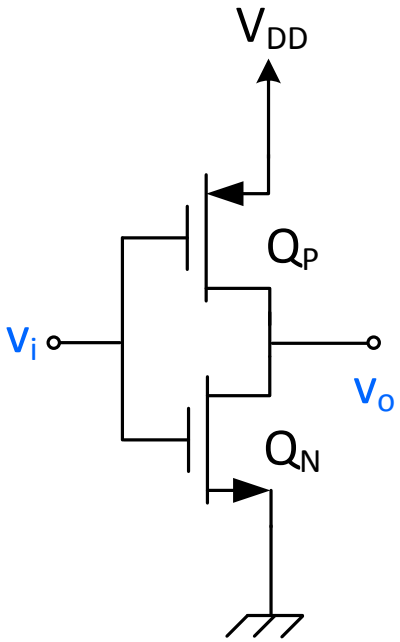
- Example: a CMOS inverter



If $\boldsymbol{v_i = 0}$

$\Rightarrow v_{GSN} = 0$ and $i_{DN} = 0$

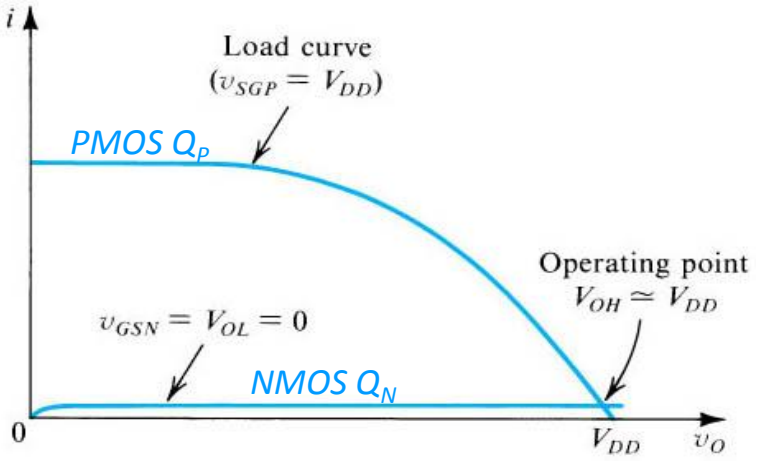
$\Rightarrow$ Transistor Q_N closed

$\Rightarrow i_{DP} = 0$ and $v_{SGP} = V_{DD}$

$\Rightarrow$ Only possible for $v_{SDP} = 0$

$\Rightarrow v_o = V_{DD} - v_{SDP}$

$\Rightarrow \boldsymbol{v_o = V_{DD}}$



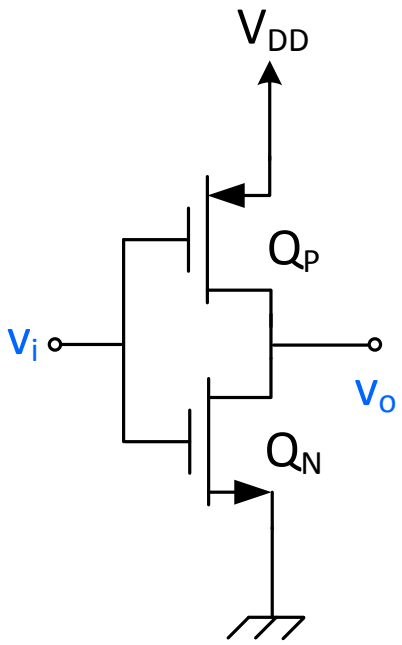
PMOS and CMOS technology

CMOS transistors

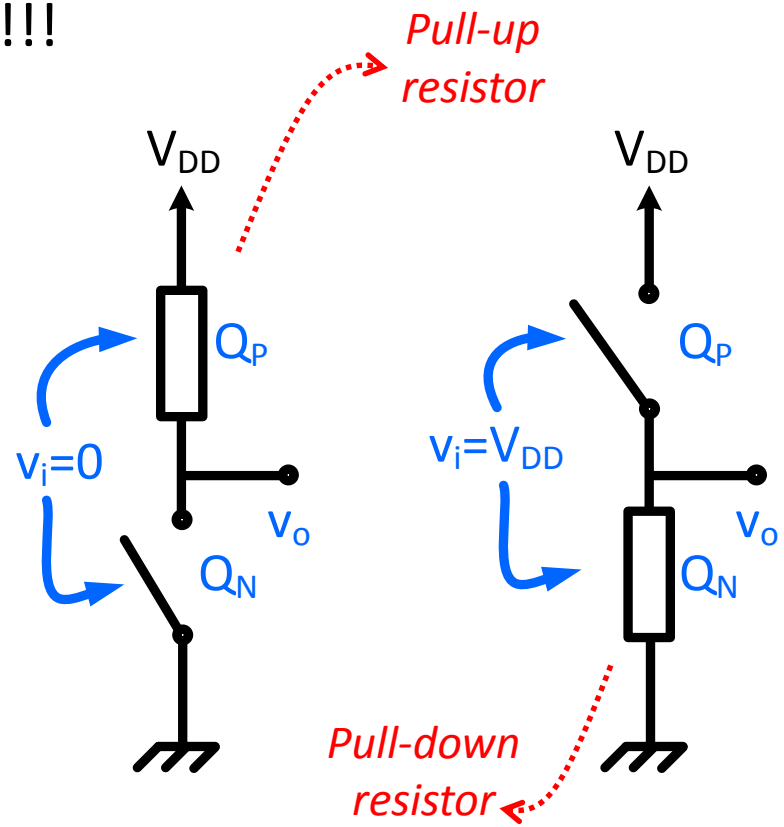
- CMOS can be seen as two switches

⇒ **No static current**

⇒ Very low current consumption !!!



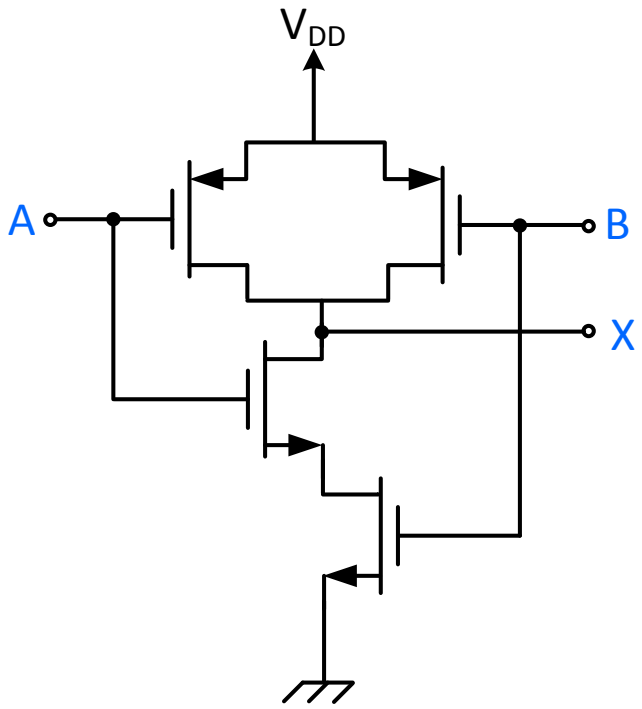
v_i	v_o
0	V_{DD}
V_{DD}	0



PMOS and CMOS technology

CMOS transistors

- NAND logic gate with CMOS transistors



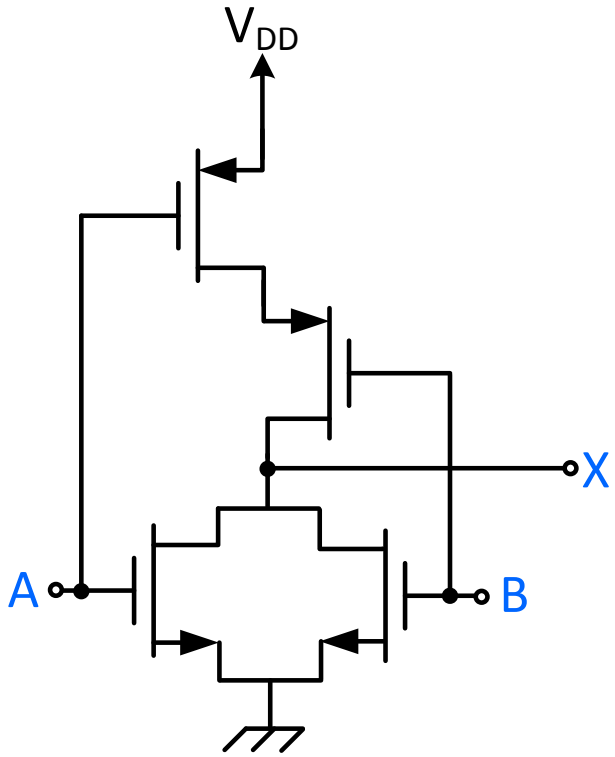
A	B	X
0	0	V_{DD}
0	V_{DD}	V_{DD}
V_{DD}	0	V_{DD}
V_{DD}	V_{DD}	0

Reminder: with NAND logic gates, you can create any sum of minterms => any combinatory function

PMOS and CMOS technology

CMOS transistors

- NOR logic gate with CMOS transistors



A	B	X
0	0	V_{DD}
0	V_{DD}	0
V_{DD}	0	0
V_{DD}	V_{DD}	0

Reminder: with NAND logic gates, you can create any sum of minterms => any combinatory function

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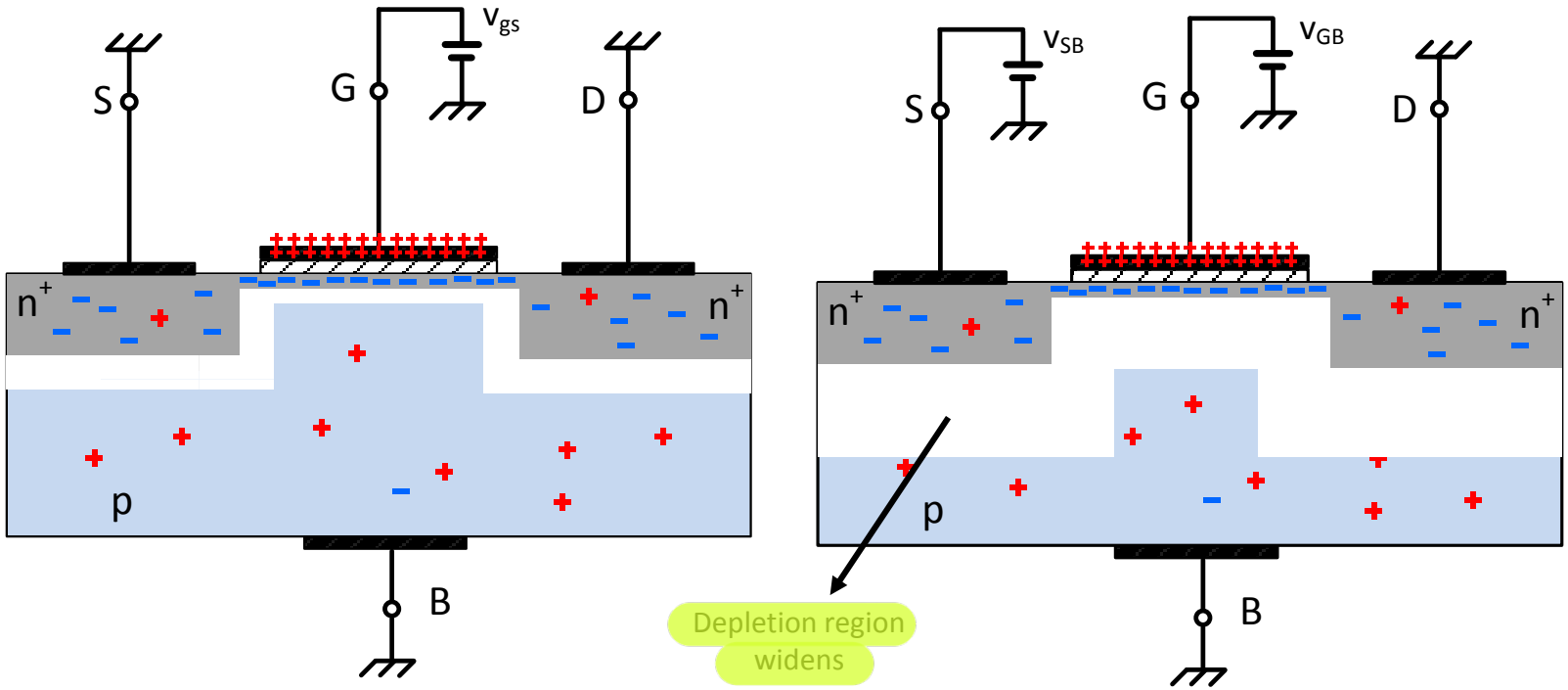
Complements on NMOS technology

Effects of the substrate

- v_{SB} not always zero
- Substrate common to many MOS transistors

  $\Rightarrow$ usually connected to most negative power supply in NMOS circuit

  $\Rightarrow$ V_{SB} may not be zero for all transistors!



Complements on NMOS technology

Effects of the substrate

- V_t changes with V_{SB}
- Depletion region widens
  - $\Rightarrow$ More negative ions in depletion region
  - $\Rightarrow$ Less electrons required to compensate positive charges at gate
  - $\Rightarrow$ n-type channel narrows

$\Rightarrow$ macroscopic effect: V_t increases

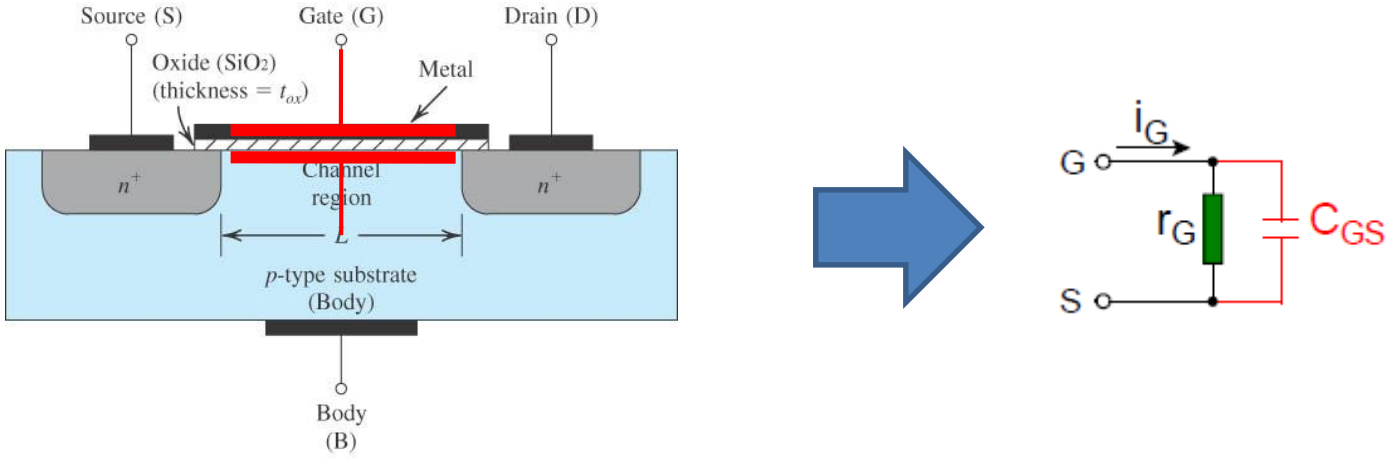
$$V_t = V_{t0} + \gamma \left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f} \right]$$

with $\gamma = \frac{\sqrt{2qN_d\varepsilon_S}}{C_{ox}}$

Complements on NMOS technology

NMOS input impedance

- Gate acts as capacitor with substrate



- Input resistance r_G very high (~10^{15} Ω) ↝ open circuit.
- C_{GS} ~ a few fF to some nF depending on size of NMOS ↝ not negligible (parasitic effect.)

⇒ purpose of i_G is to load C_{GS}

⇒ static i_G is zero

if problems: generally the ± effect

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Depletion-type MOSFET

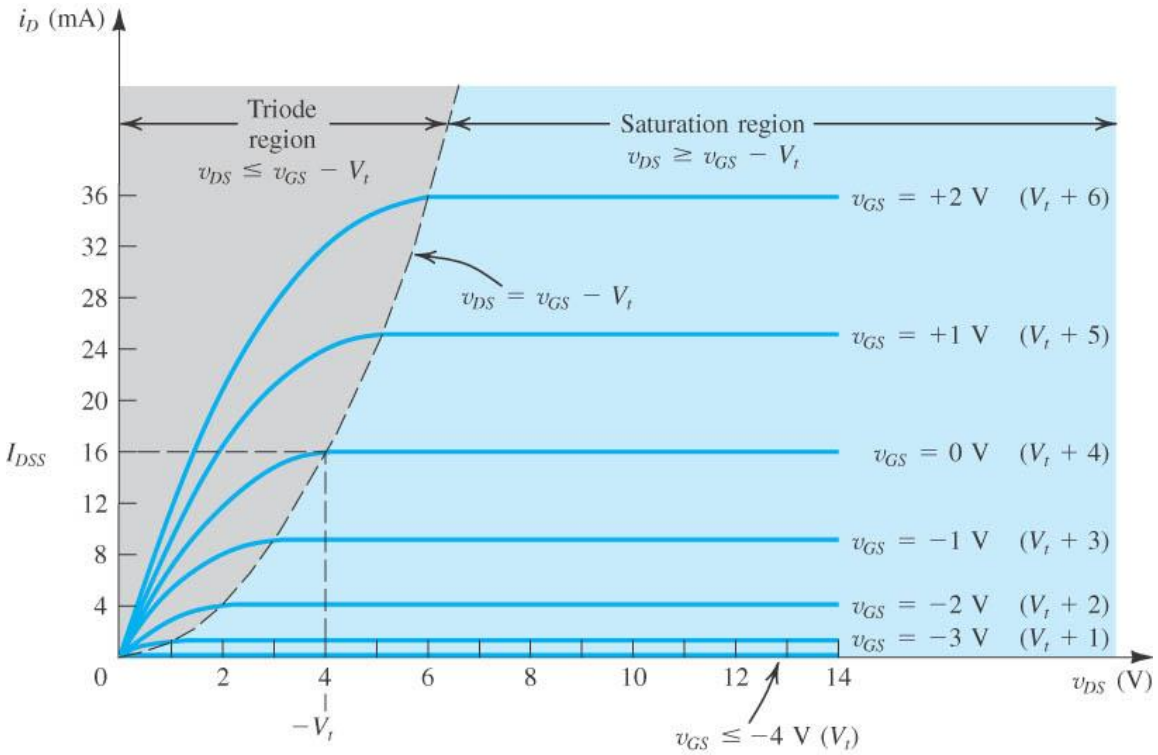
channel is physically implanted in MOSFET

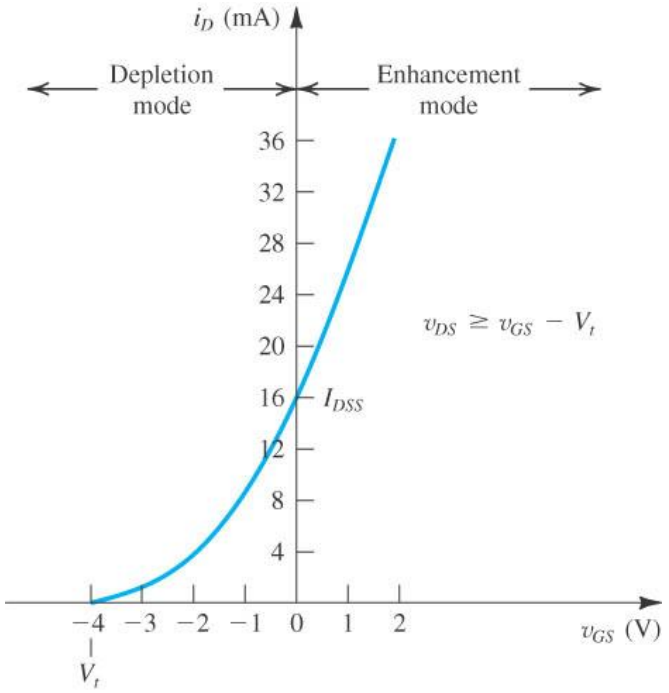
- For a NMOS, the channel is of type n
  - ⇒ A n-type silicon region is implanted between the n^+ source and the n^+ drain at the top of the p-type substrate
  - ⇒ If voltage v_{DS} is applied between drain and source, a current i_D flows, even for $v_{GS} = 0$
  - ⇒ There is no need to induce a channel
- Channel depth and conductivity is controlled through v_{GS}
  - ⇒ Positive v_{GS} : more electrons into channel => channel enhanced
  - ⇒ Negative v_{GS} : electrons repelled from channel => channel becomes shallower => conductivity decreases

Depletion-type MOSFET

I-V characteristics

- The curve $i_D = f(v_{GS})$ is shifted to the left





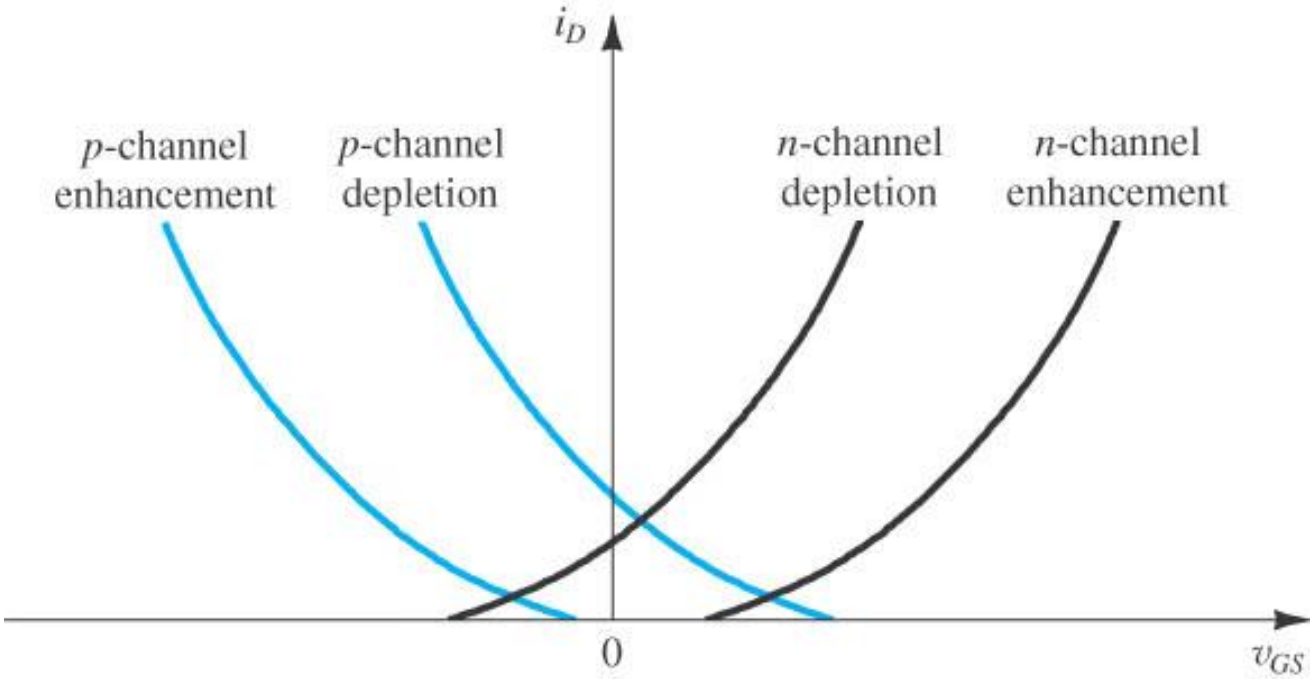
Depletion-type MOSFET

Enhancement-type vs depletion-type

- Enhancement-type and depletion-type MOSFET can be realized onto the same IC chip

  $\Rightarrow$ Circuits with improved characteristics

  $\Rightarrow$ See part on active loads in next chapter



Conclusions

- Transistors are created with semiconductors
  - Voltage at gate creates a channel that allows current to flow
  - Voltage at gate determines the width of the channel

  $\Rightarrow$ voltage-controlled current source
- MOSFET transistors have internal resistance
  - Due to channel pinching
- PMOS transistors are complementary of NMOS
  - PMOS + NMOS = CMOS

  $\Rightarrow$ CMOS offers interesting circuit for digital logic
- Depletion-type MOSFET have pre-implanted channel
  - No treshold voltage to have current flowing