ASSIGNMENT 4

Name: Ishan thakkar

ID NO.: - 21EL032

Division: - 04

Year: - 2023-24

Subject: - Digital System Design (3EL42)

Branch: - Electronics (EL)

1 BCD TIMECOUNT

Verilog code:-

```
module BCD_TimeCounter(
  input wire clk,        // Clock input
  input wire rst,        // Reset input
  output reg [3:0] bcd_seconds, // BCD representation of seconds
  output reg [3:0] bcd_minutes, // BCD representation of minutes
  output reg [3:0] bcd_hours    // BCD representation of hours
);

reg [3:0] seconds;
reg [3:0] minutes;
reg [3:0] hours;
```

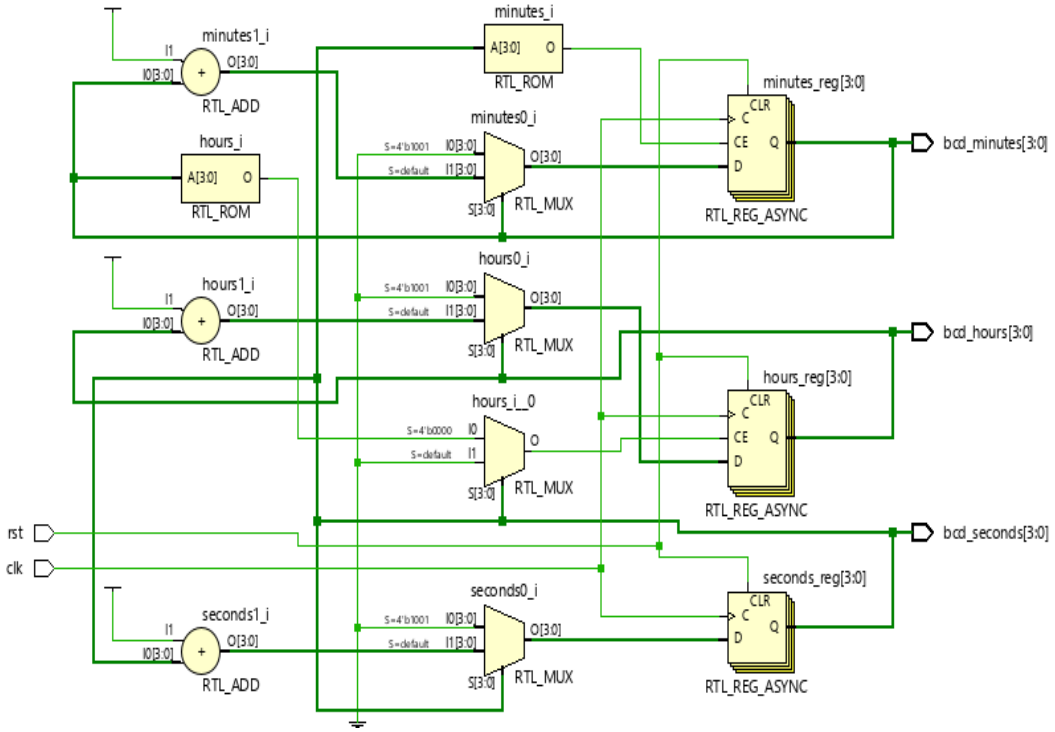
```
always @(posedge clk or posedge rst) begin
  if (rst) begin
    seconds <= 4'b0000;
    minutes <= 4'b0000;
    hours   <= 4'b0000;
  end else begin
    seconds <= (seconds == 4'b1001) ? 4'b0000 : seconds + 4'b0001;
    if (seconds == 4'b0000) begin
      minutes <= (minutes == 4'b1001) ? 4'b0000 : minutes + 4'b0001;
      if (minutes == 4'b0000) begin
        hours <= (hours == 4'b1001) ? 4'b0000 : hours + 4'b0001;
      end
    end
  end
end

always @(*) begin
  bcd_seconds = seconds;
  bcd_minutes = minutes;
  bcd_hours = hours;
end

endmodule
```

Testbench:-

```
module BCD_TimeCounter_Testbench;
reg clk;
reg rst;
wire [3:0] bcd_seconds;
```

```
wire [3:0] bcd_minutes;
wire [3:0] bcd_hours;

BCD_TimeCounter uut (
  .clk(clk),
  .rst(rst),
  .bcd_seconds(bcd_seconds),
  .bcd_minutes(bcd_minutes),
  .bcd_hours(bcd_hours)
);

initial begin
  clk = 0;
  rst = 0;

  rst = 1;
  #10 rst = 0;

  repeat (100) begin
    #5 clk = ~clk;
  end


  $display("Time: %d%d:%d%d:%d%d", bcd_hours, bcd_hours, bcd_minutes, bcd_minutes,
bcd_seconds, bcd_seconds);
  $finish;
end

endmodule
```

RTlsymatic:-



Synthesis report:-

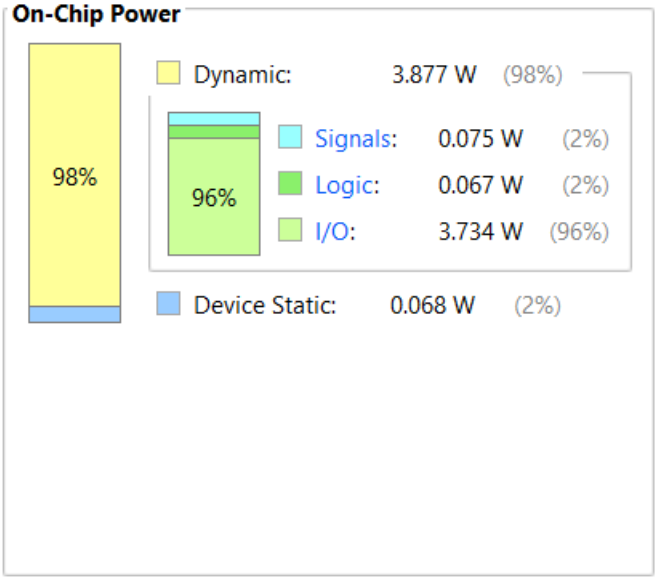
```
Start Writing Synthesis Report
------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+-+-----+------+
| |Cell |Count |
+-+-----+------+
+-+-----+------+
------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:31 ; elapsed = 00:00:35 . Memory (MB): peak = 1020.398 ; gain = 0.078
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**3.945 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**49.4°C**
Thermal Margin:	75.6°C (12.1 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



2 3-1 MUX

Verilog code:-

```
module mux3to1(
 input wire a,
 input wire b,
 input wire c,
 input wire sel,
 output wire y
);

assign y = (sel == 2'b00) ? a :
        (sel == 2'b01) ? b :
        (sel == 2'b10) ? c :
        (sel == 2'b11) ? 1'b0 : 1'bx;

Endmodule
```

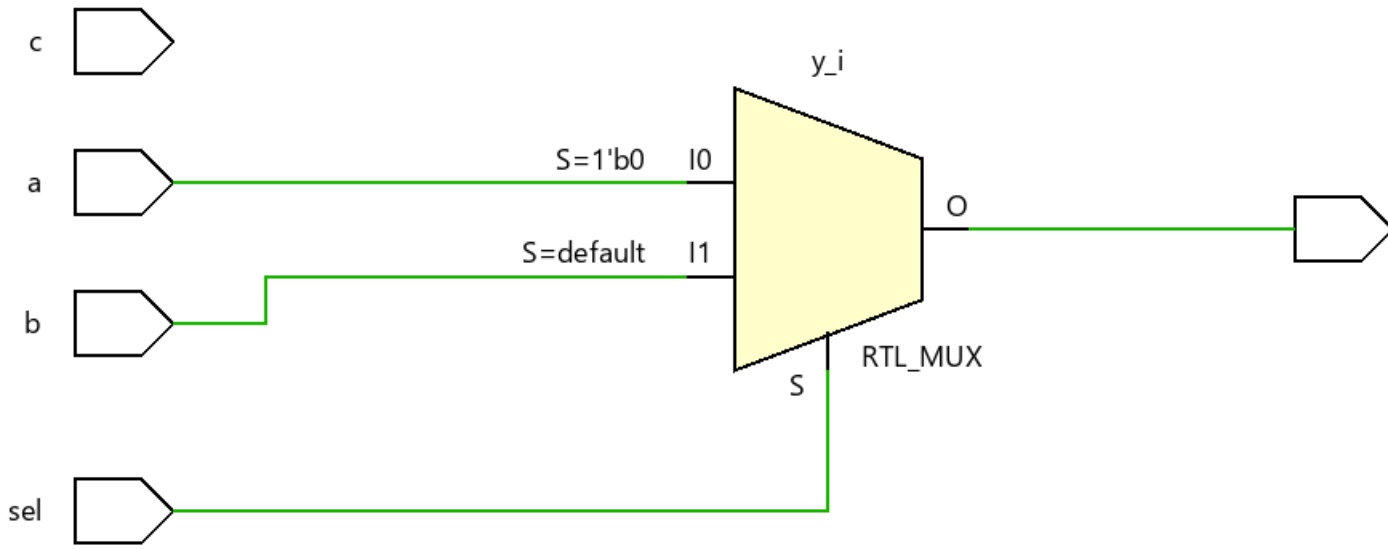
Testbench:-

```
module testbench_mux3to1;
```

```
reg a, b, c, sel;
// Output
wire y;


mux3to1 uut (
  .a(a),
  .b(b),
  .c(c),
  .sel(sel),
  .y(y)
);

initial begin

  a = 1'b0;
  b = 1'b1;
  c = 1'b1;
  sel = 2'b00;


  #10 sel = 2'b01;
  #10 sel = 2'b10;
  #10 sel = 2'b11;
```

```
  $finish;
 end


 always @(y) begin
  $display("y = %b", y);
 end

endmodule
```

Rtl symatic:-



Synthesis report:-

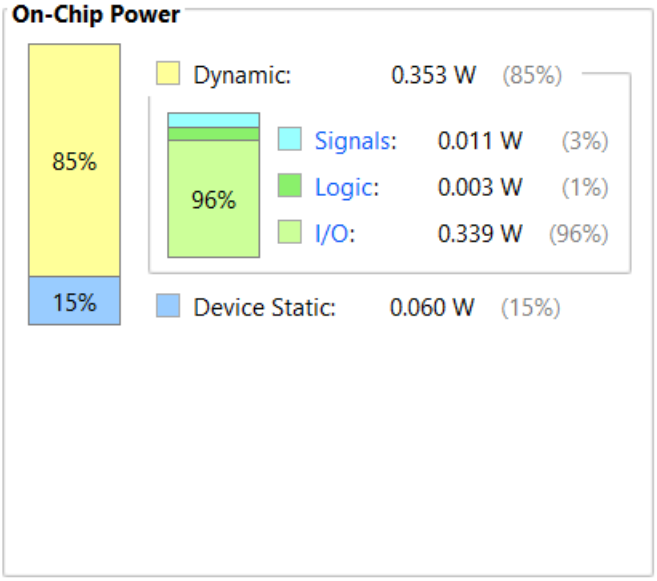
```
Start Writing Synthesis Report
-------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     1|
|2     |IBUF |     3|
|3     |OBUF |     1|
+------+-----+------+
-------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB):
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.413 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.6°C**
Thermal Margin:	97.4°C (15.6 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



3 BCD TO SEVEN SEGMENT DISPLAY

Verilog code:-

```
module bcd_to_7seg(
    input wire [3:0] bcd_in,
    output wire [6:0] seg_out
);
```

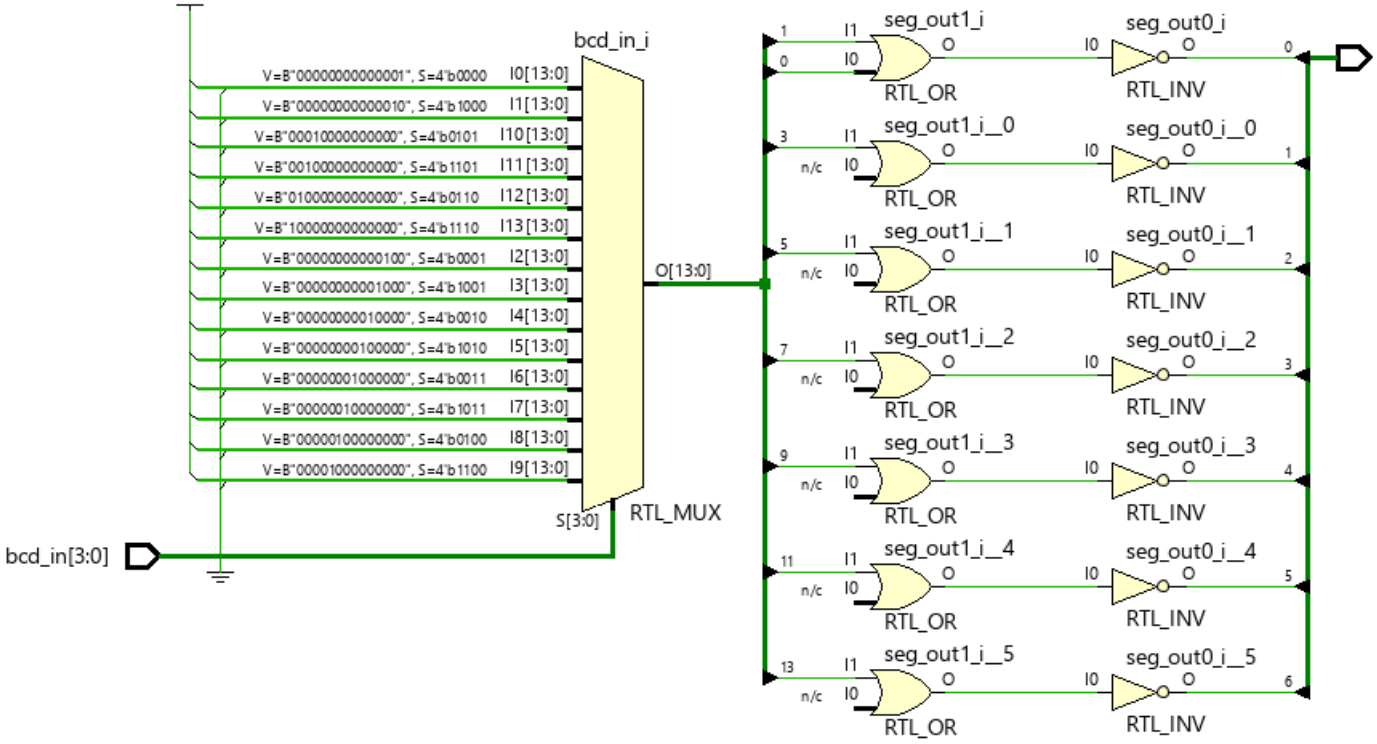
```
assign seg_out[0] = ~((bcd_in == 4'b0000) | (bcd_in == 4'b1000));
assign seg_out[1] = ~((bcd_in == 4'b0001) | (bcd_in == 4'b1001));
assign seg_out[2] = ~((bcd_in == 4'b0010) | (bcd_in == 4'b1010));
assign seg_out[3] = ~((bcd_in == 4'b0011) | (bcd_in == 4'b1011));
assign seg_out[4] = ~((bcd_in == 4'b0100) | (bcd_in == 4'b1100));
assign seg_out[5] = ~((bcd_in == 4'b0101) | (bcd_in == 4'b1101));
assign seg_out[6] = ~((bcd_in == 4'b0110) | (bcd_in == 4'b1110));

endmodule
```

Testbench:-

```
module testbench_bcd_to_7seg;

    reg [3:0] bcd_in;

    wire [6:0] seg_out;



    bcd_to_7seg uut (
        .bcd_in(bcd_in),
        .seg_out(seg_out)
    );



    initial begin
        $monitor("bcd_in = %b, seg_out = %b", bcd_in, seg_out);
        bcd_in = 4'b0000;
        #10 bcd_in = 4'b0001;
```

```
    #10 bcd_in = 4'b0010;
    #10 bcd_in = 4'b0011;
    #10 bcd_in = 4'b0100;
    #10 bcd_in = 4'b0101;
    #10 bcd_in = 4'b0110;
    #10 bcd_in = 4'b0111;
    #10 bcd_in = 4'b1000;
    #10 bcd_in = 4'b1001;
    #10 bcd_in = 4'b1010;
    #10 bcd_in = 4'b1100;
    #10 bcd_in = 4'b1111;
    $finish;
  end

endmodule
```

Rtl symatic:-



Synthesis report:-

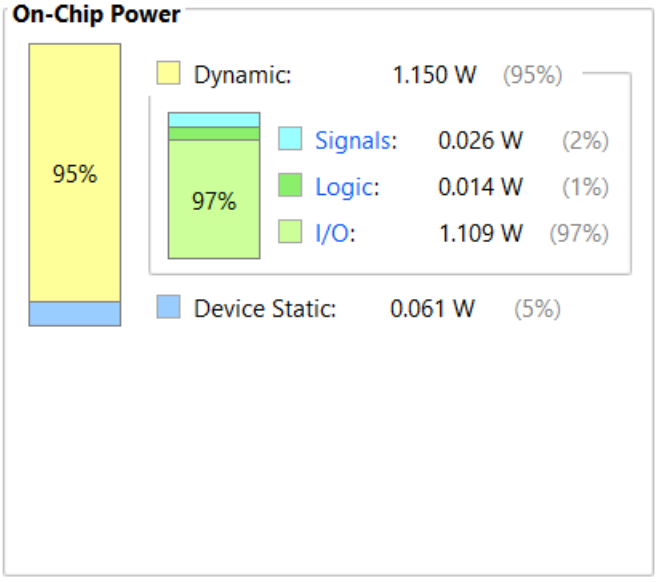
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     7|
|2     |IBUF |     3|
|3     |OBUF |     7|
+------+-----+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:19 ; elapsed = 00:00:25 . Memory (MB):
---------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.212 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**32.5°C**
Thermal Margin:	92.5°C (14.8 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



4 D LATCH USING 2:1 MUX

Verilog code:-

```
module d_latch_with_mux (
    input wire D,
```

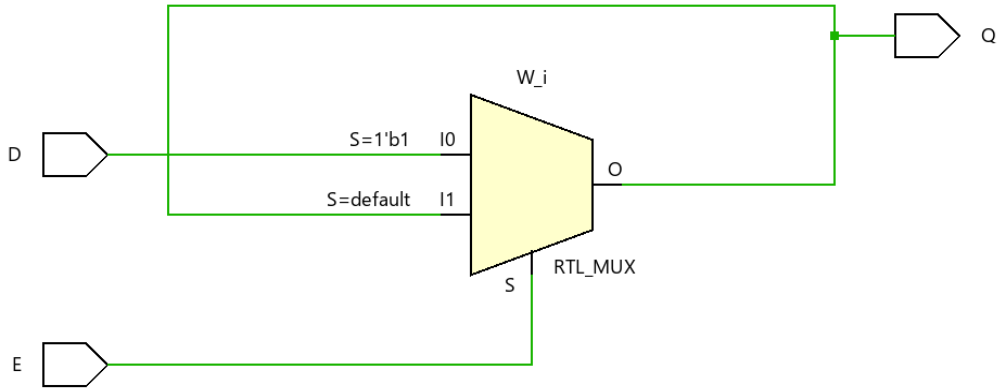
```
  input wire E,
  output wire Q
);

wire W;
assign W = (E) ? D : Q;

assign Q = W;

endmodule
```

Testbench:-

```
module testbench_d_latch_with_mux;

 reg D, E;


 wire Q;


 d_latch_with_mux uut (
  .D(D),
  .E(E),
  .Q(Q)
 );


 initial begin
  $monitor("D = %b, E = %b, Q = %b", D, E, Q);
```

```
    D = 1'b0;
    E = 1'b0;

    #10 E = 1'b1;
    D = 1'b1;


    #10 E = 1'b0;
    D = 1'b0;


    #10 E = 1'b1;
    D = 1'b1;


    #10 E = 1'b0;
    D = 1'b0;


    $finish;
  end

endmodule
```

RTlsymatic:-



Synthesis report:-

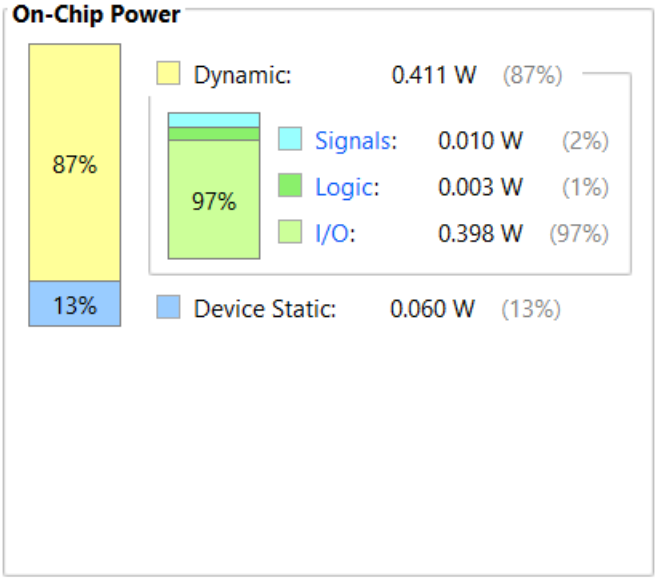
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     1|
|2     |IBUF |     2|
|3     |OBUF |     1|
+------+-----+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:21 ; elapsed = 00:00:23 . Memory (MB): peak = 1029.855 ; gain = 11.023
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.472 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.9°C**
Thermal Margin:	97.1°C (15.5 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



5 8-BIT BARREL SHIFTER

Verilog code:-

```
module barrel_shifter(
    input wire [7:0] data_in,    // Input data (8 bits)
    input wire [2:0] shift_amount, // Shift amount (0 to 7)
    input wire shift_left,      // Shift direction (0: right, 1: left)
    output wire [7:0] data_out  // Output data (8 bits)
);

    assign data_out = (shift_left) ? (data_in << shift_amount) : (data_in >> shift_amount);

endmodule
```

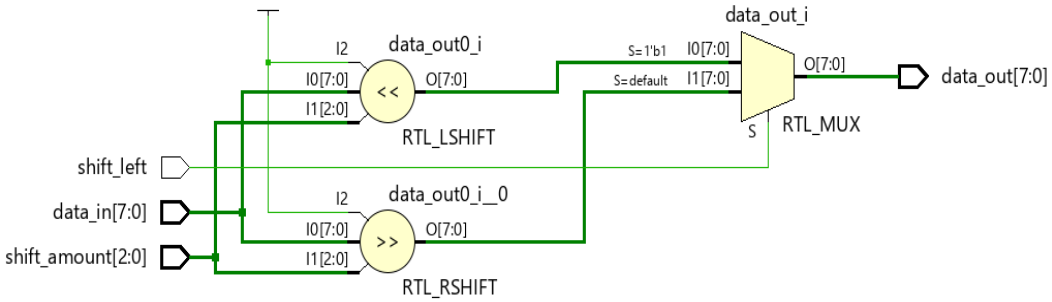
Testbench:-

```
module test_bench;
    reg [7:0] data_in;
    reg [2:0] shift_amount;
    reg shift_left;
    wire [7:0] data_out;
```

```
barrel_shifter uut (
    .data_in(data_in),
    .shift_amount(shift_amount),
    .shift_left(shift_left),
    .data_out(data_out)
);

initial begin
    $display("Testing Barrel Shifter");

    data_in = 8'b11001100;
    shift_amount = 3'b001;
    shift_left = 1'b0;

    #10 $display("Data In: %b", data_in);
    $display("Shift Amount: %b", shift_amount);
    $display("Shift Direction: %b", shift_left);
    #10 $display("Data Out: %b", data_out);

    data_in = 8'b11001100;
    shift_amount = 3'b001;
    shift_left = 1'b1;

    #10 $display("Data In: %b", data_in);
    $display("Shift Amount: %b", shift_amount);
    $display("Shift Direction: %b", shift_left);
    #10 $display("Data Out: %b", data_out);
```

```
        $finish;
    end
endmodule
```

RTlsymatic:-



Synthesis report:-

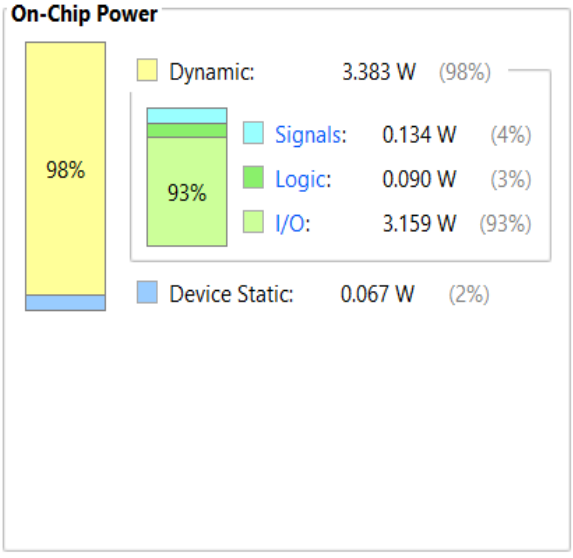
```
Start Writing Synthesis Report
------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     4|
|2     |LUT4 |     4|
|3     |LUT5 |     6|
|4     |LUT6 |    10|
|5     |IBUF |    12|
|6     |OBUF |     8|
+------+-----+------+
------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:20 ; elapsed = 00:00:25 . Memory (MB): peak = 1035.742 ; gain = 21.305
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**3.45 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**46.3°C**
Thermal Margin:	78.7°C (12.6 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



6 1-BIT COMPARATOR USING 4X1 MUX

Verilog code:-

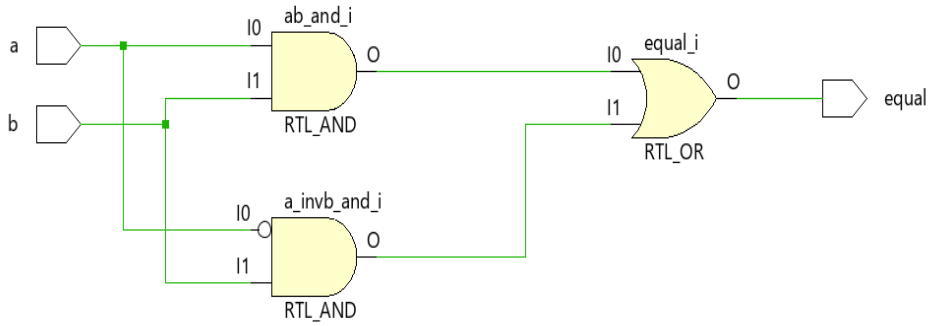
```
module comparator_1bit(
    input wire a,
    input wire b,
    output wire equal
);
    wire a_inv;
    wire b_inv;
    wire ab_and;
    wire a_invb_and;

    assign a_inv = ~a;
    assign b_inv = ~b;

    assign ab_and = a & b;
    assign a_invb_and = a_inv & b;

    assign equal = (ab_and | a_invb_and);

endmodule
```

Testbench:-

```
module test_bench;
    reg a;
    reg b;
    wire equal;
    comparator_1bit uut (
        .a(a),
```

```
        .b(b),
        .equal(equal)
    );

    initial begin
        $display("Testing 1-Bit Comparator");
        a = 1'b0;
        b = 1'b0;
        #10 $display("a: %b, b: %b, Equal: %b", a, b, equal);
        a = 1'b0;
        b = 1'b1;
        #10 $display("a: %b, b: %b, Equal: %b", a, b, equal);
        a = 1'b1;
        b = 1'b0;
        #10 $display("a: %b, b: %b, Equal: %b", a, b, equal);
        a = 1'b1;
        b = 1'b1;
        #10 $display("a: %b, b: %b, Equal: %b", a, b, equal);
        $finish;
    end
endmodule
```

RTLsymatic:-



Synthesis report:-

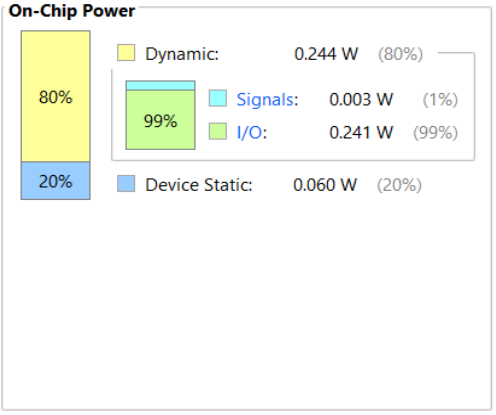
```
Start Writing Synthesis Report
-------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |IBUF |     1|
|2     |OBUF |     1|
+------+-----+------+
-------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:20 ; elapsed = 00:00:24 . Memory (MB): peak = 1020.594 ; gain = 3.348
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.304 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.9°C**
Thermal Margin:	98.1°C (15.7 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



7 LOGICAL, ALGEBRAIC, AND ROTATE SHIFT OPERATIONS

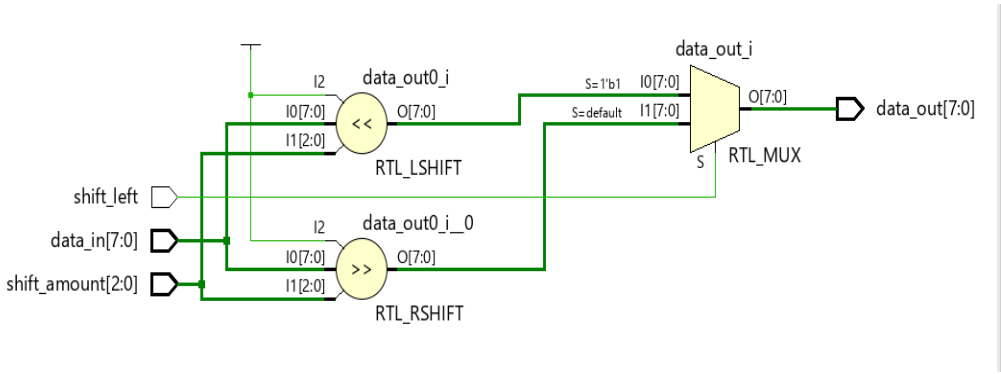
(1) Logical operation

Verilog code:-

```
module logical_shift(
input wire [7:0] data_in,
input wire [2:0] shift_amount,
input wire shift_left,
output wire [7:0] data_out
);

assign data_out = (shift_left) ? (data_in << shift_amount) : (data_in >> shift_amount);
```

endmodule

Rtlsymatic:-



Synthesis report:-

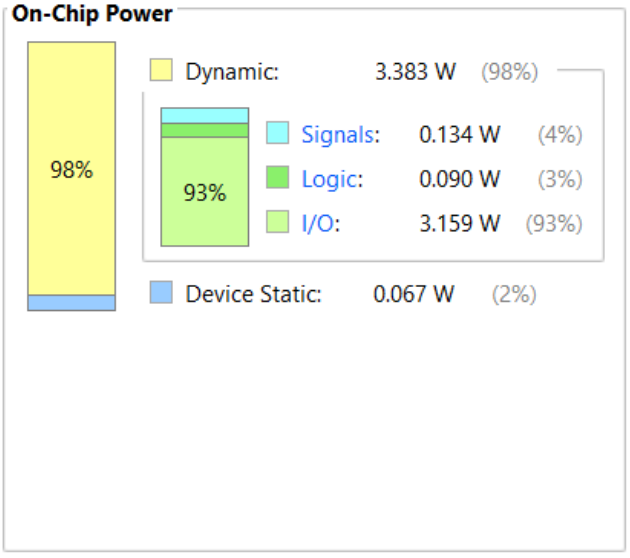
```
Start Writing Synthesis Report
-------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     4|
|2     |LUT4 |     4|
|3     |LUT5 |     6|
|4     |LUT6 |    10|
|5     |IBUF |    12|
|6     |OBUF |     8|
+------+-----+------+
-------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 1034.711 ; gain = 20.508
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**3.45 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**46.3°C**
Thermal Margin:	78.7°C (12.6 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

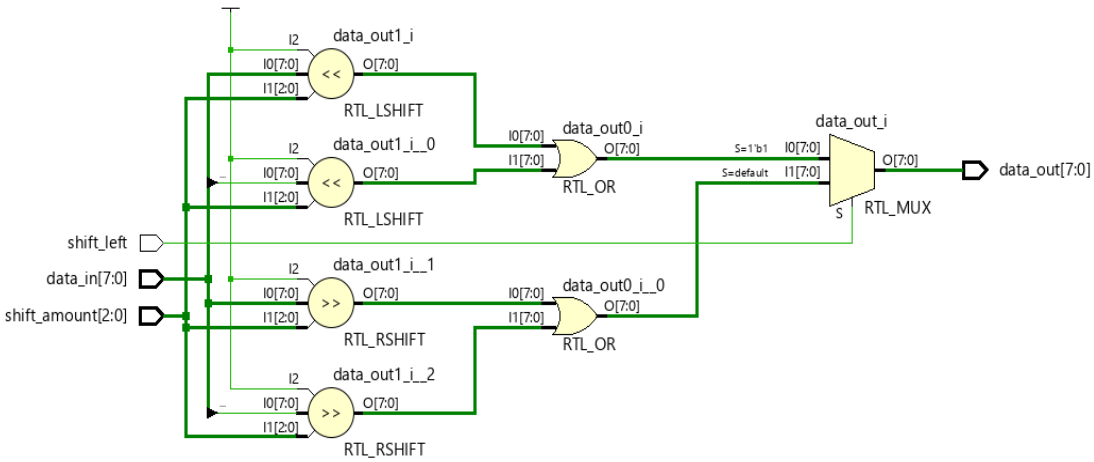


(2)Algebraic shift

Verilog code:-

```
module algebraic_shift(
   input wire [7:0] data_in,
   input wire [2:0] shift_amount,
   input wire shift_left,
   output wire [7:0] data_out
);

   assign data_out = (shift_left) ? ((data_in << shift_amount) | ({8{data_in[7]}} <<
shift_amount)) :
                                    ((data_in >> shift_amount) | ({8{data_in[7]}} >>
shift_amount));

Endmodule
```

RTlsymatic:-



Synthesis report:-

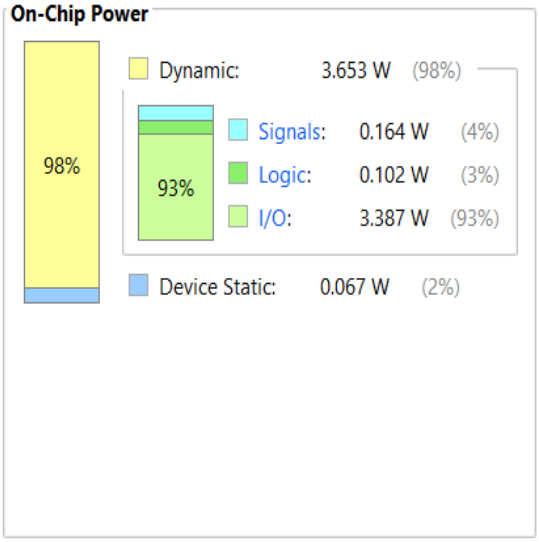
```
Start Writing Synthesis Report
------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+------+------+
|      |Cell  |Count |
+------+------+------+
|1     |LUT4  |     7|
|2     |LUT5  |    11|
|3     |LUT6  |    10|
|4     |MUXF7 |     3|
|5     |IBUF  |    12|
|6     |OBUF  |     8|
+------+------+------+
------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:19 ; elapsed = 00:00:25 . Memory (MB): peak = 1031.508 ; gain = 16.961
------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**3.72 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**48.0°C**
Thermal Margin:	77.0°C (12.3 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

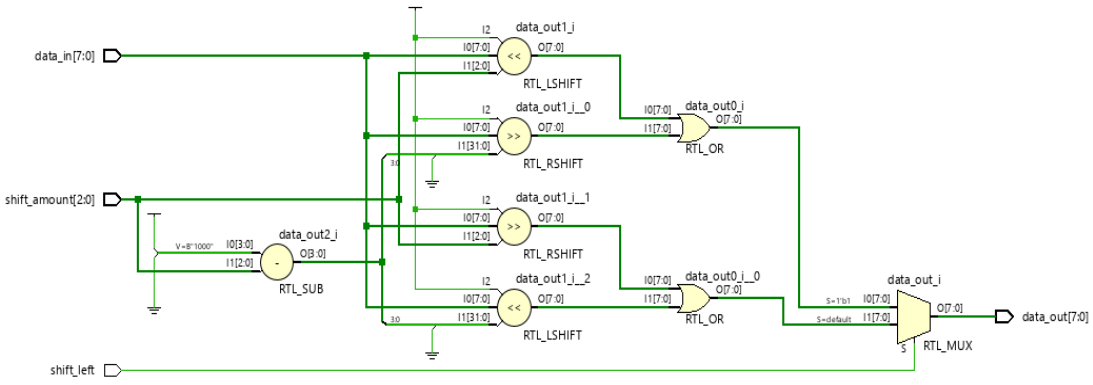


(3)Rotate shift:-

Verilog code:-

```
module rotate_shift(
   input wire [7:0] data_in,
   input wire [2:0] shift_amount,
   input wire shift_left,
   output wire [7:0] data_out
);

   assign data_out = (shift_left) ? (data_in << shift_amount) | (data_in >> (8 - shift_amount)) :
          (data_in >> shift_amount) | (data_in << (8 - shift_amount));

Endmodule
```

RTlsymatic:-



Synthesis report:-

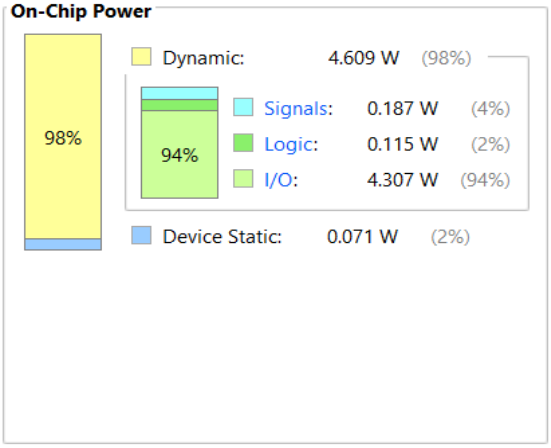
```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT6 |    24|
|2     |IBUF |    12|
|3     |OBUF |     8|
+------+-----+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:18 ; elapsed = 00:00:25 . Memory (MB): peak = 1035.004 ; gain = 17.523
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**4.68 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**53.9°C**
Thermal Margin:	46.1°C (7.4 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Test bench:-

```
module test_bench;
  reg [7:0] data_in;
  reg [2:0] shift_amount;
  reg shift_left;
  wire [7:0] logical_shift_left;
  wire [7:0] logical_shift_right;
  wire [7:0] algebraic_shift_left;
  wire [7:0] algebraic_shift_right;
  wire [7:0] rotate_shift_left;
  wire [7:0] rotate_shift_right;

  logical_shift uut_logical_shift_left (
    .data_in(data_in),
    .shift_amount(shift_amount),
    .shift_left(1'b1),
    .data_out(logical_shift_left)
```

```
);

logical_shift uut_logical_shift_right (
   .data_in(data_in),
   .shift_amount(shift_amount),
   .shift_left(1'b0),
   .data_out(logical_shift_right)
);

algebraic_shift uut_algebraic_shift_left (
   .data_in(data_in),
   .shift_amount(shift_amount),
   .shift_left(1'b1),
   .data_out(algebraic_shift_left)
);

algebraic_shift uut_algebraic_shift_right (
   .data_in(data_in),
   .shift_amount(shift_amount),
   .shift_left(1'b0),
   .data_out(algebraic_shift_right)
);

rotate_shift uut_rotate_shift_left (
   .data_in(data_in),
   .shift_amount(shift_amount),
   .shift_left(1'b1),
   .data_out(rotate_shift_left)
);

rotate_shift uut_rotate_shift_right (
   .data_in(data_in),
   .shift_amount(shift_amount),
   .shift_left(1'b0),
   .data_out(rotate_shift_right)
);

initial begin
   $display("Testing Shift Operations");

   data_in = 8'b11001100;
   shift_amount = 3'b001;
   shift_left = 1'b1;
```

```
    #10 $display("Data In: %b", data_in);
    $display("Shift Amount: %b", shift_amount);
    $display("Logical Shift Left: %b", logical_shift_left);
    $display("Logical Shift Right: %b", logical_shift_right);
    $display("Algebraic Shift Left: %b", algebraic_shift_left);
    $display("Algebraic Shift Right: %b", algebraic_shift_right);
    $display("Rotate Shift Left: %b", rotate_shift_left);
    $display("Rotate Shift Right: %b", rotate_shift_right);

    $finish;
  end
endmodule
```

8 ALU

Verilog code:-

```
module alu(
        input [7:0] A,B,
        input [3:0] ALU_Sel,
        output [7:0] ALU_Out,
        output CarryOut
  );
  reg [7:0] ALU_Result;
  wire [8:0] tmp;
  assign ALU_Out = ALU_Result;
  assign tmp = {1'b0,A} + {1'b0,B};
  assign CarryOut = tmp[8];
  always @(*)
  begin
    case(ALU_Sel)
    4'b0000:
      ALU_Result = A + B ;
    4'b0001:
      ALU_Result = A - B ;
    4'b0010:
      ALU_Result = A * B;
    4'b0011:
      ALU_Result = A/B;
    4'b0100:
      ALU_Result = A<<1;
     4'b0101:
      ALU_Result = A>>1;
     4'b0110:
```

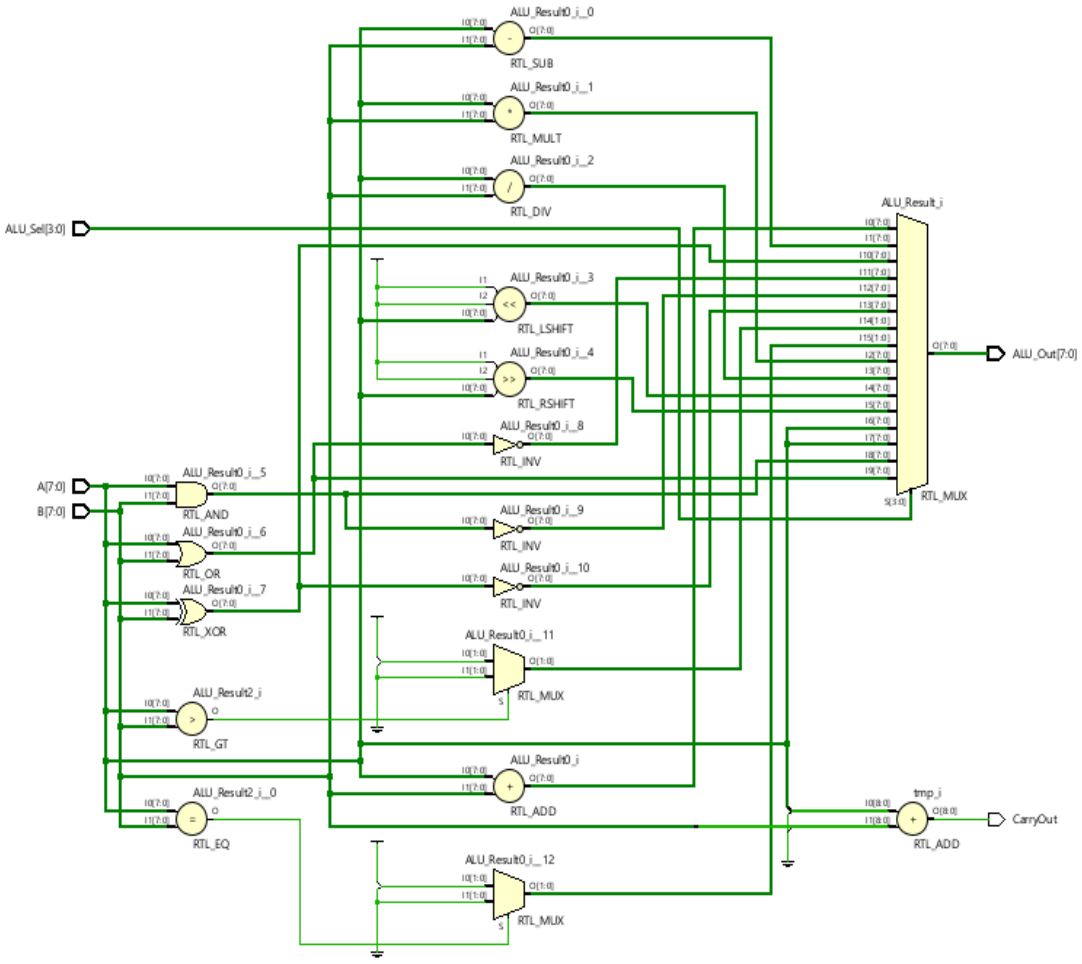
```
        ALU_Result = {A[6:0],A[7]};
      4'b0111:
        ALU_Result = {A[0],A[7:1]};
      4'b1000:
        ALU_Result = A & B;
      4'b1001:
        ALU_Result = A | B;
      4'b1010:
        ALU_Result = A ^ B;
      4'b1011:
        ALU_Result = ~(A | B);
      4'b1100:
        ALU_Result = ~(A & B);
      4'b1101:
        ALU_Result = ~(A ^ B);
      4'b1110:
        ALU_Result = (A>B)?8'd1:8'd0 ;
      4'b1111:
        ALU_Result = (A==B)?8'd1:8'd0 ;
      default: ALU_Result = A + B ;
    endcase
  end

endmodule
```

Test bench:-

```
module tb_alu;
reg[7:0] A,B;
 reg[3:0] ALU_Sel;

wire[7:0] ALU_Out;
 wire CarryOut;

 integer i;
 alu test_unit(
        A,B,
        ALU_Sel,
        ALU_Out,
        CarryOut
   );
  initial begin
```

```
    A = 8'h0A;
    B = 4'h02;
    ALU_Sel = 4'h0;

    for (i=0;i<=15;i=i+1)
    begin
     ALU_Sel = ALU_Sel + 8'h01;
     #10;
    end;

    A = 8'hF6;
    B = 8'h0A;

   end
endmodule
```

RTLsymatic:-



Synthesis report:-

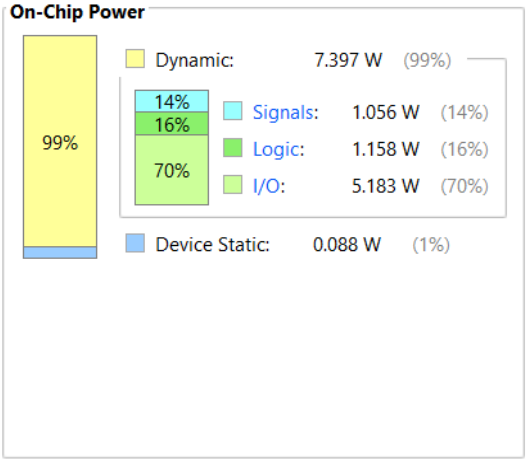
```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |CARRY4 |    34|
|2     |LUT2   |    53|
|3     |LUT3   |    51|
|4     |LUT4   |    26|
|5     |LUT5   |    17|
|6     |LUT6   |    31|
|7     |MUXF7  |     7|
|8     |IBUF   |    20|
|9     |OBUF   |     9|
+------+-------+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:16 ; elapsed = 00:00:25 . Memory (MB): peak = 1039.219 ; gain = 23.547
--------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**7.485 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**71.3°C**
Thermal Margin:	53.7°C (8.5 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



9 4-BIT ASYNCHRONOUS DOWN COUNTER

Verilog code:-

```
module down_counter_4bit(
   input wire clk,         // Clock input
   input wire reset,       // Reset input (active low)
   output reg [3:0] count   // 4-bit counter output
);

   always @(posedge clk or negedge reset) begin
      if (!reset) begin
         count <= 4'b1111;  // Reset the counter to its maximum value
      end else begin
         if (count > 4'b0000) begin
```

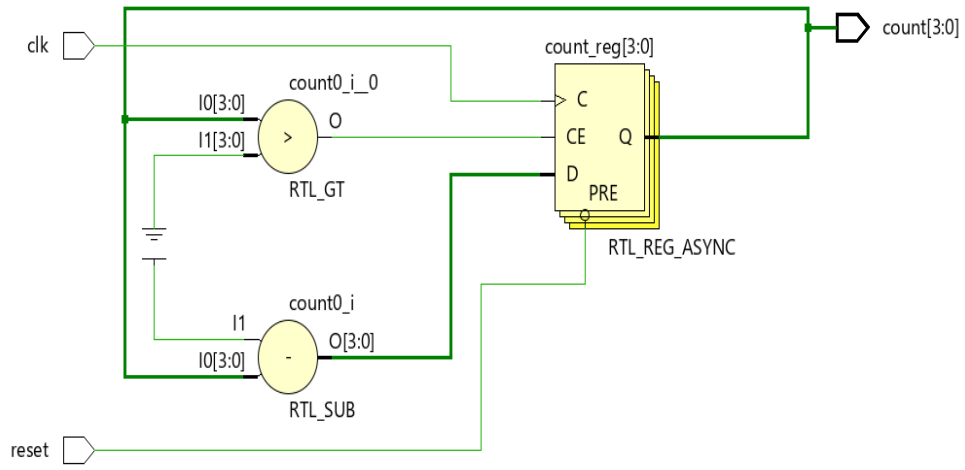
```
            count <= count - 1;  // Decrement the counter
        end
    end
  end

endmodule
```

Test bench:-

```
module test_bench_down_counter;
  reg clk;
  reg rst;
  wire [3:0] count;

  down_counter_4bit uut (
    .clk(clk),
    .rst(rst),
    .count(count)
  );

  initial begin
    $display("Testing 4-bit Asynchronous Down Counter");

    clk = 0;
    rst = 0;

    #10 rst = 1;
    #10 rst = 0;

    #50;

    $display("Counter Value: %b", count);


    #100;


    $display("Counter Value: %b", count);

    $finish;
  end

  always begin
    #5 clk = ~clk;
```

```
    end
endmodule
```

RTLsymatic:-



Synthesis report:-

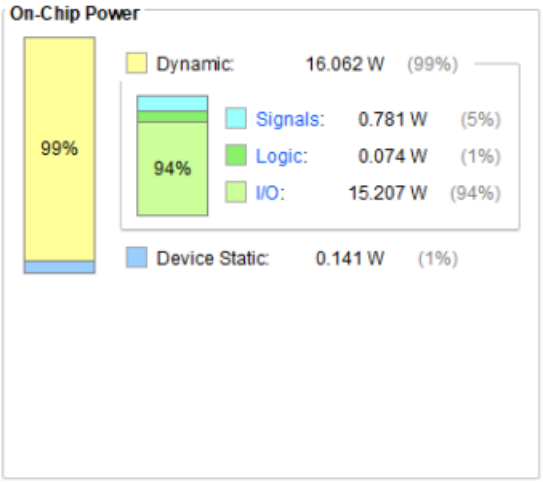
```
Start Writing Synthesis Report
------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT1 |     4|
|3     |FDCE |     4|
|4     |IBUF |     2|
|5     |OBUF |     8|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    19|
|2     |  dff1   |dff    |     2|
|3     |  dff2   |dff_0  |     2|
|4     |  dff3   |dff_1  |     2|
|5     |  dff4   |dff_2  |     2|
+------+---------+-------+------+
------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:27 ; elapsed = 00:00:37 . Memory (MB): peak = 1017.906 ; gain = 0.000
------------------------------------------------------------------------------
```

Power report:-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**16.203 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**55.5°C**
Thermal Margin:	29.5°C (15.5 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



10 MOD-N UPDOWN COUNTER

Verilog code:-

```
module up_down_counter (
   input wire clk,
   input wire rst,
   input wire up,
   output wire [3:0] count
);

   reg [3:0] count_reg;

   always @(posedge clk or posedge rst) begin
      if (rst) begin
         count_reg <= 4'b0000;
      end else if (up) begin

         if (count_reg == 4'b0111)
            count_reg <= 4'b0000;
         else
            count_reg <= count_reg + 1;
      end else begin

         if (count_reg == 4'b0000)
            count_reg <= 4'b0111;
         else
            count_reg <= count_reg - 1;
      end
   end

   assign count = count_reg;
```

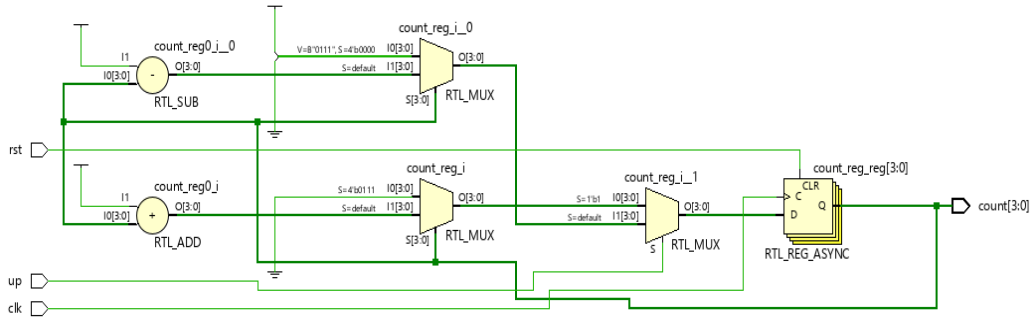
```
endmodule
```

Testbench:-

```
module test_bench;

   reg clk;
   reg rst;
   reg up;
   wire [3:0] count;

   up_down_counter uut (
      .clk(clk),
      .rst(rst),
      .up(up),
      .count(count)
   );


   always begin
      #5 clk = ~clk;
   end

   initial begin

      clk = 0;
      rst = 0;
      up = 1;


      rst = 1;
      #10 rst = 0;


      #50 up = 1;
      #100 up = 0;
      #100 up = 1;
      #100 up = 0;


      $finish;
   end


   always @(posedge clk) begin
```

```
    $display("Count: %b", count);
  end

endmodule
```

RTlsymatic:-



Synthesis report:-

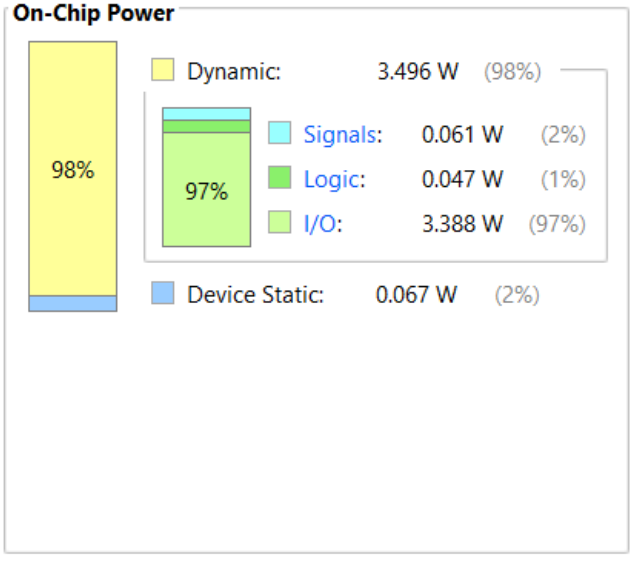
```
Start Writing Synthesis Report
-------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+-+-----+------+
| |Cell |Count |
+-+-----+------+
+-+-----+------+
-------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:22 ; elapsed = 00:00:24 . Memory (MB): peak = 1019.258 ; gain = 4.250
-------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**3.563 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**47.0°C**
Thermal Margin:	53.0°C (8.5 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



11 UNIVERSAL BINARY COUNTER

Verilog code:-

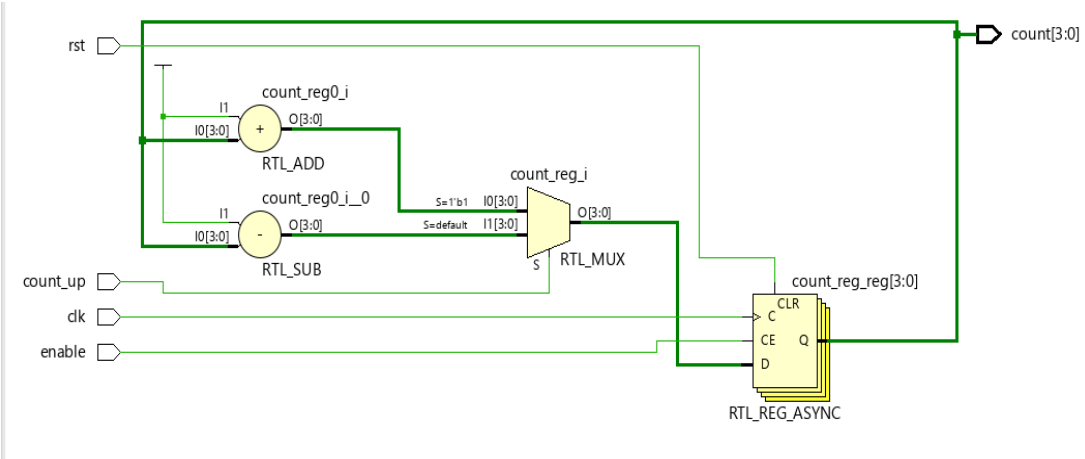
```
module universal_binary_counter (
  input wire clk,
  input wire rst,
  input wire enable,
  input wire count_up,
  output wire [3:0] count
);

  reg [3:0] count_reg;

  always @(posedge clk or posedge rst) begin
    if (rst) begin
      count_reg <= 4'b0000;
    end else if (enable) begin
      if (count_up) begin
        count_reg <= count_reg + 4'b0001;
      end else begin
        count_reg <= count_reg - 4'b0001;
      end
    end
  end

  assign count = count_reg;

endmodule
```

Test bench:-

```
module tb_universal_binary_counter;
  reg clk;
  reg rst;
  reg enable;
  reg count_up;
  wire [3:0] count;


  universal_binary_counter uut (
    .clk(clk),
    .rst(rst),
    .enable(enable),
    .count_up(count_up),
    .count(count)
  );
```

```
  always begin
    #5 clk = ~clk;
  end

  initial begin

    clk = 0;
    rst = 0;
    enable = 1;
    count_up = 1;


    rst = 1;
    #10 rst = 0;


    $display("Counting Up:");
    for (int i = 0; i < 16; i = i + 1) begin
      #5;
      $display("Count: %b", count);
    end


    $display("Counting Down:");
    count_up = 0;
    for (int i = 15; i >= 0; i = i - 1) begin
      #5;
      $display("Count: %b", count);
    end

    $finish;
  end
endmodule
```

RTL symatic:-



Synthesis report:-

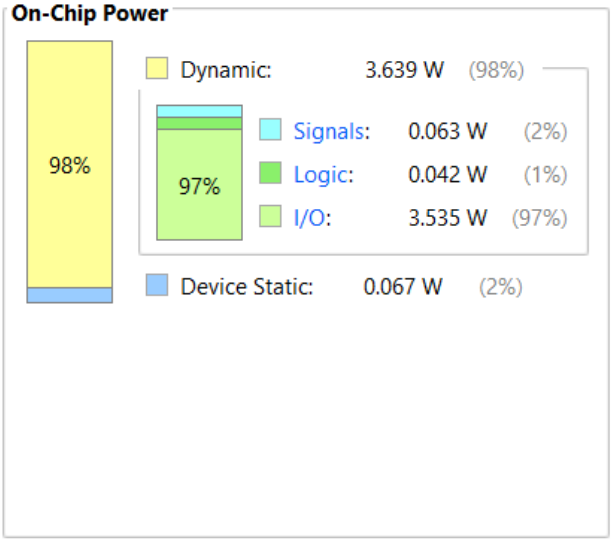
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT1 |     1|
|3     |LUT3 |     1|
|4     |LUT4 |     1|
|5     |LUT5 |     1|
|6     |FDCE |     4|
|7     |IBUF |     4|
|8     |OBUF |     4|
+------+-----+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:20 ; elapsed = 00:00:24 . Memory (MB): peak = 1029.250 ; gain = 10.988
---------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**3.707 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**47.9°C**
Thermal Margin:	77.1°C (12.3 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



12 UNIVERSAL SHIFT REGISTER

Verilog code:-

```
module universal_shift_register (
  input wire clk,
  input wire rst,
  input wire shift_left,
  input wire shift_right,
  input wire enable,
  input wire [3:0] data_in,
  output wire [3:0] data_out
);

  reg [3:0] shift_reg;

  always @(posedge clk or posedge rst) begin
    if (rst) begin
      shift_reg <= 4'b0000;
    end else if (enable) begin
      if (shift_left) begin
        shift_reg <= {shift_reg[2:0], data_in[0]};
      end else if (shift_right) begin
        shift_reg <= {data_in[3], shift_reg[3:1]};
      end
    end
  end

  assign data_out = shift_reg;

endmodule
```

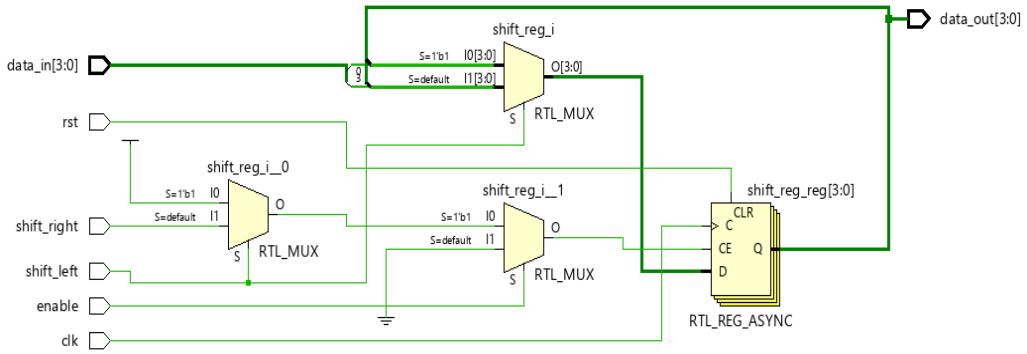
Test bench:-

```
module tb_universal_shift_register;
  reg clk;
  reg rst;
  reg shift_left;
  reg shift_right;
  reg enable;
  wire [3:0] data_in;
  wire [3:0] data_out;



  universal_shift_register uut (
    .clk(clk),
    .rst(rst),
    .shift_left(shift_left),
    .shift_right(shift_right),
```

```
  .enable(enable),
  .data_in(data_in),
  .data_out(data_out)
);


always begin
  #5 clk = ~clk;
end

initial begin

  clk = 0;
  rst = 0;
  shift_left = 1;
  shift_right = 0;
  enable = 1;
  data_in = 4'b1101;


  rst = 1;
  #10 rst = 0;


  $display("Left Shift:");
  for (int i = 0; i < 4; i = i + 1) begin
    #5;
    $display("Data Out: %b", data_out);
    data_in = data_in << 1;
  end


  $display("Right Shift:");
  shift_left = 0;
  shift_right = 1;
  data_in = 4'b1101;
  for (int i = 0; i < 4; i = i + 1) begin
    #5;
    $display("Data Out: %b", data_out);
    data_in = data_in >> 1;
  end

  $finish;
end
```

endmodule

RTlsymatic:-



Synthesis report:-

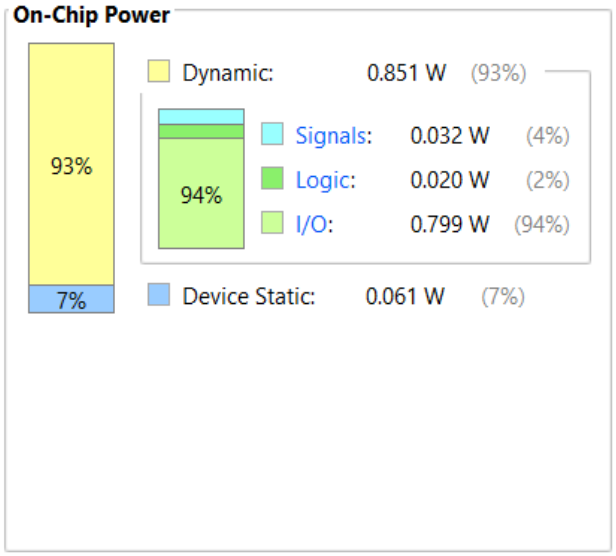
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT3 |     5|
|3     |FDCE |     4|
|4     |IBUF |     7|
|5     |OBUF |     4|
+------+-----+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:33 ; elapsed = 00:00:44 . Memory (MB): peak = 1032.137 ; gain = 15.234
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.912 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.6°C**
Thermal Margin:	94.4°C (15.1 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



13 : CN(CHANGE-NO CHANGE FLIPFLOP) USING 2:1 MUX

Verilog code:-

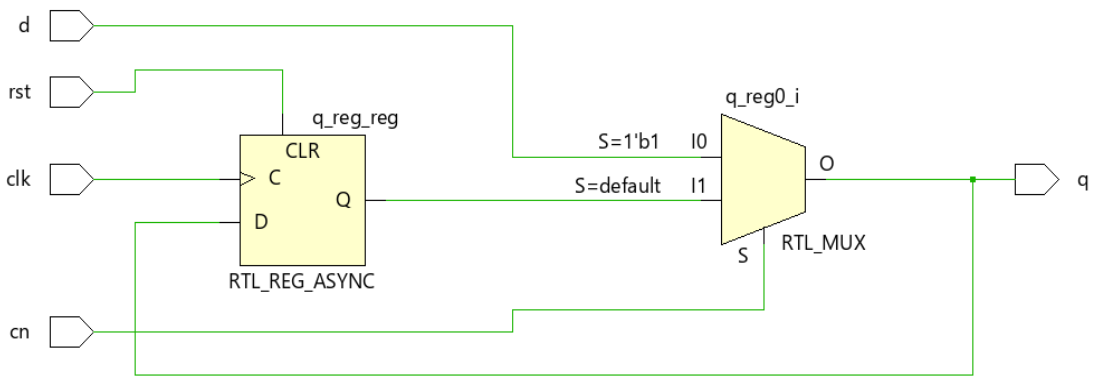
```
module cn_flip_flop (
  input wire clk,
  input wire rst,
  input wire cn,
  input wire d,
  output wire q
);

  reg q_reg;
  wire mux_out;


  always @(posedge clk or posedge rst) begin
    if (rst) begin
      q_reg <= 1'b0;
    end else if (cn) begin
      q_reg <= d;
    end
  end


  assign mux_out = cn ? d : q_reg;

  assign q = mux_out;

endmodule
```

Test bench:-

```
module tb_cn_flip_flop;
  reg clk;
  reg rst;
  reg cn;
  reg d;
  wire q;


  cn_flip_flop uut (
    .clk(clk),
    .rst(rst),
    .cn(cn),
    .d(d),
    .q(q)
```

```
  );


  always begin
    #5 clk = ~clk;
  end

  initial begin

    clk = 0;
    rst = 0;
    cn = 0;
    d = 0;


    rst = 1;
    #10 rst = 0;


    $display("Clock | CN | D | Q");
    $display("------|----|---|---");
    for (int i = 0; i < 8; i = i + 1) begin
      d = $random % 2;
      cn = $random % 2;
      #5;
      $display("%4b | %2b | %1b | %1b", clk, cn, d, q);
    end

    $finish;
  end
endmodule
```

RTlsymatic:-



Synthesis report:-

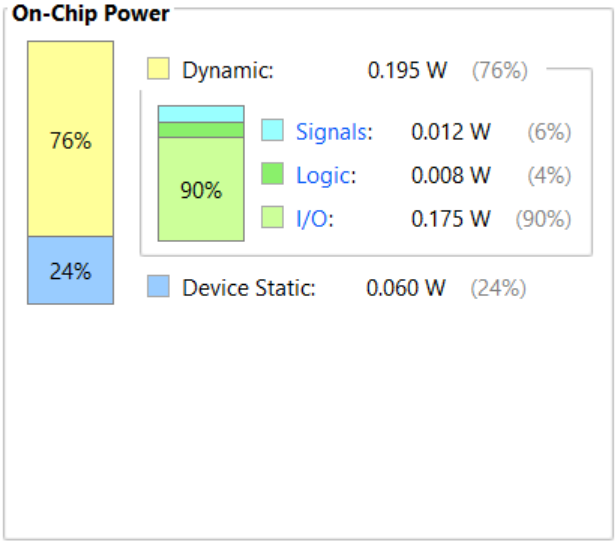
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT3 |     1|
|3     |FDCE |     1|
|4     |IBUF |     4|
|5     |OBUF |     1|
+------+-----+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:33 ; elapsed = 00:00:40 . Memory (MB): peak = 1033.520 ; gain = 18.836
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.255 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.6°C**
Thermal Margin:	98.4°C (15.7 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



14 FREQUENCY DIVIDER BY ODD NUMBERS

Verilog code:-

module odd_frequency_divider (

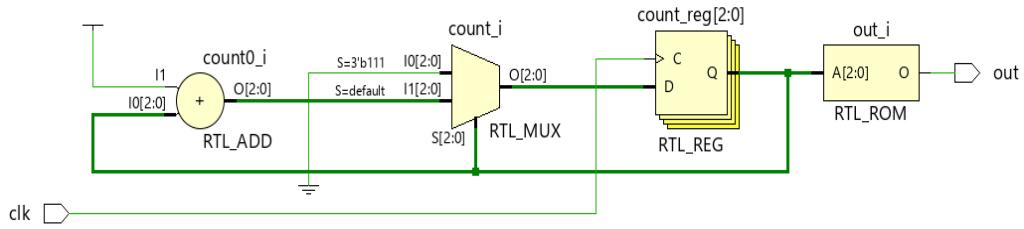
```
  input wire clk,
  output wire out
);

reg [2:0] count;

always @(posedge clk) begin

  if (count == 3'b111) begin
    count <= 3'b000;
  end
  else begin
    count <= count + 1;
  end
end

assign out = (count == 3'b100) ? 1'b1 : 1'b0;

endmodule
```

Testbench:-

```
module test_odd_frequency_divider;

reg clk;
wire out;

odd_frequency_divider UUT (
  .clk(clk),
  .out(out)
);
always begin
  #5 clk = ~clk;
end

initial begin
  clk = 0;
  #10;

  $display("Time=%0t, Clock=%b, Output=%b", $time, clk, out);
  #10;
```

```
 $finish;
end

endmodule
```

RTlsymatic:-



Synthasis report:-

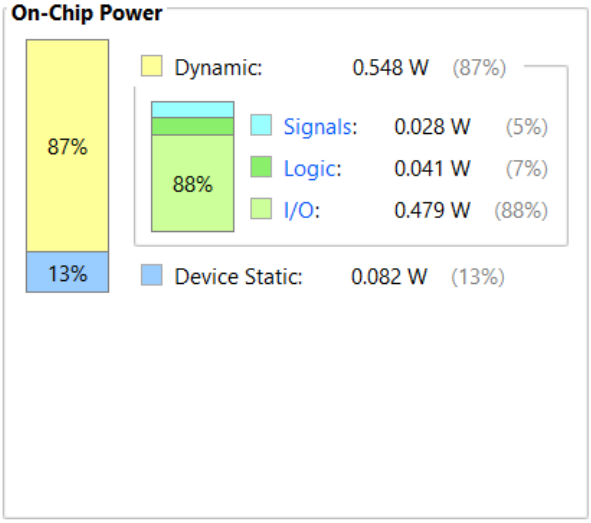
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT1 |     1|
|3     |LUT2 |     1|
|4     |LUT3 |     2|
|5     |FDRE |     3|
|6     |IBUF |     1|
|7     |OBUF |     1|
+------+-----+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:33 ; elapsed = 00:00:38 . Memory (MB): peak = 1042.262 ; gain = 24.605
---------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.631 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.2°C**
Thermal Margin:	58.8°C (31.0 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



15 GREATEST COMMON DIVISOR USING BEHAVIOURAL MODELLING

Verilog code:-

```
module gcd_calculator (
  input wire [31:0] a,
  input wire [31:0] b,
  output wire [31:0] gcd
);

// Helper function to compute the GCD
function [31:0] compute_gcd;
  input [31:0] x, y;
  begin
    if (y == 0) begin
      compute_gcd = x;
    end else begin
      compute_gcd = compute_gcd(y, x % y);
    end
  end
endfunction
```

Test bench:-

```
module test_gcd_calculator;

reg [31:0] a, b;
wire [31:0] gcd;


gcd_calculator UUT (
  .a(a),
  .b(b),
  .gcd(gcd)
);

initial begin

  a = 48;
  b = 18;
  #10;


  $display("GCD(%d, %d) = %d", a, b, gcd);
```

```
  $finish;
end

endmodule
assign gcd = compute_gcd(a, b);

endmodule
```

16 GREATEST COMMON DIVISOR VIA FSM

Verilog code:-

```
module gcd_calculator (
  input wire clk,
  input wire rst,
  input wire [31:0] a,
  input wire [31:0] b,
  output wire [31:0] gcd,
  output wire done
);


parameter IDLE = 2'b00;
parameter COMPARE = 2'b01;
parameter SUBTRACT = 2'b10;

reg [1:0] state, next_state;

always @(posedge clk or posedge rst) begin
  if (rst) begin
    state <= IDLE;
  end else begin
    state <= next_state;
  end
end

always @(*) begin
  case(state)
    IDLE: next_state = COMPARE;
    COMPARE: next_state = (a > b) ? SUBTRACT : COMPARE;
    SUBTRACT: next_state = (b > a) ? COMPARE : SUBTRACT;
    default: next_state = IDLE;
  endcase
end
```

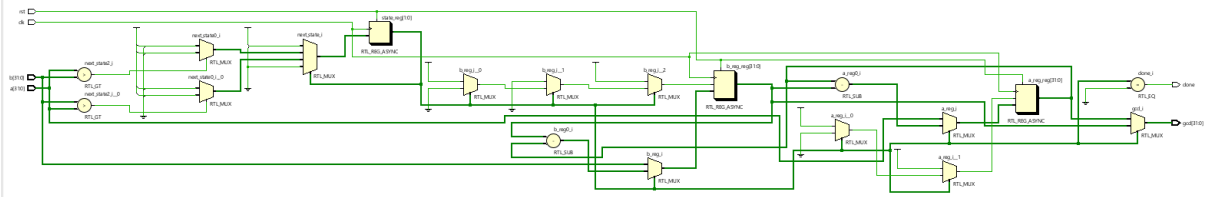
```
reg [31:0] a_reg, b_reg;

always @(posedge clk or posedge rst) begin
  if (rst) begin
    a_reg <= 32'b0;
    b_reg <= 32'b0;
  end else if (state == IDLE) begin
    a_reg <= a;
    b_reg <= b;
  end else if (state == SUBTRACT) begin
    a_reg <= a_reg - b_reg;
  end else if (state == COMPARE) begin
    b_reg <= b_reg - a_reg;
  end
end

assign done = (state == IDLE);
assign gcd = (state == IDLE) ? a_reg : b_reg;

endmodule
```

Test bench:-

```
module test_gcd_calculator;

reg clk;
reg rst;
reg [31:0] a, b;
wire [31:0] gcd;
wire done;


gcd_calculator UUT (
  .clk(clk),
  .rst(rst),
  .a(a),
  .b(b),
  .gcd(gcd),
  .done(done)
);

initial begin
  clk = 0;
```

```
  rst = 0;
  a = 48;
  b = 18;
  #5 rst = 1;
  #5 rst = 0;
  #10;


  $display("GCD(%d, %d) = %d", a, b, gcd);



  $finish;
end


always begin
  #2 clk = ~clk;
end

endmodule
```

Rtl symatic:-



Synthesis report:-

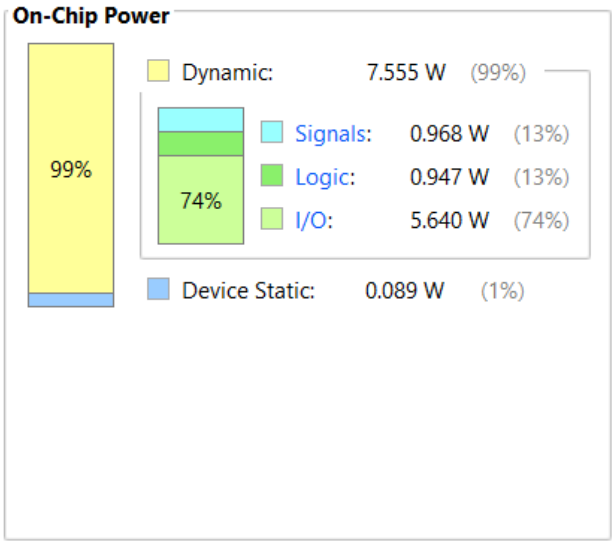
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     1|
|2     |CARRY4 |    24|
|3     |LUT2   |    66|
|4     |LUT3   |    96|
|5     |LUT4   |    65|
|6     |LUT5   |     1|
|7     |FDCE   |    66|
|8     |FDPE   |     1|
|9     |IBUF   |    66|
|10    |OBUF   |    33|
+------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:32 ; elapsed = 00:00:49 . Memory (MB): peak = 1032.867 ; gain = 13.016
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**7.644 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**72.3°C**
Thermal Margin:	52.7°C (8.4 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



17 SINGLE PORT RAM

Verilog code:-

```
module single_port_ram (
  input wire clk,
  input wire we,
  input wire [3:0] addr,
  input wire [7:0] data_in,
  output wire [7:0] data_out
);

reg [7:0] memory [15:0];

always @(posedge clk) begin
```

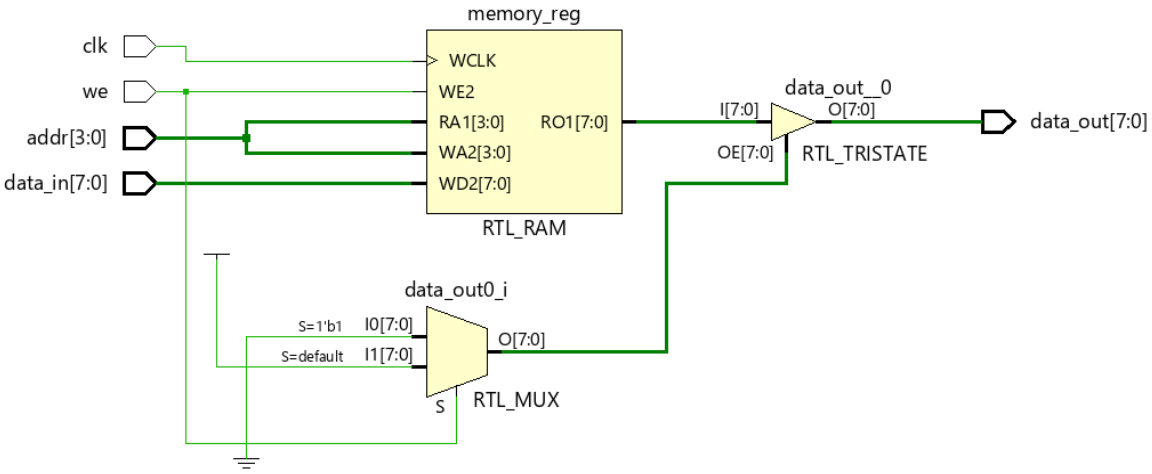
```
  if (we) begin
    memory[addr] <= data_in;
  end
end

assign data_out = we ? 8'bZZZZ_ZZZZ : memory[addr];

endmodule
```

Testbench:-

```
module test_single_port_ram;

reg clk;
reg we;
reg [3:0] addr;
reg [7:0] data_in;
wire [7:0] data_out;


single_port_ram UUT (
  .clk(clk),
  .we(we),
  .addr(addr),
  .data_in(data_in),
  .data_out(data_out)
);

initial begin
  clk = 0;
  we = 1;
  addr = 3'b101;
  data_in = 8'b1101_0011;


  #10 we = 0;


  $display("Read data at address %d: %h", addr, data_out);



  $finish;
end
```

```
always begin
  #5 clk = ~clk;
end

endmodule
```

RTlsynthesis:-



Synthesis report:-

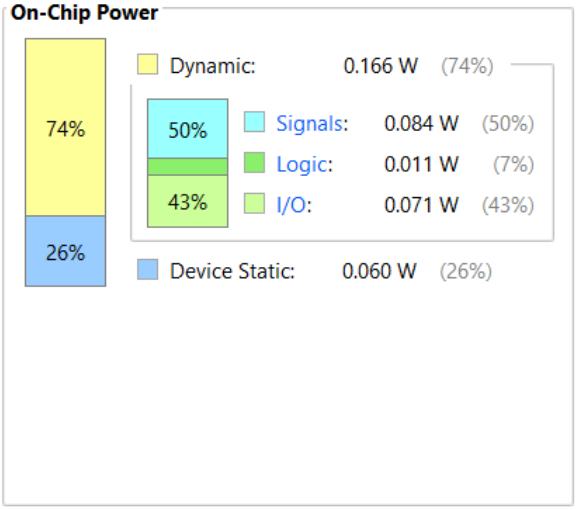
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+---------+------+
|      |Cell     |Count |
+------+---------+------+
|1     |BUFG     |     1|
|2     |RAM16X1S |     8|
|3     |IBUF     |    14|
|4     |OBUFT    |     8|
+------+---------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:18 ; elapsed = 00:00:25 . Memory (MB): peak = 1034.625 ; gain = 20.000
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.226 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.4°C**
Thermal Margin:	98.6°C (15.8 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



18 DUAL PORT RAM

Verilog code:-

```
module dual_port_ram (
 input wire clk,

 input wire we,
 input wire [3:0] addr_w,
 input wire [7:0] data_in,

 input wire re,
 input wire [3:0] addr_r,
 output wire [7:0] data_out
);

reg [7:0] memory [15:0];

always @(posedge clk) begin
 if (we) begin
  memory[addr_w] <= data_in;
 end
end

assign data_out = (re) ? memory[addr_r] : 8'bZZZZ_ZZZZ;

endmodule
```

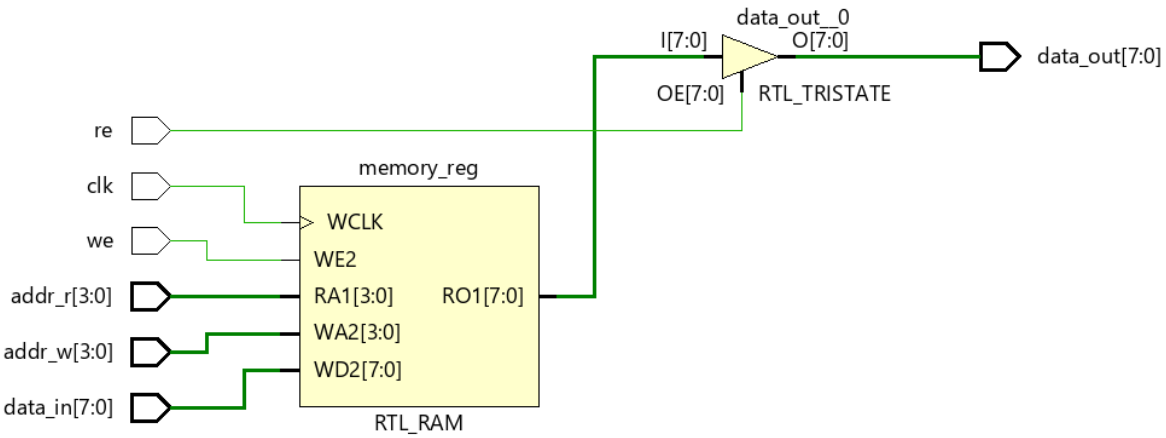
Test bench:-

```
module test_dual_port_ram;
```

```
reg clk;
reg we;
reg [3:0] addr_w;
reg [7:0] data_in;
reg re;
reg [3:0] addr_r;
wire [7:0] data_out;


dual_port_ram UUT (
  .clk(clk),
  .we(we),
  .addr_w(addr_w),
  .data_in(data_in),
  .re(re),
  .addr_r(addr_r),
  .data_out(data_out)
);

initial begin
  clk = 0;
  we = 1;
  addr_w = 3'b101;
  data_in = 8'b1101_0011;


  #10 we = 0;


  re = 1;
  addr_r = 3'b101;
  #10;
  $display("Read data at address %d: %h", addr_r, data_out);



  $finish;
end


always begin
  #5 clk = ~clk;
end
```

endmodule

RTlsymatic:-



Synthesis report:-

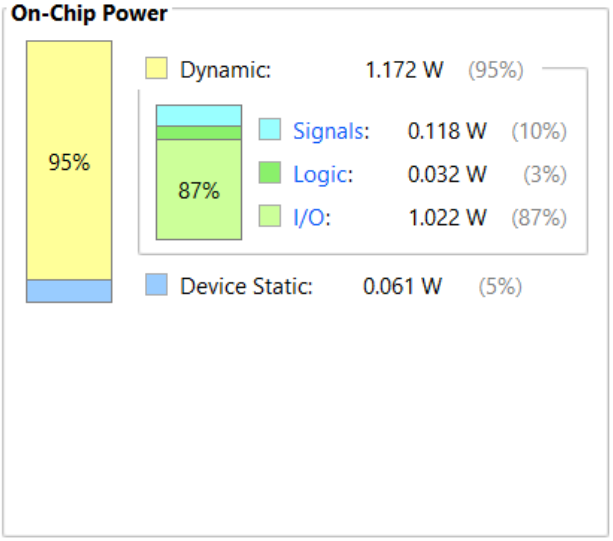
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     1|
|2     |LUT1   |     1|
|3     |RAM32M |     2|
|4     |IBUF   |    19|
|5     |OBUFT  |     8|
+------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:16 ; elapsed = 00:00:25 . Memory (MB): peak = 1026.965 ; gain = 7.105
---------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.233 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**32.6°C**
Thermal Margin:	92.4°C (14.8 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



19 CLOCK BUFFER

Verilog code:-

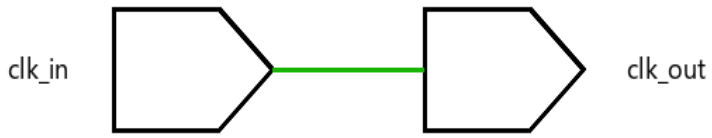
```
module clock_buffer (
  input wire clk_in,
  output wire clk_out
);

assign clk_out = clk_in;

endmodule
```

Test bench:-

```
module test_clock_buffer;

reg clk_in;
wire clk_out;

clock_buffer UUT (
  .clk_in(clk_in),
  .clk_out(clk_out)
);

initial begin
  clk_in = 0;


  forever begin
    #5 clk_in = ~clk_in;
```

```
  end

  $monitor("Time=%0t, Input Clock=%b, Output Clock=%b", $time, clk_in,
clk_out);

  #50;


  $finish;
end

endmodule
```

RTLsymatic:-



Synthesis report:-

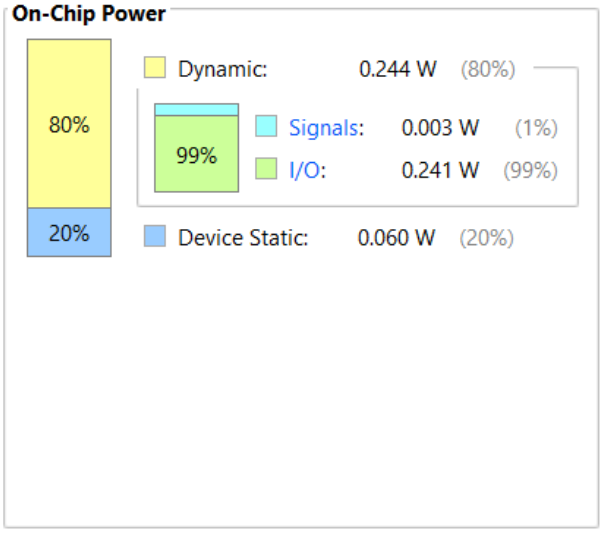
```
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |IBUF |     1|
|2     |OBUF |     1|
+------+-----+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:13 ; elapsed = 00:00:25 . Memory (MB): peak = 1018.867 ; gain = 0.000
---------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.304 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.9°C**
Thermal Margin:	98.1°C (15.7 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



20 SYNCHRONOUS FIFO

Verilog code:-

```
module fifo(
  input wire clk,
  input wire rst,
  input wire wr_en,
  input wire [7:0] data_in,
  output wire [7:0] data_out,
  output wire rd_empty,
  output wire wr_full
);

parameter DEPTH = 4;
parameter WIDTH = 8;

reg [WIDTH-1:0] memory [0:DEPTH-1];
reg [2:0] wr_ptr, rd_ptr;
reg [3:0] count;

assign data_out = (count == 0) ? 8'b0 : memory[rd_ptr];

assign rd_empty = (count == 0);
assign wr_full = (count == DEPTH);

always @(posedge clk or posedge rst) begin
  if (rst) begin
    wr_ptr <= 3'b0;
    rd_ptr <= 3'b0;
```

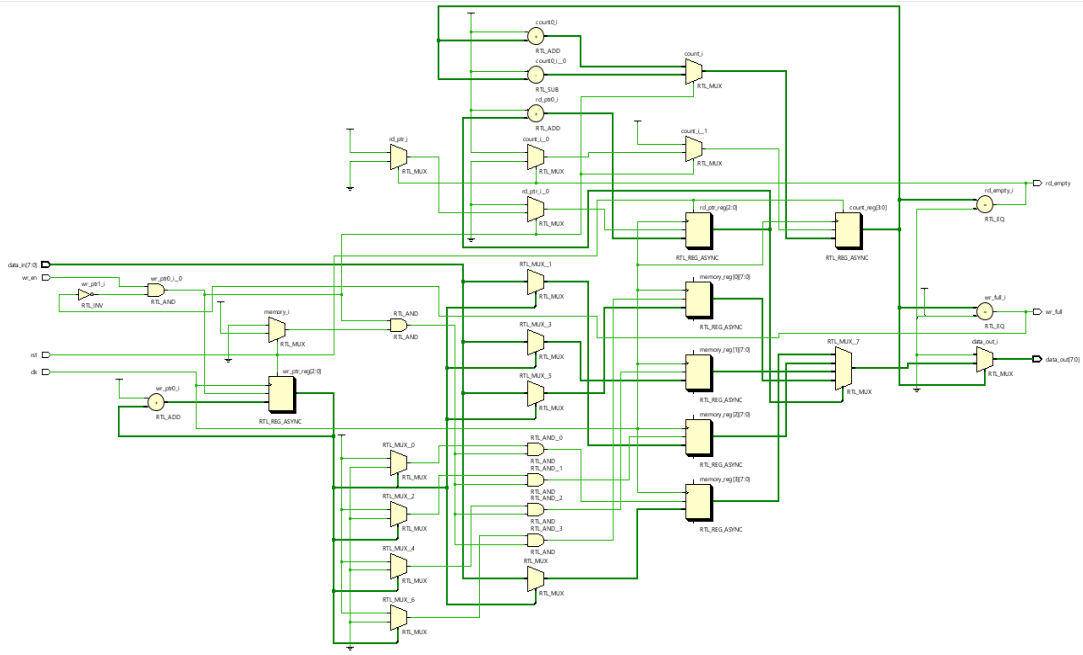
```
    count <= 0;
  end
  else if (wr_en && !wr_full) begin
    memory[wr_ptr] <= data_in;
    wr_ptr <= wr_ptr + 1;
    count <= count + 1;
  end
  else if (!rd_empty) begin
    rd_ptr <= rd_ptr + 1;
    count <= count - 1;
  end
end

endmodule
```

Testbench:-

```
module tb_fifo();

reg clk;
reg rst;
reg wr_en;
reg [7:0] data_in;
wire [7:0] data_out;
wire rd_empty;
wire wr_full;

fifo my_fifo (
  .clk(clk),
  .rst(rst),
  .wr_en(wr_en),
  .data_in(data_in),
  .data_out(data_out),
  .rd_empty(rd_empty),
  .wr_full(wr_full)
);

initial begin
  clk = 0;
  rst = 1;
  wr_en = 0;
  data_in = 8'h00;

  #10 rst = 0;
  #10 wr_en = 1;
```

```
  data_in = 8'hAA;
  #10 data_in = 8'h55;
  #10 wr_en = 0;
  #10 wr_en = 1;
  data_in = 8'h33;
  #10 data_in = 8'hFF;
  #10 wr_en = 0;
  #20 $finish;
end

always begin
  #5 clk = ~clk;
end

endmodule
```

RTlsymatic:-



Synthesis report:-

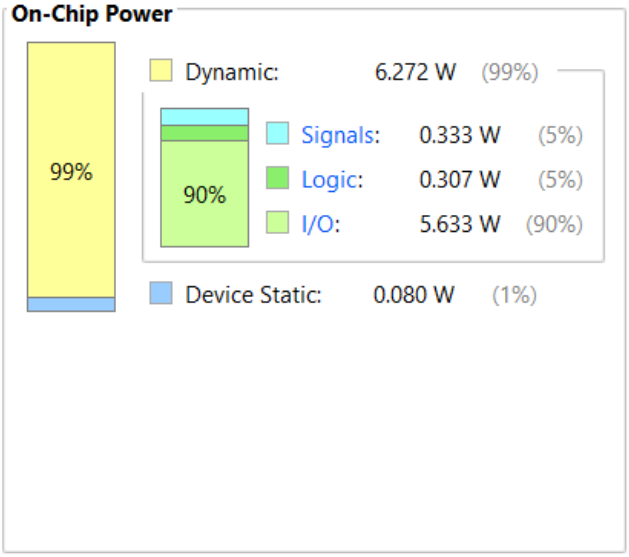
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT1 |     1|
|3     |LUT3 |     1|
|4     |LUT4 |     7|
|5     |LUT5 |    13|
|6     |LUT6 |    10|
|7     |FDCE |     8|
|8     |FDRE |    32|
|9     |IBUF |    11|
|10    |OBUF |    10|
+------+-----+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:21 ; elapsed = 00:00:25 . Memory (MB): peak = 1041.223 ; gain = 34.371
---------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**6.352 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**64.3°C**
Thermal Margin:	35.7°C (5.7 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



21 PRIORITY ENCODER

Verilog code:-

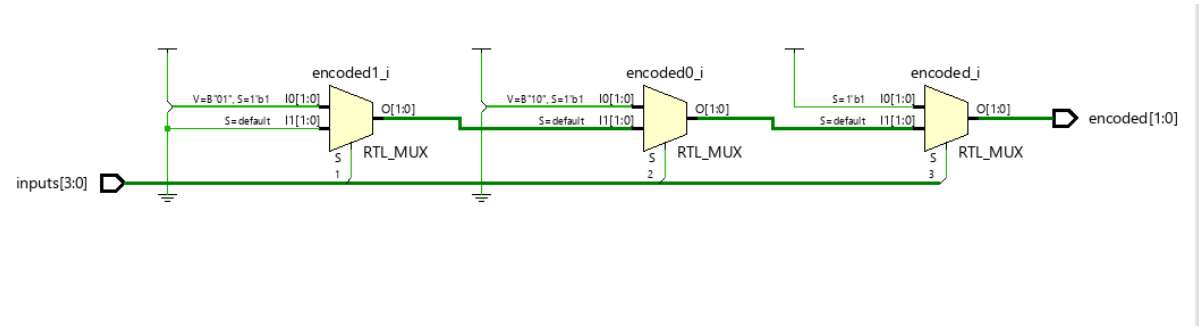
```
module priority_encoder_4_to_2(
  input wire [3:0] inputs,
  output wire [1:0] encoded
);

assign encoded = (inputs[3]) ? 2'b11 :
                 (inputs[2]) ? 2'b10 :
                 (inputs[1]) ? 2'b01 :
                               2'b00;
```

Endmodule

Test bench:-

```
module tb_priority_encoder_4_to_2();

reg [3:0] inputs;
wire [1:0] encoded;

priority_encoder_4_to_2 my_encoder (
  .inputs(inputs),
  .encoded(encoded)
);

initial begin
  $display("Testing 4-to-2 Priority Encoder");
  $display("Input (HEX)\tOutput (BIN)");
  $monitor("%h\t\t%b", inputs, encoded);


  for (inputs = 0; inputs < 16; inputs = inputs + 1) begin
    #5;
  end

  $finish;
end

endmodule
```

RTlsynthasis:-



Synthsis report:-

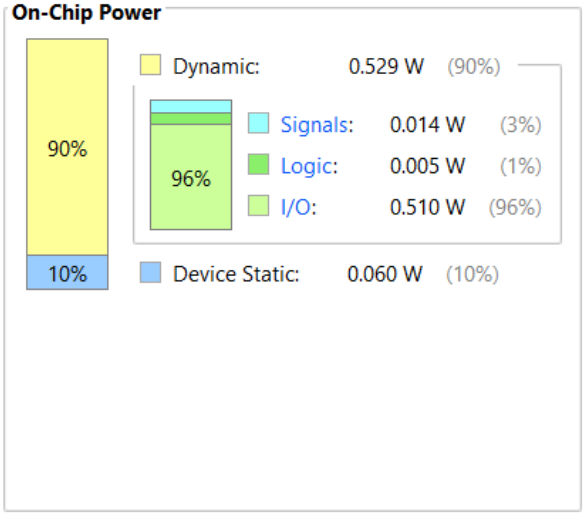
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT2 |     1|
|2     |LUT3 |     1|
|3     |IBUF |     3|
|4     |OBUF |     2|
+------+-----+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:20 ; elapsed = 00:00:26 . Memory (MB): peak = 1029.832 ; gain = 12.234
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.59 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**28.6°C**
Thermal Margin:	96.4°C (15.4 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



22 SEVEN SEGMENT DISPLAY USING ROM

Verilog code:-

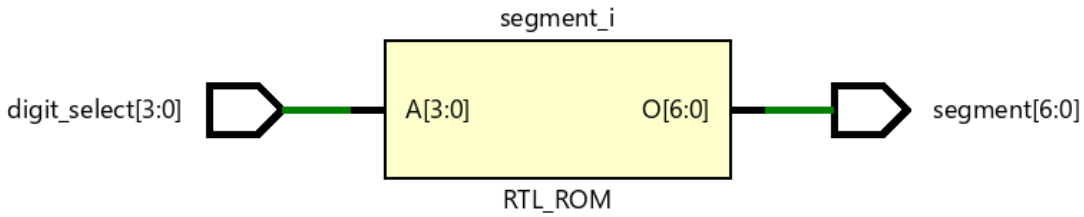
```
module seven_segment_display(
  input wire [3:0] digit_select,
  output wire [6:0] segment
);


reg [6:0] rom [0:9];


initial begin
  rom[0] = 7'b1000000;
  rom[1] = 7'b1111001;
  rom[2] = 7'b0100100;
```

```
  rom[3] = 7'b0110000;
  rom[4] = 7'b0011001;
  rom[5] = 7'b0010010;
  rom[6] = 7'b0000010;
  rom[7] = 7'b1111000;
  rom[8] = 7'b0000000;
  rom[9] = 7'b0010000;
end

assign segment = rom[digit_select];

endmodule
```

Testbench:-

```
module tb_seven_segment_display();

reg [3:0] digit_select;
wire [6:0] segment;

seven_segment_display my_display (
  .digit_select(digit_select),
  .segment(segment)
);

initial begin
  $display("Testing Seven-Segment Display");
  $display("Digit\tSegment Pattern (BIN)");


  for (digit_select = 0; digit_select < 10; digit_select = digit_select + 1) begin
    #5;
  end

  $finish;
end

endmodule
```

RTlsymatic:-



Synthesis report:-

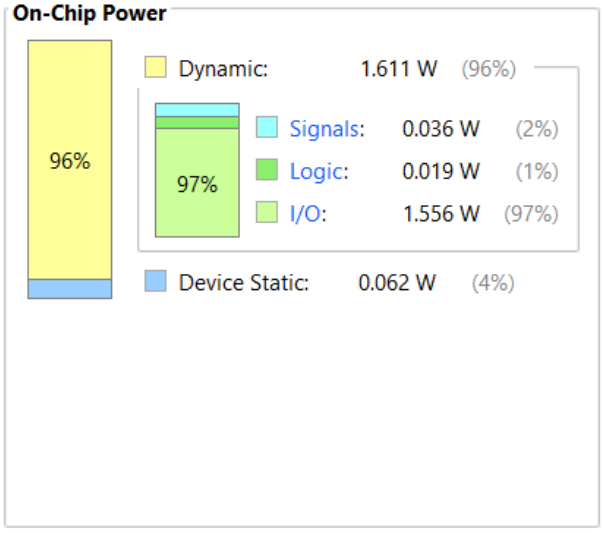
```
Start Writing Synthesis Report
-----------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT4 |     7|
|2     |IBUF |     4|
|3     |OBUF |     7|
+------+-----+------+
-----------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:32 ; elapsed = 00:00:44 . Memory (MB): peak = 1032.320 ; gain = 0.000
-----------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.673 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**35.3°C**
Thermal Margin:	89.7°C (14.3 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



23 SERIAL ADDER

Verilog code:-

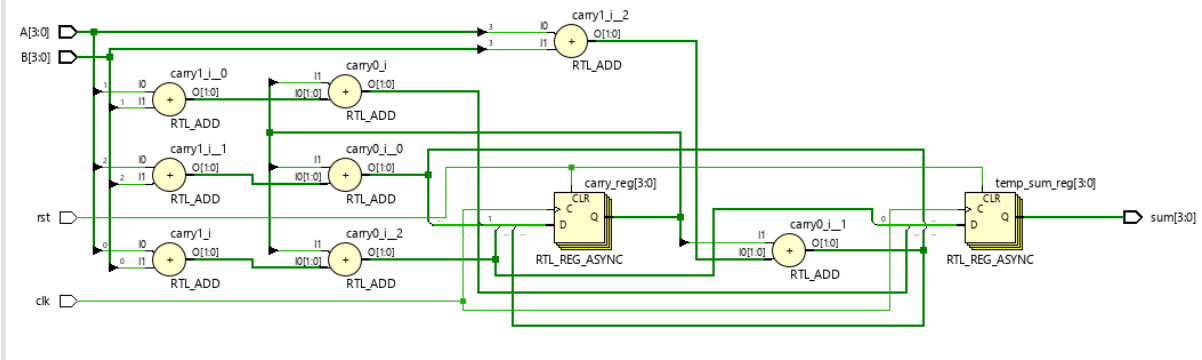
```
module serial_adder(
  input wire clk,
  input wire rst,
  input wire [3:0] A,
  input wire [3:0] B,
  output wire [3:0] sum
);

reg [3:0] carry;
reg [3:0] temp_sum;

always @(posedge clk or posedge rst) begin
  if (rst) begin
    carry <= 4'b0;
    temp_sum <= 4'b0;
  end
  else begin
    {carry[0], temp_sum[0]} <= A[0] + B[0] + carry[0];
    {carry[1], temp_sum[1]} <= A[1] + B[1] + carry[1];
    {carry[2], temp_sum[2]} <= A[2] + B[2] + carry[2];
    {carry[3], temp_sum[3]} <= A[3] + B[3] + carry[3];
  end
end

assign sum = temp_sum;

endmodule
```

Test bench:-

```
module tb_serial_adder();

reg clk;
reg rst;
reg [3:0] A;
reg [3:0] B;
wire [3:0] sum;

serial_adder my_adder (
  .clk(clk),
  .rst(rst),
  .A(A),
  .B(B),
  .sum(sum)
);
```

```
initial begin
  clk = 0;
  rst = 1;
  A = 4'b0;
  B = 4'b0;


  #5 A = 4'b0101;
  B = 4'b0011;
  rst = 0;
  #10 rst = 1;
  #5;


  A = 4'b0111;
  B = 4'b1001;
  rst = 0;
  #10 rst = 1;
  #5;



  $finish;
end

always begin
  #5 clk = ~clk;
end

endmodule
```

RTlsymatic:-



Synthesis report:-

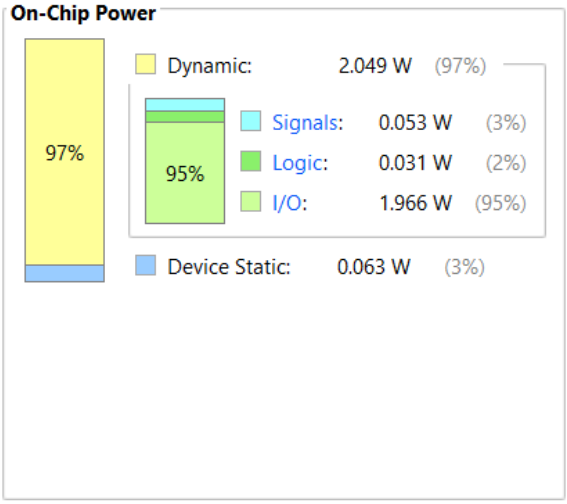
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT3 |     8|
|3     |FDCE |     8|
|4     |IBUF |    10|
|5     |OBUF |     4|
+------+-----+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:32 ; elapsed = 00:00:46 . Memory (MB): peak = 1026.422 ; gain = 10.727
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**2.112 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**38.1°C**
Thermal Margin:	86.9°C (13.9 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



24 FIXED PRIORITY ARBITER

Verilog code:-

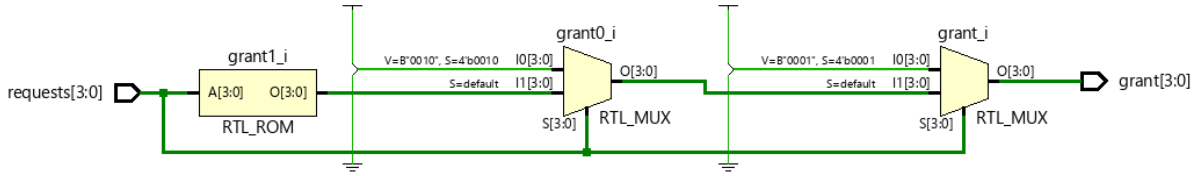
```
module fixed_priority_arbiter(
 input wire [3:0] requests,
 output wire [3:0] grant
);

assign grant = (requests == 4'b0001) ? 4'b0001 :
           (requests == 4'b0010) ? 4'b0010 :
           (requests == 4'b0100) ? 4'b0100 :
                       4'b1000;

Endmodule
```

Test bench:-

```
module tb_fixed_priority_arbiter();
```

```
reg [3:0] requests;
wire [3:0] grant;

fixed_priority_arbiter my_arbiter (
  .requests(requests),
  .grant(grant)
);

initial begin
  $display("Testing Fixed-Priority Arbiter");
  $display("Requests (BIN)\tGrant (BIN)");
  $monitor("%b\t\t\t%b", requests, grant);


  requests = 4'b0001;
  #10 requests = 4'b0000;


  requests = 4'b0010;
  #10 requests = 4'b0000;


  requests = 4'b0100;
  #10 requests = 4'b0000;


  requests = 4'b1000;
  #10 requests = 4'b0000;


  requests = 4'b0011;
  #10 requests = 4'b0000;


  requests = 4'b1100;
  #10 requests = 4'b0000;

  $finish;
end

endmodule
```

RTlsynthesis:-



Synthesis report:-

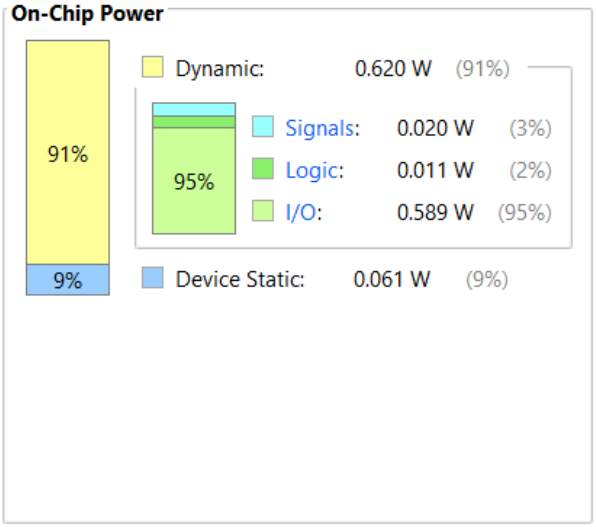
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT4 |     4|
|2     |IBUF |     4|
|3     |OBUF |     4|
+------+-----+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:32 ; elapsed = 00:00:50 . Memory (MB): peak = 1032.109 ; gain = 16.793
---------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.68 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**29.2°C**
Thermal Margin:	95.8°C (15.3 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



25 ROUND ROBIN ARBITER

Verilog code:-

```
module round_robin_arbiter(
  input wire clk,
  input wire rst,
  input wire [3:0] requests,
  output wire [3:0] grant
);

reg [1:0] round_robin_pointer;

always @(posedge clk or posedge rst) begin
  if (rst) begin
    round_robin_pointer <= 2'b00;
  end
  else begin
    if (requests == 4'b0000) begin
      round_robin_pointer <= 2'b00; // No requests, reset pointer
    end
    else begin
      // Round-robin logic
      round_robin_pointer <= round_robin_pointer + 1;
      if (round_robin_pointer == 2'b11) begin
        round_robin_pointer <= 2'b00; // Wrap around to the beginning
      end
    end
  end
end

assign grant = (round_robin_pointer == 2'b00) ? requests :
           (round_robin_pointer == 2'b01) ? requests >> 1 :
           (round_robin_pointer == 2'b10) ? requests >> 2 :
                                    requests >> 3;

endmodule
```

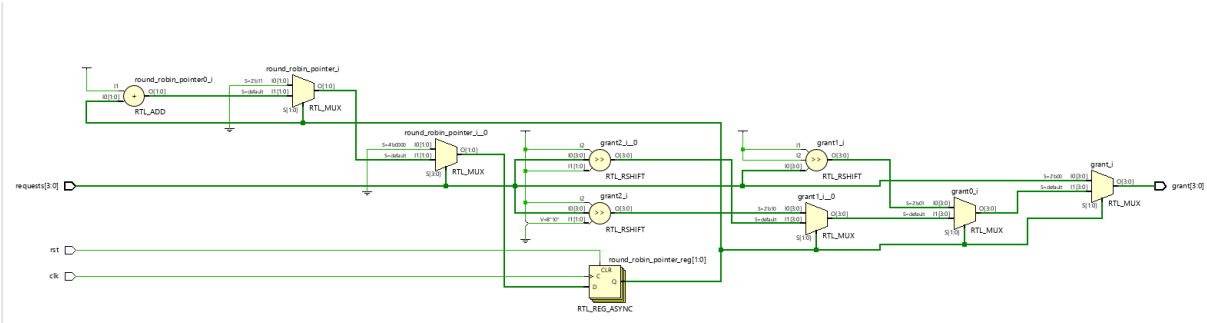
Test bench:-

```
module tb_round_robin_arbiter();

reg clk;
reg rst;
reg [3:0] requests;
wire [3:0] grant;
```

```
round_robin_arbiter my_arbiter (
  .clk(clk),
  .rst(rst),
  .requests(requests),
  .grant(grant)
);

initial begin
  $display("Testing Round-Robin Arbiter");
  $display("Requests (BIN)\tGrant (BIN)");
  $monitor("%b\t\t\t%b", requests, grant);


  rst = 1;
  requests = 4'b0001;
  #5 rst = 0;
  #5;


  rst = 1;
  requests = 4'b0010;
  #5 rst = 0;
  #5;


  rst = 1;
  requests = 4'b0100;
  #5 rst = 0;
  #5;


  rst = 1;
  requests = 4'b1000;
  #5 rst = 0;
  #5;


  rst = 1;
  requests = 4'b1111;
  #5 rst = 0;
  #5;

  $finish;
end
```

```
always begin
  #5 clk = ~clk;
end

endmodule
```

RTlsymatic:-



Synthasis report:-

```
Start Writing Synthesis Report
-------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT3 |     1|
|3     |LUT4 |     1|
|4     |LUT5 |     2|
|5     |LUT6 |     2|
|6     |FDCE |     2|
|7     |IBUF |     6|
|8     |OBUF |     4|
+------+-----+------+
-------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:32 ; elapsed = 00:01:00 . Memory (MB): peak = 1032.254 ; gain = 14.828
-------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**3.327 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**45.6°C**
Thermal Margin:	79.4°C (12.7 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity