

CSE 7381: Computer Architecture

Fall 2018, Southern Methodist University,

Team: E

Topic: Floating point addition & subtraction

To run the code

1. Copy the 4 files in genuse server.
2. log in to genuse server in terminal
3. Navigate to that directory using 'cd' command
4. Run this command : `verilog +gui floating_point_adder.v double_to_float.v float_to_double.v test_bench.v &`
5. Your output should be something like this

```
genuse50.engr.smu.edu - PuTTY

555 River Oaks Parkway
San Jose, California 95134

For technical assistance please contact the Cadence Response Center at
1-877-CDS-4911 or send email to support@cadence.com

For more information on Cadence's Verilog-XL product line send email to
talkv@cadence.com

Compiling source file "floating_point_adder.v"
Compiling source file "double_to_float.v"
Compiling source file "float_to_double.v"
Compiling source file "test_bench.v"
Highest level modules:
test_ALU_CTL

simvision(64): 15.20-s036: (c) Copyright 1995-2017 Cadence Design Systems, Inc.
Application initialization failed: no display name and no $DISPLAY environment variable
SimVision process terminated before a connection could be established.
SimVision process terminated before a connection was established

OUTPUTS=====>>

A= 5.500000,      B= 7.500000,      result= 13.000000
A= 13.300000,     B= 9.110000,      result= 22.410000
```

