

CSE 7381: Computer Architecture

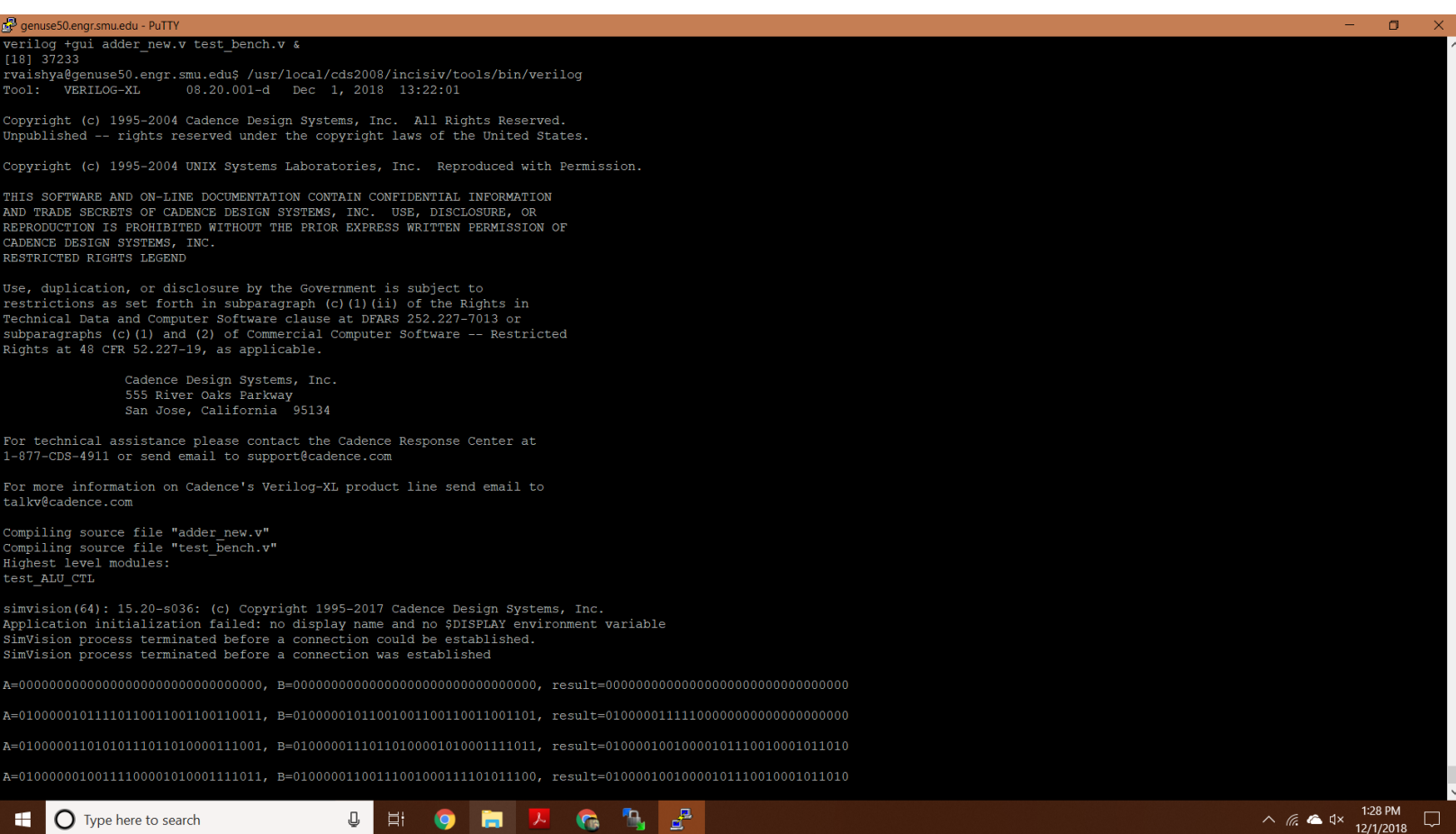
Fall 2018, Southern Methodist University,

Team: E

Topic: Floating point addition & subtraction

To run the code

1. Copy the 2 files in genuse server.
2. log in to genuse server in terminal
3. Navigate to that directory using 'cd' command
4. Run this command : **verilog +gui floating_point_adder.v test_bench.v &**
5. Your output should be something like this



```
genuse50.engr.smu.edu - PuTTY
verilog +gui adder_new.v test_bench.v &
[18] 37233
rvaishya@genuse50.engr.smu.edu$ /usr/local/cds2008/incisiv/tools/bin/verilog
Tool: VERILOG-XL      08.20.001-d   Dec  1, 2018  13:22:01

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Compiling source file "adder_new.v"
Compiling source file "test_bench.v"
Highest level modules:
test_ALU_CTL

simvision(64): 15.20-s036: (c) Copyright 1995-2017 Cadence Design Systems, Inc.
Application initialization failed: no display name and no $DISPLAY environment variable
SimVision process terminated before a connection could be established.
SimVision process terminated before a connection was established

A=00000000000000000000000000000000, B=00000000000000000000000000000000, result=00000000000000000000000000000000
A=01000001011110110011001100110011, B=01000001011001001100110011001101, result=01000001111100000000000000000000
A=01000001101010111011010000111001, B=01000001110110100001010001111011, result=01000010010000101110010001011010
A=0100000100111100001010001111011, B=01000001100111001000111101011100, result=01000010010000101110010001011010
```

