

# Label Switch Router (LSR) for NetFPGA

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Developed by Algo-Logic Systems for Google

http://Algo-Logic.com

Multiprotocol Label Switching (MPLS) is a mechanism that allows networks to carry data from one network node to the next with the help of short labels. MPLS enables creation of virtual links between distant nodes and can readily forward packets between data centers by encapsulating packets of multiple network protocols.

The MPLS Label Switch Router is a hardware-accelerated LSR implemented built by Algo-Logic Systems for Google that adds MPLS label switching functionality over and beyond the default NetFPGA reference switch.

The Structure of an MPLS packet with four MPLS tags is shown below.

ENet	MPLS Tag 1 MPLS Tag 2	•	MPLS Tag 4	IPv4 or V6 Header	Packet Payload
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MPLS tags can be seen immediately after ether type in Ethernet Header. Each MPLS Tag consists of 32 bits in the following format.

Label (20 bit)	EXP (3)	S (1)	TTL (8)

"EXP" is the experimental bits and we are not using it.

"S" indicates the end of Tag. If S is "1" it indicates that corresponding Tag is the last one in the MPLS Tag stack. 8 bits in the LSB side is allotted for TTL. 20 bits in the MSB side is the MPLS label and is used for Label switching operations. The MPLS operations that we have implemented are

- Swap
- Push
- Swap+Push
- Pop
- Pop+Swap

The operations to be performed in the input MPLS packets are decided by the 72 bit MPLS words which are stored in the SRAM of 1G NetFPGA card. The address of the 72 bit MPLS word is extracted from the 20 bit label in the first MPLS Tag. So whenever a packet enters in the NetFPGA hardware pipeline we extract the 20 bit label from the first MPLS Tag and do a lookup operation for obtaining the corresponding 72 bit MPLS word from SRAM. The format of the 72 MPLS word stored in SRAM is shown below.

Cmd [4]	LD [4]	Dest Port [6]	Dest MAC [8]	Next Label [20]	Push Label –or- Distribution Offset [20]	2 Bits (Not Used)	Parity Chk [8]
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Each field of the 72 bit MPLS word is given below

Cmd - MPLS Commands: 4 bits, which are represented as

No Op=0, Swap=1, Push=2, Swap+Push=3, Pop=4 and Pop+Swap=5

LD - Load Distribution Count: 4 bits

The number of load distribution entries starting from the Load distribution offset. Default value is 0

#### **Dest Port**

Address of the output Physical port (nf2c0, nf2c1 ... )

#### **Dest MAC**

Index to 256-entry table of MAC addresses stored in on-chip BRAM

#### **Next Label**

20 bit MPLS label used to swap with the 20 bit label of the first MPLS Tag in the incoming packet

#### **Push Label -or- Distribution offset**

For commands which do push uses these 20 bits as the pushing MPLS label. If LD > 0 these 20 bits will be the starting address of the load distribution entries.

#### Parity/Checksum

N-bit check of bits

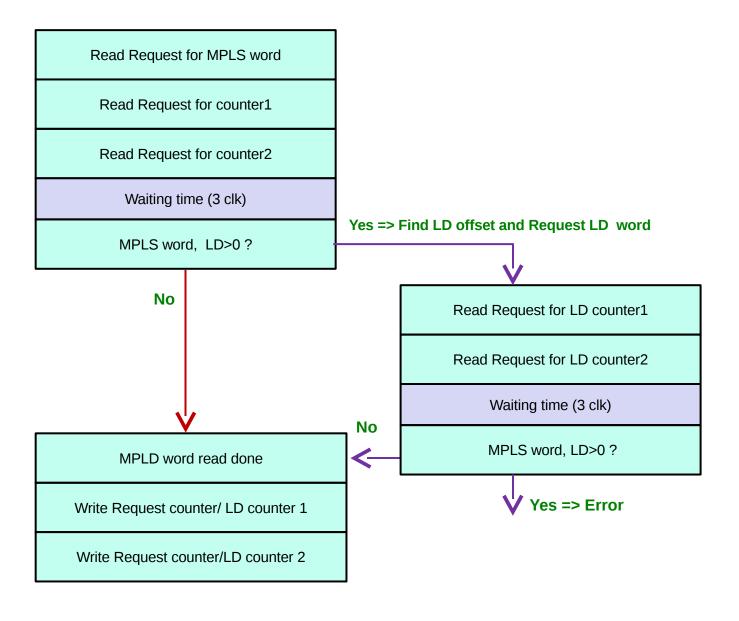
## Label spaces and partitions in SRAM:

SRAM in a 1G NetFPGA board can store 256k words with a width of 72bits. The total label space is divided in to four (LS1, LS2, LS3 and LS4) and each space is assigned to each input port. There is a separate space for the load distribution entries which is named as LD space. For each entry in the LS space and LD space there will two counters. First counter gives the total number of packets which uses that particular entry and the second counter indicates the total byte count of those packets. Each of these counters take 1/3 of the total SRAM space. The whole SRAM space allotted for these spaces are shown below.

LS 1 : MPLS Table
LS 2 : MPLS Table
LS 3 : MPLS Table
LS 4 : MPLS Table
LD : MPLS Table
Packet Counter entries
Packet Byte Counter entries

## **SRAM Lookup:**

If the Ethernet parser find a MPLS Unicast packet the first 20 bits from the first MPLS Tag is extracted and added with a constant value (software offset) to find out the lookup address. After the SRAM lookup the Ethernet parser module will check the 4 bit LD value in the 72 bit MPLS word. If the LD value is zero the received MPLS word is latched and the corresponding Packet counter and Packet byte counter is incremented. If LD value is not equal to zero then the 20 bit LD offset value is latched. Consider "n" is the LD value. This indicates that there will



be n valid LD entries starting from the address 'LD offset' and from these n entries one is to be selected for the later MPLS operations. A hash value is generated by making use of the following parameters.

- Source IP address (32 bit) of the packet.
- Destination IP address (32 bit) of the packet.
- TCP source port (16 bit) if the packet is a TCP packet (or UDP source port if the packet is a UDP packet)
- TCP destination port (16 bit) if the packet is a TCP packet (or UDP destination port if the packet is a UDP packet)

Let k is the hash value, then (k modulo n) will give a number p whose value will be in between 0 and n-1.

The address of the LD entry selected = (LD offset + p)

A second SRAM look up operation is performed for this selected address. After latching the MPLS word corresponding packet counter and packet byte counter are incremented.

# **BRAM Lookup:**

Dest Mac field (8 bits) of latched MPLS word is used for BRAM lookup to get the destination Mac address of the outgoing packet. A maximum of 256 Mac addresses can be stored in the BRAM.

## Packet flow through NetFPGA hardware pipeline:

Mac receiver unit receives packet and direct it to output look-up module through the input arbiter.

In Output look-up, module header of the packet is parsed by the help of header parser module.

It latches all the header information in a status FIFO. The packets are stored in a FIFO in the look-up module.

The Actions in the output look-up module are taking place in the following

order.

If the packet is MPLS multicast it is forwarded to CPU.

If the Multicast bit is not set and the Destination Mac Address is not matching, then the packet is dropped and the corresponding counter (Not for us counter) is incremented.

If the packet is MPLS unicast and SRAM lookup address derived from 20 bit MPLS Tag is out of the expected label space, then the packet is dropped and the corresponding counter (LS error counter) is incremented.

If the packet is not MPLS unicast it is forwarded to CPU.

If the packet is MPLS unicast, it waits for the MPLS look-up action to complete.

After getting the MPLS word from the SRAM Corresponding packet counter and packer byte counter content in the SRAM is incremented.

Index for the Destination Mac address is latched from the 72 bit MPLS word and BRAM lookup is performed.

If there a parity error in the look-up MPLS word it is dropped and corresponding counter is incremented

If there is no error, then the MPLS unicast packet with the modified Destination mac and output port are passed to the MPLS processing unit along with the MPLS look-up word from SRAM.

MPLS processing unit check the TTL and if it is expired forward it to CPU and corresponding counter is incremented.

Else it Modify the Packet header according to the "cmd" bit in the MPLS word and it is passed to the output queue module.

Output queue module check the output port address and forward the packet to corresponding DRAM queue and then it is forwarded to corresponding Mac transmitting unit.

# **Register Interface:**

MPLS word entry in SRAM and output Mac address entry in BRAM, are populated using register interface. Address of all registers, SRAM base and Block ram base are defined in

```
~/netfpga/projects/mpls switch/lib/C/reg defines mpls switch.h
```

NetFPGA register interface support the read and write of 32 bit wide word. In order to write a single SRAM entry (72 bits) we make use of SRAM address locations between "0Xxxxxxxx0" and "0Xxxxxxxxf". 32 bits of SRAM entry in the LSB side is buffered if we use the address location 0XxxxxxxxC, Next 32 bits (middle) is buffered for the address location 0Xxxxxxxx8 and the next 8 bits (MSB side) are buffered for the address location 0Xxxxxxxx4. These buffered 72 bits is written to the SRAM when we write a trigger value of "0xfffffff" to the address location "0Xxxxxxxx0". The following example illustrate the procedure to write a 72 bit SRAM entry "0X12345678ABCDFFFF98" to the SRAM locations from address 0X1000000 to 0X100000f.

```
writeReg(&nf2, 0x100000C, 0xCDFFFF98);
writeReg(&nf2, 0x1000008, 0x345678AB);
writeReg(&nf2, 0x1000004, 0x00000012);
writeReg(&nf2, 0x1000000, 0xffffffff);
```

Writing a Mac address in BRAM also follow the same procedure. The following example illustrate how we write a Mac address "12345678ABCD" to the BRAM region spanned between "0x2002030" and "0x200203f".

```
writeReg(&nf2, 0x100000C, 0x5678ABCD);
writeReg(&nf2, 0x1000008, 0x00001234);
writeReg(&nf2, 0x1000000, 0xffffffff);
```

Other important registers needed for proper MPLS operations are added below.

```
#define SWITCH_OP_LUT_MACO_HI_REG 0x2000100
#define SWITCH_OP_LUT_MACO_LO_REG 0x2000104
#define SWITCH_OP_LUT_MAC1_HI_REG 0x2000108
#define SWITCH_OP_LUT_MAC1_LO_REG 0x200010c
#define SWITCH_OP_LUT_MAC2_HI_REG 0x2000110
```

```
#define SWITCH_OP_LUT_MAC2_LO_REG 0x2000114
#define SWITCH_OP_LUT_MAC3_HI_REG 0x2000118
#define SWITCH_OP_LUT_MAC3_LO_REG 0x200011c
```

Above registers are used for storing Mac Address of the NetFPGA Mac ports. This Mac address is used for matching with the destination Mac address of the incoming packets.

```
#define SWITCH OP LUT LS1 BASE REG
                                          0x2000120
#define SWITCH OP LUT LS1 BOUND REG
                                          0x2000124
#define SWITCH_OP_LUT_LS2_BASE_REG
                                          0x2000128
#define SWITCH OP LUT LS2 BOUND REG
                                          0x200012c
#define SWITCH_OP_LUT_LS3_BASE_REG
                                          0x2000130
#define SWITCH OP LUT LS3 BOUND REG
                                          0x2000134
#define SWITCH OP LUT LS4 BASE REG
                                          0x2000138
#define SWITCH_OP_LUT_LS4_BOUND_REG
                                          0x200013c
#define SWITCH OP LUT LD BASE REG
                                          0x2000140
#define SWITCH_OP_LUT_LD_BOUND_REG
                                          0x2000144
```

Above registers are used for storing Base addresses and Bound for four label spaces and one LD space.

```
#define SWITCH_OP_LUT_SOFT_OFFSET_REG 0x2000150
```

Used to load software offset. The content of this register is added with the 20 bit MPLS label of the first MPLS Tag in the incoming packet to find out the SRAM lookup address.

```
#define SWITCH_OP_LUT_NOT_FOR_US_REG 0x2000154
```

Content of this register gives the number packets dropped due to the mismatching destination Mac address

```
#define SWITCH_OP_LUT_PARITY_ERROR_REG 0x2000158
```

Content of this register gives the number of times parity error found while SRAM MPLS lookup.

```
#define SWITCH_OP_LUT_TTL_ERROR_REG 0x200015c
```

Content of this register gives TTL error count

```
#define SWITCH OP LUT LS ERROR REG 0x2000160
```

This counter is incremented if the index for the SRAM lookup is not matching with the assigned label space for the incoming packet.

```
#define SWITCH_OP_LUT_LD_ERROR_REG 0x2000164
Gives the LD error count.
```

#### Software:

Software programs to help populating SRAM and BRAM and other register entries are provided in ~/netfpga/projects/mpls switch/sw

SWap is the command for entering a swap entry with Id value zero in sram and it should be followed

- 1: Destination port number
- 2: SRAM entry number
- 3: BRAM Mac entry number and
- 4: Next mpls label

push is the command for entering a push entry with Id value zero in sram and it should be followed

- 1: Destination port number
- 2: SRAM entry number
- 3: BRAM Mac entry number and
- 4: push label

**POP** is the command for entering a pop entry with Id value zero in sram and it should be followed

- 1: Destination port number
- 2: SRAM entry number
- 3: BRAM Mac entry number

Spush is the command for entering a swap+push entry with Id value zero in sram and it should be followed by

- 1: Destination port number
- 2: SRAM entry number
- 3: BRAM Mac entry number
- 4: Next mpls label
- 5: push label

**pswap** is the command for entering a pop+swap entry with ld value zero in sram and it should be followed

1: SRAM entry number

d is the command for entering an entry with a nonzero ld value in sram and it should be followed by

- 1: ld value
- 2: SRAM entry number
- 3: Distribution offset

mac\_out is the command for entering a mac entry in bram and it should be followed by

- 1: mac address without colon or space in between
- 2: BRAM entry number

ISId\_init is the command for entering label space, Id space and pkt counter base and bound and it should be followed by

- 1: Label space 1 base address
- 2: Label space 1 bound (number of entries)
- 3: Label space 2 base address
- 4: Label space 2 bound (number of entries)
- 5: Label space 3 base address
- 6: Label space 3 bound (number of entries)
- 7: Label space 4 base address
- 8: Label space 4 bound (number of entries)
- 9: Ld space base address
- 10: Ld space bound (number of entries)

- 11: packet counter space base address
- 12: Packet byte counter space base address

mac0\_add, mac1\_add, mac2\_add, mac3\_add are the commands for entering mac addresses of corresponding mac ports and these should be followed by

1: mac address without colon or space in between

Isr\_init is the command for initializing label space registers, Id space registers, software offset register, Mac address registers and error count registers with default values.

Following are some underlying C functions which can be used to perform MPLS operations.

lsr\_fn is a function which can be used to enter a 72 bit SRAM entry.

int lsr\_fn(int dest\_port,int ld\_entry, int mac\_bram\_entry, int
next\_label, int next\_label2,int op, int entry\_num)

- dest\_port Destination port
- ld\_entry Load distribution entry
- int mac\_bram\_entry Index of BRAM to read the output Mac Address
- next\_label Label used for the swap operation (input any value if it is not used)
- next\_label2 load distribution offset or push value (input any value if it is not used)
- op MPLS cmd (value between 0 to 5)
- entry\_num Index of SRAM to write the MPLS word

mac\_out is the function to write a Mac address entry to the BRAM lookup Table.

int mac\_out(int mac\_oh, int mac\_ol, int entry\_num)

- mac\_oh value for 16 bits in the MSB side of the Mac address
- mac\_o1 value for 32 bits in the LSB side of the Mac address
- entry\_num - Index of BRAM to write the Mac address

lsr1\_init is the function to write Label space 1 starting index and bound (number of entries in SRAM) to corresponding registers.

int lsr1\_init(int base\_address, int bound)

- base\_address Starting Address of the Label space 1 in SRAM
- bound Number of entries for the Label space 1 in SRAM

Similarly 1sr1\_init, 1sr1\_init, 1sr1\_init can be used to enter base and bound values for other label spaces.

lsr\_ld\_init is the function to write LD space starting index and bound to corresponding registers.

int lsr\_ld\_init(int base\_addr, int bound)

- base\_addr Starting Address of the LD space in SRAM
- bound Number of entries for the LD space in SRAM

cnt\_base\_init is the function to write packet counter and packet
byte counter starting indexes to corresponding registers.

int cnt\_base\_init(int packet\_counter\_base\_addr, int byte\_counter\_base\_addr)

- packet\_counter\_base\_addr Starting Address of the packet counter in SRAM
- byte\_counter\_base\_addr Starting Address of the packet byte counter in SRAM

soft\_offset\_init is the function to write software offset value to corresponding register.

```
int soft_offset init(int soft_offset)
```

• soft\_offset - software offset value .

mac0\_init is the function to enter the Mac address of the Port 0
 of the NetFPGA board

```
int mac0 init(int mac0 hi, int mac0 lo)
```

- mac0\_hi value for 16 bits in the MSB side of the Mac address
- mac0 10 value for 32 bits in the LSB side of the Mac address

similarly mac1\_init, mac2\_init, mac3\_init can be used to enter Mac addresses for other three ports.

lsr\_init is the function which set up default values in different
registers

```
int lsr_init()
```

This function initializes the following parameters

- Label space and LD space base and bound values. Equally distributed entries for all the four label spaces (corresponds to each port) and LD space. default is to assign each port N=8888 h=34,952d entries of the total of 512k entries 3 table regions
- packet counter and Packet byte counter base address
- offset value added to input label value (-1,000,000 in 2's complement; as per Juniper default)
- MAC address of nf2c0: MSB,LSB = 00:90:69:B1:D0:7E
- Reset count of packets arriving with MAC != self
- Reset counter corresponds to Parity errors in SRAM lookups
- Reset counter corresponds to TTL expirations
- Reset counter corresponds to Label Space out-of-bound error
- Reset counter corresponds to Load Distribution error

User can also read and write any registers using regread and regwrite commands which can be find in ~/netfpga/lib/C/reg\_access. For example user can use regread 0x0600028 to read the number of packets transmitted through mac-0 port.

# Implementation and testing:

(1) Starting at the top-level of a NetFPGA base distribution

(typically: /home/user/netfpga), extract tarball file to
populate lib and project/mpls-switch sub-directories.
 eg:
 cd ~/netfpga
 tar xvf lsr-netFPGA.tar

- (2) Download the LSR bitfile to the netfpga nf download ./bitfiles/mpls switch.bit
- (3) Compile the mpls control and configuration software cd ./projects/mpls\_switch/sw ./make
- (4) Run the command-line program to initialize LSR switch ./Isr lsr\_init
  Will initialize tables with default values.
- (5) For testing,
- \* connect eth1 (NIC) to nf2c0 (Port 0 of NetFPGA) with short cat5e cable,
- \* connect eth2 (NIC) to nf2c1 (Port 1 of NetFPGA) with short cat5e cable,

- \* run wireshark on eth2 to monitor output packets
- \* and run command like:

cd /../pcap\_files
tcpreplay intf1=eth1 preswap.cap
to verify operation of lsr switch with sample packets

The cable connections between the Host machine and the NetFPGA board is shown below



(6) To add entries to SRAM to perform specific swap, pop, push, swap+push, and pop+swap operations, use the command syntax documented by running ./lsr

#### Results:

**W**ireshark capture of of the packet send to the NetFPGA port 0 and the output packet from NetFPGA port 1 is shown below.

### **Swap operation**

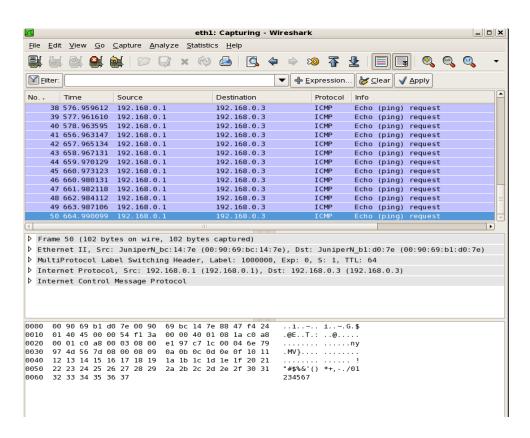
The following commands are used for setup

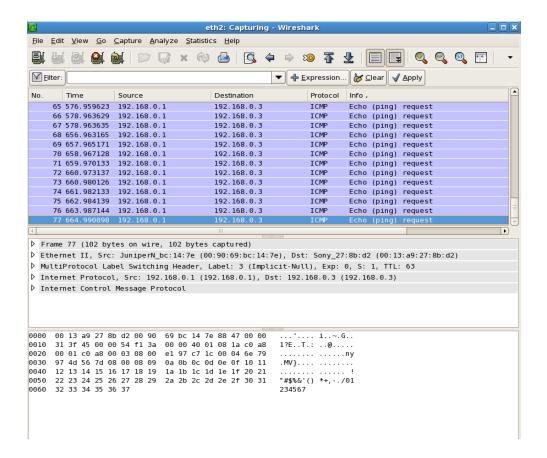
./lsr lsr\_init

./lsr swap 2033

./Isr mac out 13a9278bd2 3

tcpreplay intf1=eth1 preswap.cap





# **Push operation**

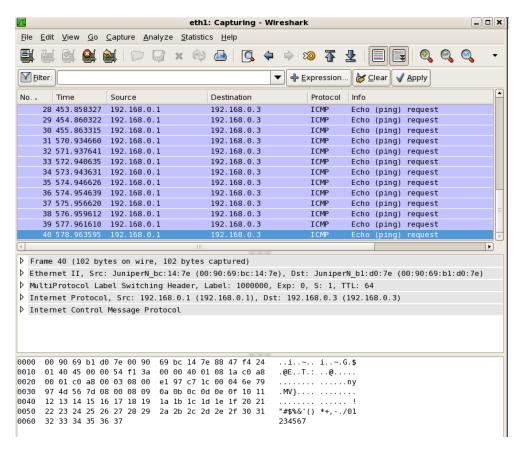
The following commands are used for setup

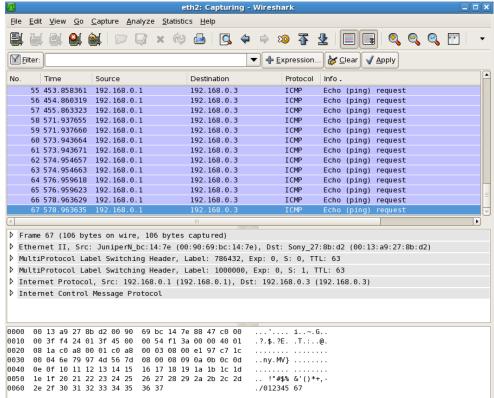
./Isr lsr\_init

./lsr push 2 0 3 786432

./lsr mac\_out 13a9278bd2 3

tcpreplay intf1=eth1 preswap.cap





### Pop operation

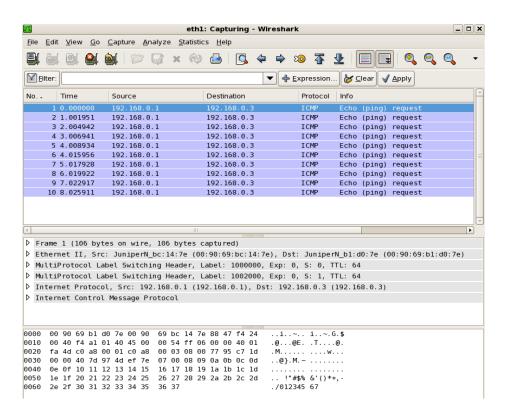
The following commands are used for setup

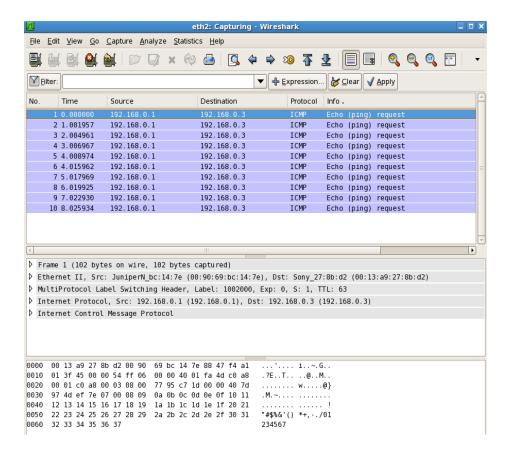
./lsr lsr\_init

./lsr pop 2 0 3

./lsr mac\_out 13a9278bd2 3

tcpreplay intf1=eth1 predoublepop.cap





## Swap+push operation

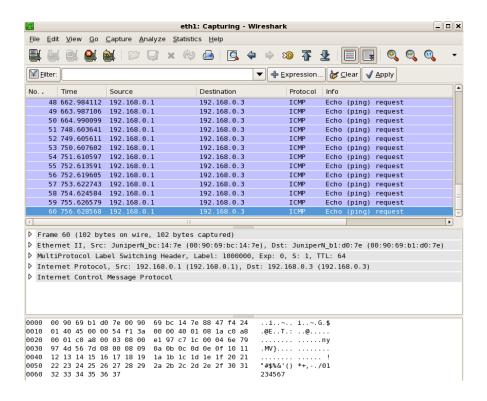
The following commands are used for setup

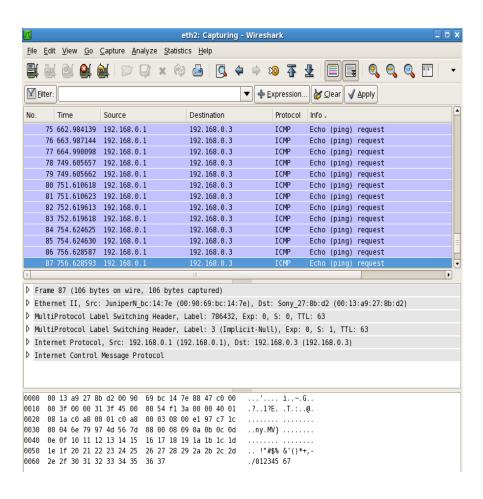
./lsr lsr\_init

./lsr spush 2 0 3 3 786432

./lsr mac out 13a9278bd2 3

tcpreplay intf1=eth1 preswap.cap





### Pop+swap operation

The following commands are used for setup

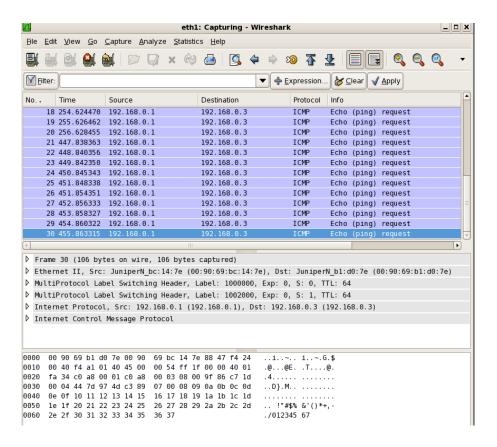
./lsr lsr\_init

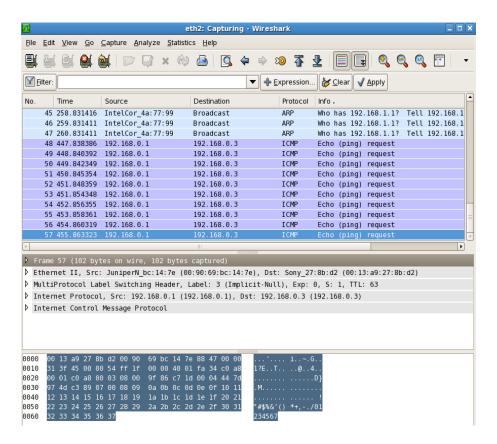
./Isr pswap 0

./lsr swap 2 2000 3 9

./lsr mac\_out 13a9278bd2 3

tcpreplay intf1=eth1 predoublepop.cap





# For Additional help and Assistance:

Contact: <a href="mailto:lsr">lsr</a> support@algo-logic.com</a>