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Neuromorphic NoC Accelerator Architecture for Spiking Neural Networks

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Abstract- A neuromorphic accelerator architecture that is optimised to run smaller scale Spiking Neural Networks (SNNs), using a network of nodes optimised for high speeds and low power consumption. This implementation aims at capturing and representing the inherent asynchronous behaviour of SNNs.

Aim- To optimise communication and memory management within the system on chip to bring out the best performance of the hardware.

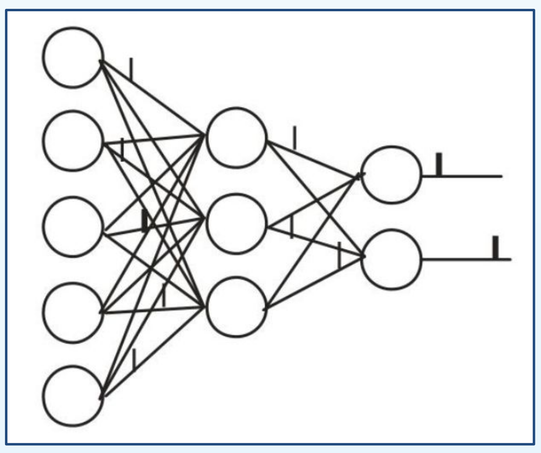


Figure 1: An SNN

An **SNN** is an event driven ANN that passes information only when a neuron spikes.

Motivation- Existing neuromorphic hardware are expensive yet excellent in realising the efficiency of SNNs. Smaller scale applications as seen in figure 2 use "the big ones" such as Loihi by Intel and TrueNorth chips to run on. This is not economical given that only less than 1/100th of the hardware will be used. We thus see the need for commercially available "smaller ones".

- Lane keeping robot using 34 neurons.

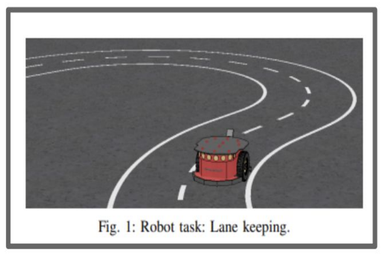
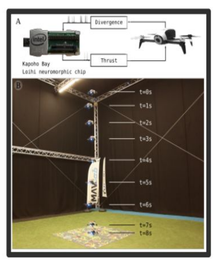
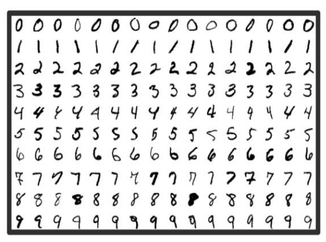


Fig. 1: Robot task: Lane keeping.

- Optic-flow-based landings of MAVs with 35 neurons.



- MNIST classification using 900- 1,578 neurons.



- Energy-Efficient Natural Language Processing with 896 neurons.

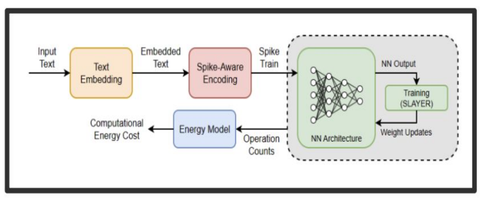


Figure 2: Small scale SNN based applications

Methodology- A modular design is employed to drive an SNN as shown in figure 3. The network interface allows communication between neurons. Each neuron has dedicated hardware units for operations. Memory is distributed such that each neuron has direct access to its parameters.

A controller running the RISC-V ISA is used to initialise the hardware to run any SNN. An FPGA synthesis will be done to collect performance measures for comparison with existing solutions.

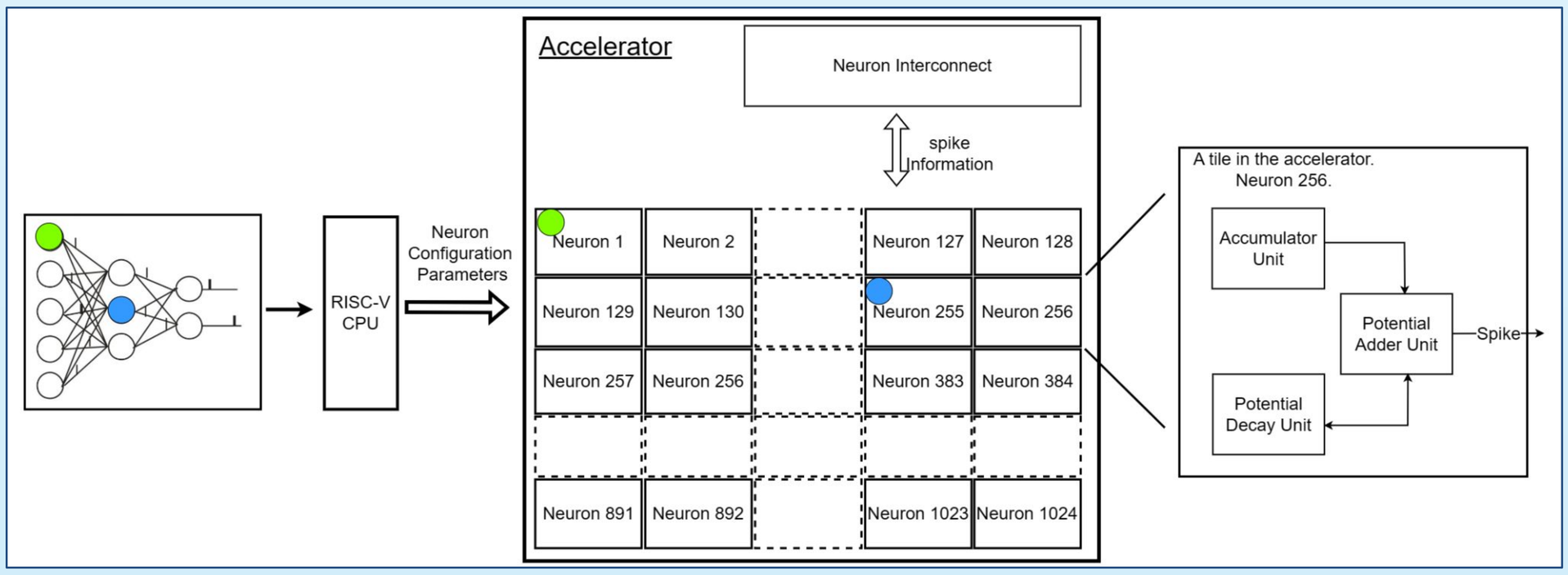


Figure 3: Design overview

Conclusion- This accelerator design optimises on power and cost associated with deploying neuromorphic hardware on embedded applications.

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