1. Is the 4-digit seven-segment display on the BASYS 3 board a common anode for common cathode? Please explain.

   Ans: common anode โดยอ้างอิงจาก Basys 3™ FPGA Board Reference Manual

8.1 Seven-Segment Display

The Basys 3 board contains one four-digit common anode seven-segment LED display. Each of the four digits is composed of seven segments arranged in a "figure 8" pattern, with an LED embedded in each segment. Segment LEDs can be individually illuminated, so any one of 128 patterns can be displayed on a digit by illuminating certain LED segments and leaving the others dark, as shown in Fig. 17. Of these 128 possible patterns, the ten corresponding to the decimal digits are the most useful.

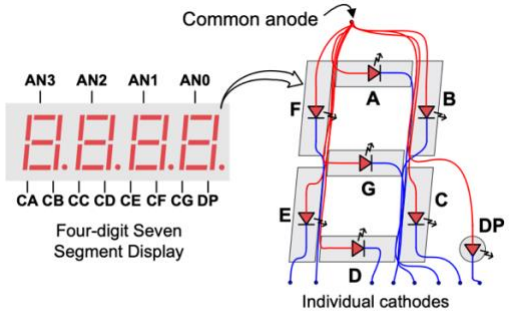

Figure 18. Common anode circuit node.

2. From the wiring of the board, which logic do you have to assign to the 7- segment pins (a to g and dot) to turn the LED on.

   Ans. ในการทำให้หลอด LED ติด เราทำให้ 7- segment pins อยู่ในสถานะ low

To illuminate a segment, the anode should be driven high while the cathode is driven low. However, since the Basys 3 uses transistors to drive enough current into the common anode point, the anode enables are inverted. Therefore, both the AN0..3 and the CA..G/DP signals are driven low when active.

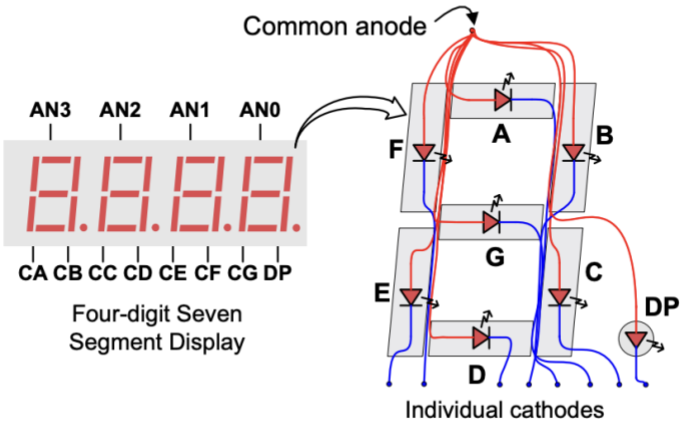

Figure 18. Common anode circuit node.

3. Given that the clock of the BASYS3 is around 10ns, how many bits do you have to divide the clock with to get the appropriate clock for the TDM. Please provide your analysis (calculation).

   Ans.

   For each of the four digits to appear bright and continuously illuminated, all four digits should be driven once every 1 to 16ms, for a refresh frequency of about 1 KHz to 60Hz. For example, in a 62.5Hz refresh scheme, the entire

   จาก reference manual 7- segment ควรถูกสลับทุกๆ 1 ถึง 16 ms เพื่อให้สายตาของมนุษย์ยังคงแยกไม่ออกว่ามีการกระพริบ ในการคำนวณนี้ผมเลือกใช้ 16ms

   จำนวน clock divider ที่ต้องใช้ $\log_2(\text{clock}_{\text{ที่ต้องการ}}/\text{clock}_{\text{จริงๆ}}) = \log_2(16\text{ms}/10\text{ns})$

   $= \log_2(1\ 600\ 000)$

   $= 20.6$

   ดังนั้นจำนวน clock divider ที่ต้องใช้คือ 20 bits