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E344 Assignment 1

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Report submitted in partial fulfilment of the requirements of the module Design (E) 344 for the degree Baccalaureus in Engineering in the Department of Electrical and Electronic Engineering at Stellenbosch University.

August 16, 2020

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Contents

List of Figures

List of Tables

Nomenclature

Variables and functions

I_{in}	Current drawn from the 9 VDC supply.
P_{in}	Power supplied by the 9 VDC supply.
P_{out}	Power supplied by the 5 VDC regulator.
$\%_{eff}$	Percentage regulator efficiency.
ΔP	Power dissipation.
$V_{I_{max}}$	Maximum rated input voltage.
V_D	Rated dropout voltage.
$P_{D_{max}}$	Maximum rated power dissipation.
V^+	Positive supply voltage.
V^-	Negative supply voltage.
$V_{stimulus}$	Temperature sensor signal.
$V_{bias_{inv}}$	Bias voltage of inverting stage.
V_{inv}	Inverting stage output voltage.
α	Op-amp gain
$V_{bias_{amp}}$	Bias voltage of amplifying stage.
V_{amp}	Amplifying stage output voltage.
f_{3dB}	3 dB bandwidth frequency.
$t_{90\%}$	90% rise time.
I_{tot}	Total current drawn.
c	Calibration constant.
T	Temperature measured.

Acronyms and abbreviations

LPF	low-pass filter
GND	ground
VDC	direct-current voltage

Chapter 1

System design

1.1. System overview

The block diagram for a temperature sensor conditioning system is shown in Fig. 1.1. The system is supplied by a 9 VDC battery, and performs conditioning of the temperature sensor data to produce an output signal which can be more easily interpreted by the user, in accordance with the specifications in [1]. Any measured temperature between 34°C and 42°C generates a defined output signal.

The voltage regulation and temperature conditioning sections of this system are designed, analysed and discussed in the remainder of this report. Further system functionality is to be added at a later stage. This functionality is not of immediate importance yet, but offers much-needed context to various design decisions (i.e. the system current limit of 100 mA).

1.2. Rationale

An inverting op-amp with unity gain is used to remove DC offset from the temperature sensor stimulus signal. Thereafter, a differential op-amp amplifies the signal to achieve the desired range of output values. A low-pass filter removes any noise from the amplified signal.

In order to supply the required 5 VDC to each op-amp, a linear voltage regulator is used to step down from the 9 VDC provided by the battery. Separate voltage dividers are also used to provide 0.69 VDC and 0.21 VDC bias voltages to the inverting and differential op-amps respectively.

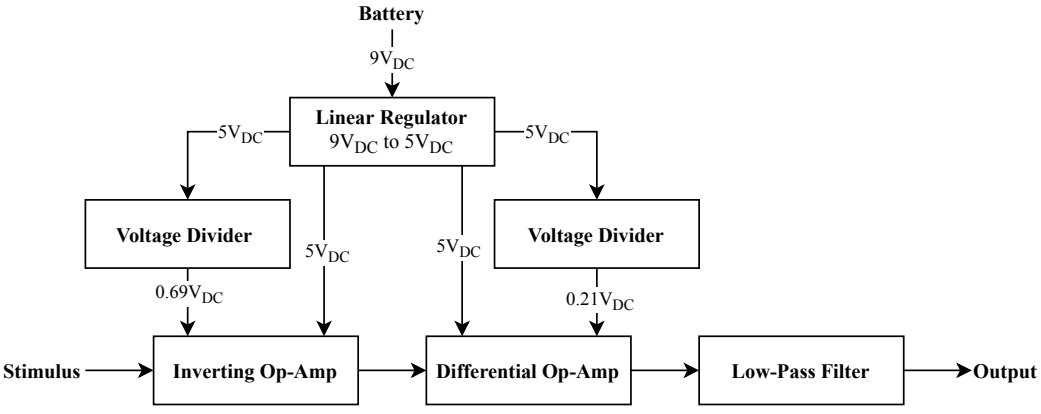


Figure 1.1: System diagram

Chapter 2

Voltage regulation

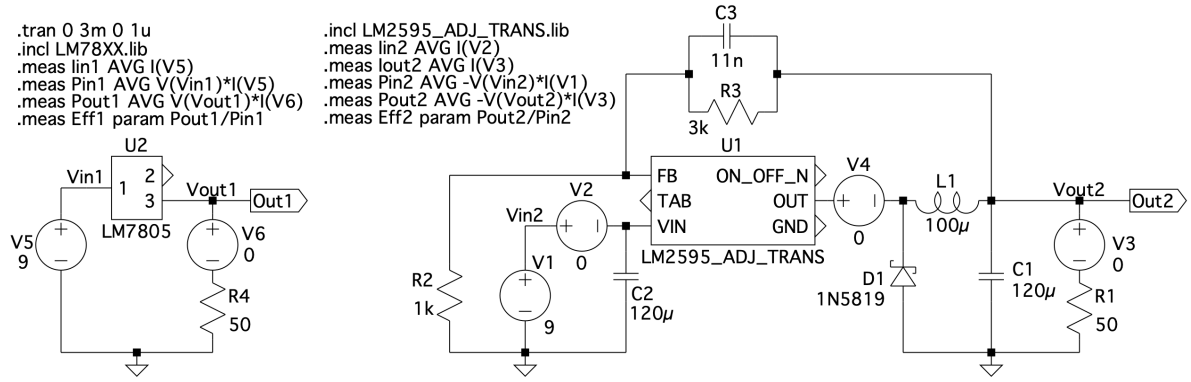
2.1. Introduction

Both a linear and switch-mode regulator are considered as voltage regulation solutions for the system. Identical scenarios, whereby a 50 kΩ load is connected to the regulator output, are simulated on LTSpice to compare various aspects of the functionality of each regulator. The component limitations in [2] and [3], and the simulation results are compared, and the more suitable regulator is chosen for the system design.

As per the system requirements [1], 9 VDC needs to be regulated down to 5 VDC in order to supply the positive input voltages for the amplification stage of the system. There is a voltage drop of 147 µV over the current sense resistor, but this value is too small to have any significant contribution to the system design, and so it is neglected. Additionally, a maximum current draw of 100 mA is allowed.

2.2. Design

Figure 2.1 shows the LTSpice models used to compare the regulators.



(a) Linear voltage regulator. **(b)** Switch-mode voltage regulator.

Figure 2.1: Circuit diagrams of the two voltage regulators.

The LM7805 linear regulator requires no additional design components to achieve the desired output, whereas the LM2595 switch-mode regulator requires an additional network of resistors, capacitors and inductors. This can be seen in Figure 2.1b. The switch-mode circuit

is designed in accordance with Figure 35 from [3], and using Equations 2.1 and 2.2.

$$V_{out} = V_{REF}\left(1 + \frac{R_3}{R_2}\right) \tag{2.1}$$

$$\therefore R_3 \approx 3\,\text{k}\Omega$$

$$C_3 = \frac{1}{31 \times 10^3 \times R_3} \approx 11\,\text{nF} \tag{2.2}$$

2.3. Results

Table 2.1 summarises the values of interest obtained via simulation, and from the datasheets [2] and [3], for each regulator. It is clear that the LM7805 linear regulator has a higher power efficiency $\%_{eff} = \frac{P_{out}}{P_{in}} \times 100$ than the LM2595 switch-mode regulator. It also remains well below the maximum rated power dissipation $P_{D_{max}} = 750\,\text{mW}$, as its power dissipation ΔP is only 446 mW.

The dropout voltage V_D of the linear regulator is higher than that of the switch-mode regulator, but this is of no concern since the system will only ever be supplied by a 9 VDC battery, which is still much higher than the 1.7 VDC linear regulator dropout voltage.

Table 2.1: Comparison of linear and switch-mode regulators.

		LM7805 linear regulator	LM2595 switch-mode regulator	
I_{in}		105,06	101,44	mA
P_{in}	$\frac{I_{in}}{V_{9VDC}}$	946	913,05	mW
P_{out}	$\frac{I_{out}}{V_{5VDC}}$	500	348,15	mW
$\%_{eff}$	$\frac{P_{out}}{P_{in}} \times 100$	52,85	38,13	%
ΔP	$P_{in} - P_{out}$	446	528,91	mW
$V_{I_{max}}$		30 [2]	45 [3]	V
V_D		1,7 [2]	0.8 [3]	V
$P_{D_{max}}$		750 [2]	internally limited [3]	mW

Figure 2.2 compares the output voltages obtained from the linear and switch-mode regulators after each was simulated in LTSpice. The LM7805 regulator produces a near-perfect expected 5 VDC output, shown in Figures 2.2a and 2.2b. The LM2595 regulator produces a less satisfying output closer to 4.9 VDC, seen in Figures 2.2c and 2.2d, and has a considerable amount more noise than the linear output, as noted in Figure 2.2e.

2.4. Summary

As seen in Figure 2.2, the LM7805 linear regulator performs as expected and produces a useful 5 VDC voltage, with no additional cost or design complexity. Any power limitations of the regulator, as stipulated in [2], will not affect the operation of the greater system.

The LM2595 switch-mode regulator produces an output voltage slightly lower than desired, around 4.9 VDC. It also requires numerous additional components, which increases the overall

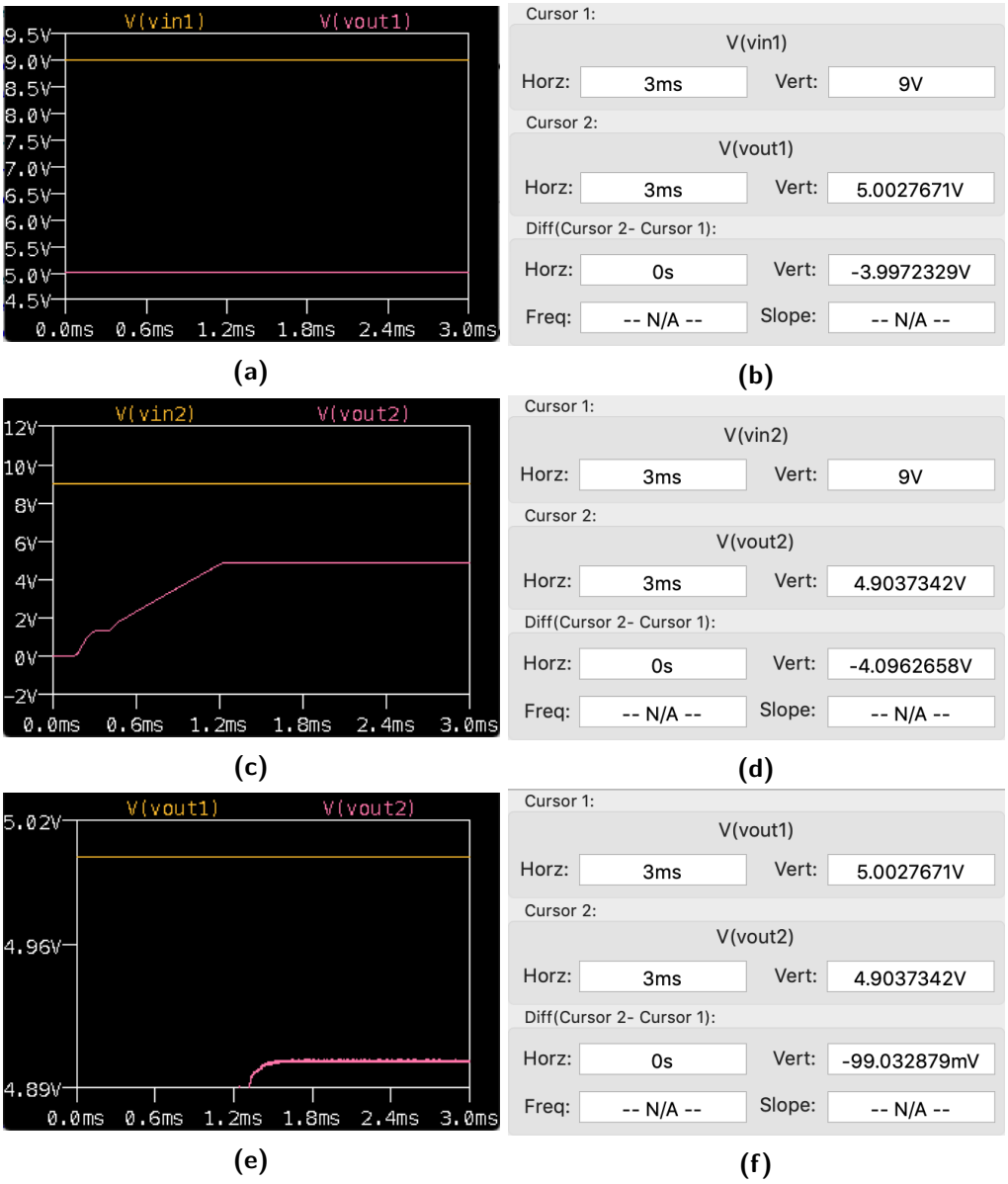


Figure 2.2: Comparing the linear and switch-mode regulators. (a), (b) LM7805 linear regulator input vs. output signals. (c), (d) LM2595 switch-mode regulator input vs. output signals. (e), (f) Linear regulator output vs. switch-mode regulator output.

cost and design complexity of the power supply. Most considerably, the switch-mode regulated signal produces far more noise than the linearly regulated signal, seen in Figure 2.2e.

For the above reasons, the LM7805 linear regulator is the chosen solution for the remainder of the system design.

Chapter 3

Temperature sensor conditioning circuit

3.1. Introduction

The conditioning circuit is given an output signal from a temperature sensor (the "stimulus"). This signal represents any temperature between 34°C and 42°C, but with significant noise and at an unusable voltage level range. This is because the sensor is capable of measuring temperatures starting at 0°C, equivalent to 0.5 VDC. The purpose of the conditioning circuit is to remove a majority of the noise and amplify the signal to a more useful range of voltage levels between 0.5 VDC and 4.5 VDC.

There are three stages to the conditioning circuit: an inversion stage, an amplification stage, and a noise filter stage. After all three stages, the output signal should reflect the temperature data in a proportional manner, as shown in Table 3.1. This is because the sensor measurement has a linear temperature coefficient of 20 mV/°C. The inversion and amplification stages are powered by the regulated voltage designed in Chapter 2.

Table 3.1: Temperature sensor data as stimulus and output voltages.

	Stimulus	Desired output	
34°C	1.18	0.50	[V]
36°C	1.22	1.50	[V]
38°C	1.26	2.50	[V]
40°C	1.30	3.50	[V]
42°C	1.34	4.50	[V]

3.2. Design

Appendix C shows the LTSpice model of the temperature sensor conditioning circuit.

All of the op-amps selected for this system are TLC2272 rail-to-rail amplifiers. The TL081 amplifier was also considered, but the TLC2272 has characteristics which are more suited to the system. The rail-to-rail op-amp can withstand a common-mode input voltage of equal value to the bottom rail, and only 1.5 V from the top rail [4]. In contrast, the TL081 recommends a common-mode voltage range [5] which allows for very little input range considering the system rails in accordance with [1]. The rails requirement stipulates that each op-amp in the circuit receives $V^+ = 5$ VDC and $V^- =$ GND.

3.2.1. Inversion stage

The inversion stage inverts the stimulus signal, and removes the DC offset created by the range of sensor values which will not be considered by this system (i.e. any temperature below 34°C or above 42°C). The signal is inverted in order to compensate for the inverting that occurs at the amplification stage. The DC offset is removed in order to simplify the calculations at the amplification stage, which adds a separate DC offset.

An inverting op-amp [6] with unity gain is used to design the inverting stage. In order to minimise the current drawn by the system, R_1 and R_2 are chosen as $100\,\text{k}\Omega$. The midpoint of the stimulus input is $1.6\,\text{V}$, and in order for the minimum value of the signal to be $\approx 0\,\text{V}$, the new midpoint needs to be $0.12\,\text{V}$. The necessary $V_{bias_{inv}}$ is calculated in Equation 3.1.

$$V_{bias_{inv}} = \frac{V_{stimulus} - V_{inv}}{2} - V_{inv} = \frac{1.6\,\text{V} - 0.12\,\text{V}}{2} - 0.12\,\text{V} = 0.69\,\text{V} \tag{3.1}$$

A voltage divider is needed to supply this $0.69\,\text{V}$ bias voltage. It is designed using Equation 3.2 and selecting $R_4 = 10\,\text{k}\Omega$. The input and bias voltages are between the maximum and minimum input and common-node voltages of the op-amp [4] of $V_{I_{max}} = V_{IC_{max}} = 5\,\text{V}$ and $V_{I_{min}} = V_{IC_{min}} = -0.3\,\text{V}$; this is confirmed during simulation.

$$V_{bias_{inv}} = \frac{5_{VDC} \times R_4}{R_3 + R_4} \tag{3.2}$$

$$\therefore R_3 = \frac{R_4 \times (5_{VDC} - V_{bias_{inv}})}{V_{bias_{inv}}} = \frac{10\,\text{k}\Omega \times (5\,\text{V} - 0.69\,\text{V})}{0.69\,\text{V}} = 62.5\,\text{k}\Omega$$

3.2.2. Amplification stage

The amplification stage increases the range of voltages used to represent the stimulus data. An inverting op-amp configuration [6] with a virtual ground is used. The desired output range is $3.5\,\text{V}$, so in accordance with [1], the ideal minimum and maximum output values are $0.5\,\text{V}$ and $4.5\,\text{V}$, respectively.

The midpoint of the inverted signal is $0.12\,\text{V}$, and the desired midpoint of the amplified signal is $2.5\,\text{V}$. The op-amp gain is therefore calculated by $\alpha = \frac{V_{amp}}{V_{inv}} = 20.8$. After several trial-and-error tests on LTSpice, $R_6 = 745\,\text{k}\Omega$ and $R_5 = 30\,\text{k}\Omega$ were selected to create this gain. In combination with the virtual ground bias voltage $V_{bias_{amp}}$ determined from Equation 3.3, this design proved to return the best results.

$$V_{amp} = \frac{R_6}{R_5} \times V_{inv} - V_{bias_{amp}} \tag{3.3}$$

$$\therefore V_{bias_{amp}} = \frac{R_6}{R_5} \times V_{inv} - V_{amp} = \frac{745\,\text{k}\Omega}{30\,\text{k}\Omega} \times 0.12\,\text{V} - 2.5\,\text{V} = 0.48\,\text{V}$$

Further tests on LTSpice show that the more ideal value for $V_{bias_{amp}}$ is proven to be $0.21\,\text{V}$. A voltage divider is needed to supply this bias voltage. The voltage divider is designed

using Equation 3.4 and selecting $R_9 = 10\,\text{k}\Omega$. The input and bias voltages are between the maximum and minimum input voltages of the op-amp [4] of $V_{I_{max}} = V_{IC_{max}} = 5\,\text{V}$ and $V_{I_{min}} = V_{IC_{min}} = -0.3\,\text{V}$; this is confirmed during simulation. The value for R_9 is adjusted slightly to $228\,\text{k}\Omega$ after further LTSpice simulation.

$$V_{bias_{amp}} = \frac{5_{VDC} \times R_9}{R_8 + R_9} \tag{3.4}$$

$$\therefore R_8 = \frac{R_9 \times (5_{VDC} - V_{bias_{amp}})}{V_{bias_{amp}}} = \frac{10\,\text{k}\Omega \times (5\,\text{V} - 0.21\,\text{V})}{0.21\,\text{V}} = 224\,\text{k}\Omega$$

3.2.3. Noise filter stage

The noise filter suppresses the sinusoidal 50 Hz noise on the sensor signal. A passive low-pass filter (LPF) is designed, in accordance with [7] and Equation 3.5. Select common capacitor value $C_1 = 0.2\,\mu\text{F}$ and design for a 3 dB bandwidth of $f_{3dB} = 4\,\text{Hz}$. The expected rise time $t_{90\%}$ is calculated by Equation 3.6.

$$f_{3dB} = \frac{1}{2\pi R_{10} C_1} \tag{3.5}$$

$$\therefore R_{10} = \frac{1}{2\pi f_{3dB} C_1} = \frac{1}{2\pi \times 4\,\text{Hz} \times 0.2\,\mu\text{F}} \approx 200\,\text{k}\Omega$$

$$t_{90\%} \cong \frac{0.35}{f_{3dB}} = \frac{0.35}{4} = 87.5\,\text{ms} \tag{3.6}$$

The total current of the conditioning circuit can now be calculated using Equation 3.7.

$$I_{tot} = \frac{5_{VDC}}{R_1 + R_2 + R_5 + R_6 + R_{10}} = 4.26\,\mu\text{A} \tag{3.7}$$

3.3. Results

Figure 3.1 depicts the simulation results obtained from the circuit in Appendix C. As stated in Section 3.2, some slight adjustments were made to the theoretical design of the conditioning circuit, particularly to the amplification and noise removal stages. It can be noted in Figure 3.1b that the minimum inverted signal value does not reach 0 V, which may be the reason why the virtual ground calculations for the amplification stage did not return complete accuracy in simulation and needed to be compensated for. The bode plot in Figure 3.1d shows that the 50 Hz noise has been significantly suppressed by the LPF.

Figure 3.2 depicts the simulation results for a 1°C step response. This was used to confirm that the rise time $t_{90\%}$ is less than 100 ms, as calculated in Equation 3.6. Cursors 1 and 2 in Figure 3.2b are 100 ms apart and show that there is voltage difference of $|\Delta V_{simul}| = 0.457\,\text{V}$. This is more than 0.450 V, which is 90% of $|\Delta V/1°C| = 0.5\,\text{V}$. This plot was also used to

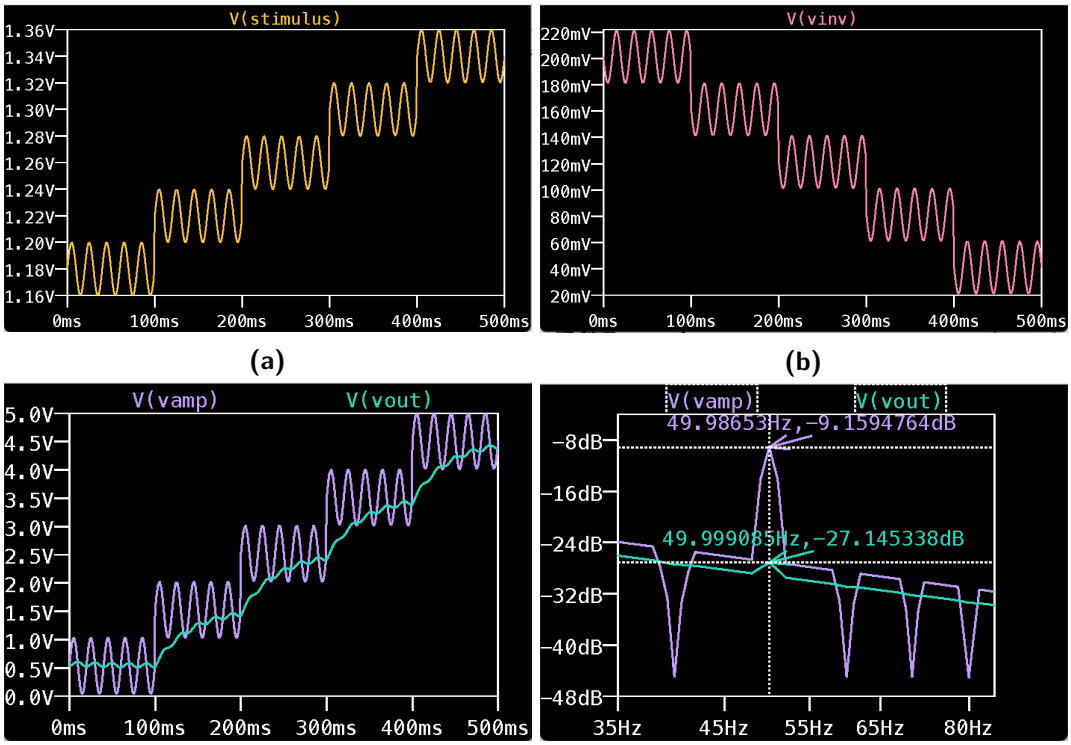


Figure 3.1: LTSpice simulation results. (a) Temperature sensor stimulus. (b) Inverting op-amp output. (c) Differential op-amp output and LPF output. (d) Bode plot of differential op-amp output and LPF output.

confirm that the 50 Hz sensor noise is indeed suppressed to less than 50 mV on the output.

3.4. Summary

The circuit in Appendix C performs as expected, within the specifications in [1]. Only slight adjustments needed to be made to the design in order to achieve the desired output. Sensor noise levels have been significantly reduced by the LPF and the final output signal successfully represents a range of temperature values as distinct voltage levels, as stipulated in Table 3.1.

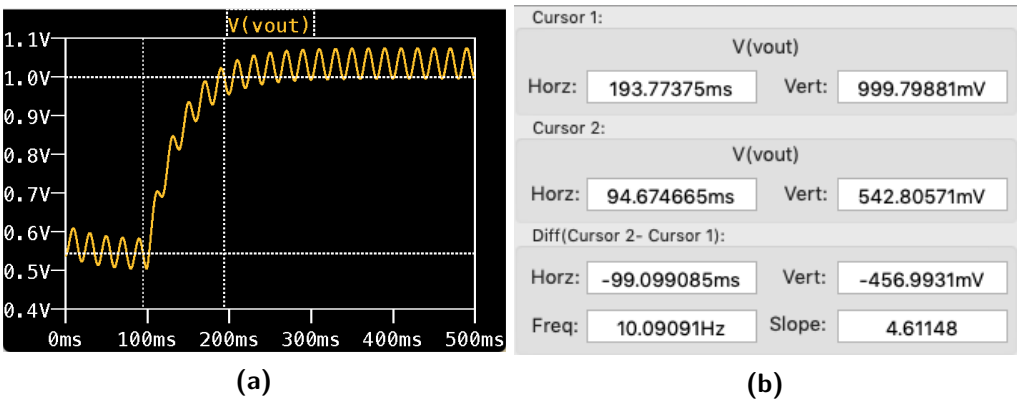


Figure 3.2: LTSpice simulation results. (a) 1°C step response plot. (b) Associated cursor values at 100 ms difference.

Chapter 4

System and conclusion

4.1. System

The system successfully meets all design specifications [1]. The current drawn from this system does not exceed $|I_{sense_{max}}| = 14.7\,\text{mA}$, as measured during simulation. Therefore the current limitation of 15 mA is adhered to and $\Delta I = 100 - 14.7 = 85.3\,\text{mA}$ is left for the rest of the system.

The full range of temperature values are measured and returned in accordance with Table 3.1. The 50 Hz sensor noise is sufficiently suppressed to less than 50 mV on the output. The 1°C step response time $t_{90\%}$ is less than 100 ms, shown in Figure 3.2a.

The voltage regulator integrated seamlessly with the temperature sensor conditioning circuit. Both of these sub-circuits will easily be able to integrate with any additional system functionality.

It is important to note that the simulation does take a significant amount of time to run. While it does remain under the specified limit of 2 minutes, this is a concern that should be further investigated before any additional functionality is added to the system.

An expected calibration constant c can be calculated based on the design of the conditioning circuit. This is done in Equation 4.1. The constant c is used to determine the measured sensor temperature T given the conditioned output signal V_{out}, as shown in Equation 4.2.

$$c = \frac{T_{max} - T_{min}}{\Delta V} = \frac{42°C - 34°C}{3.5\,\text{V}} = 1.6°C/V \tag{4.1}$$

$$T = c \times (V_{out} - 0.5) + 32 \tag{4.2}$$

4.2. Lessons learnt

1. There is a key balance between prioritising system accuracy and considering cost and scalability of a product.

2. It is helpful to make tangible records of every step of the design process to refer back to, no matter how insignificant it may seem in the moment.

3. Working neatly will benefit one in the long run.

Bibliography

[1] M. J. Booysen. (2020, July) E-design 344 assignment 1 2020. [Online]. Available: https://learn.sun.ac.za/pluginfile.php/2304150/mod_resource/content/3/E344_Ass1.pdf

[2] Fairchild Semiconductor Corporation, *MC78LXXA/LM78LXXA 3-Terminal 0.1 A Positive Voltage Regulator*, March 2013. [Online]. Available: www.fairchildsemi.com

[3] Texas Instruments Incorporated, *LM2595 SIMPLE SWITCHER (TM) Power Converter*, May 2016. [Online]. Available: www.ti.com

[4] *TLC227x, TLC227xA: Advanced LinCMOS Rail-to-Rail Operational Amplifiers*, March 2016. [Online]. Available: www.ti.com

[5] *TL08xx JFET-Input Operational Amplifiers*, May 2015. [Online]. Available: www.ti.com

[6] Electronics Tutorials, *Operational Amplifiers Summary*, 2018. [Online]. Available: https://www.electronics-tutorials.ws/opamp/opamp_8.html

[7] *Passive Low Pass Filter*, 2019. [Online]. Available: https://www.electronics-tutorials.ws/filter/filter_2.html

Appendix A

Social contract

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E-design 344 Social Contract

2020

The purpose of this document is to establish commitment between the student and the organisers of E344. Beyond the commitment made here, it is not binding.

In the months preceeding the term, the lecturer (Thinus Booysen) and the Teaching Assistant (Michael Ritchie) spent countless hours to prepare for E344 to ensure that you get your money's worth and that you are enabled to learn from the module and demonstrate and be assessed on your skills. We commit to prepare for the module, to set the tests and assessments fairly, to be reasonably available, and to provide feedback and support as best and fast we can. We will work hard to give you the best opportunity to learn from and pass analogue electronic design E344.

Signature: ..... Date: 13 July 2020

.....

I, *Thandi Colley* have registered for E344 of my own volition with the intention to learn of and be assessed on the principals of analogue electronic design. Despite the potential publication of supplementary videos on specific topics, I acknowledge that I am expected to attend the lectures and lab sessions to make the most of these appointments and learning opportunities. Moreover, I realise I am expected to spend the additional requisite number of hours on E344 as specified in the yearbook.

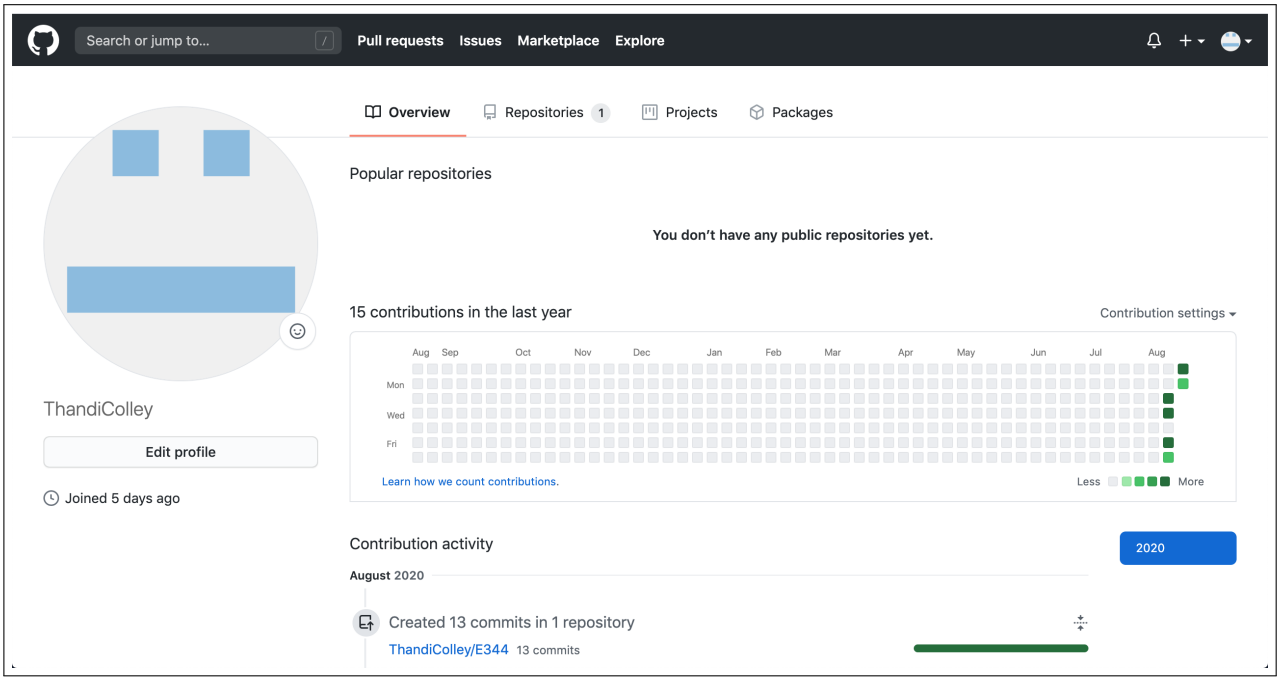
I acknowledge that E344 is an important part of my journey to becoming a professional engineer, and that my conduct should be reflective thereof. This includes doing and submitting my own work, working hard, starting on time, and assimilating as much information as possible. It also includes showing respect towards the University's equipment, staff, and their time.

Signature: ..... Date: *17 August 2020*

1

Appendix B

GitHub Activity Heatmap



Appendix C

Circuit diagram