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E344 Assignment 3

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Nomenclature

Variables and functions

α	Op-amp gain
C_{HPF}	High-pass filter capacitor.
C_{LPF}	Low-pass filter capacitor.
ΔI	Current dissipation.
I_{in}	Current drawn from the 9 VDC supply.
I_{tot}	Total current drawn.
$\%_{eff}$	Percentage regulator efficiency.
f	Base frequency.
f_{3dB}	3 dB bandwidth frequency.
ΔP	Power dissipation.
$P_{D_{max}}$	Maximum rated power dissipation.
P_{in}	Power supplied by the 9 VDC supply.
P_{out}	Power supplied by the 5 VDC regulator.
R_{sense}	Internal resistance of sensor.
$rate_{bpm}$	Heart-rate in bpm.
V^+	Positive supply voltage.
V^-	Negative supply voltage.
V_D	Rated dropout voltage.
V_{ID}	Maximum rated differential input voltage.
$V_{IN_{max}}$	Maximum rated input voltage.
$V_{IN_{min}}$	Minimum rated input voltage.
T	Period of heartbeat signal.
$t_{90\%}$	90% rise time.

Acronyms and abbreviations

AC	alternating-current
ADC	analogue-to-digital converter
bpm	beats per minute
DC	direct-current
FFT	fast Fourier transform
GND	ground
HPF	high-pass filter
LPF	low-pass filter
GND	ground
VDC	direct-current voltage

Chapter 1

System design

1.1. System overview

The block diagram for a temperature and heartbeat sensor conditioning system is shown in Figure 1.1. The system is supplied with 9 VDC. It performs the conditioning of temperature and heart-rate sensor data to produce an output signal which can be more easily interpreted by the user in accordance with the specifications in [1] and [2]. The output signals from this system are further processed and calibrated to provide the user with the correct temperature and heart-rate information from the sensor input. This report investigates the design and analysis of the temperature- and heartbeat-conditioning circuits, as well as the calibration and digitisation of the system output signals.

Taking into consideration the total current budget of 100 mA and the current draw of the two conditioning subsystems, there remains 70 mA for further functionality of the system. This may be needed for further interfacing with the sensors or the micro-controller which will perform processing of the output signals.

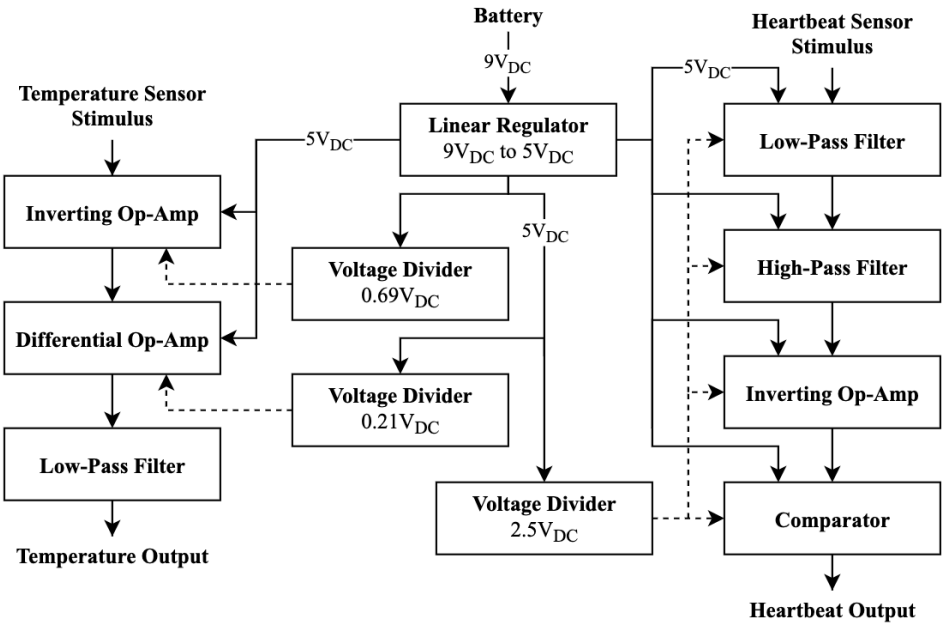


Figure 1.1: System diagram

Chapter 2

Voltage regulation

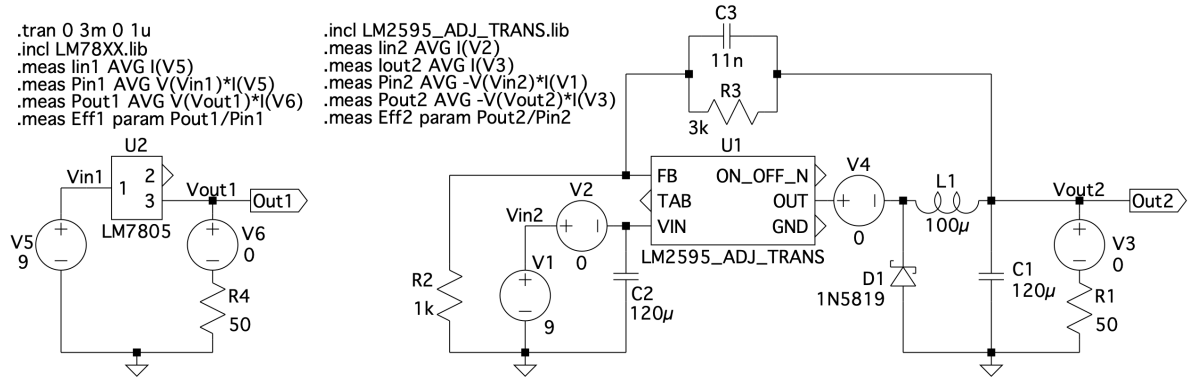
2.1. Introduction

Both a linear and switch-mode regulator are considered as voltage regulation solutions for the system. Identical scenarios, whereby a 50 kΩ load is connected to the regulator output, are simulated on LTSpice to compare various aspects of the functionality of each regulator. The component limitations in [3] and [4], and the simulation results are compared, and the more suitable regulator is chosen for the system design.

As per the system requirements [2], 9 VDC needs to be regulated down to 5 VDC in order to supply the positive input voltages for the amplification stage of the system. There is a voltage drop of 147 µV over the current sense resistor, but this value is too small to have any significant contribution to the system design, and so it is neglected. Additionally, a maximum current draw of 100 mA is allowed.

2.2. Design

Figure 2.1 shows the LTSpice models used to compare the regulators.



(a) Linear voltage regulator. **(b)** Switch-mode voltage regulator.

Figure 2.1: Circuit diagrams of the two voltage regulators.

The LM7805 linear regulator requires no additional design components to achieve the desired output, whereas the LM2595 switch-mode regulator requires an additional network of resistors, capacitors and inductors. This can be seen in Figure 2.1b. The switch-mode circuit

is designed in accordance with Figure 35 from [4], and using Equations 2.1 and 2.2.

$$V_{out} = V_{REF}\left(1 + \frac{R_3}{R_2}\right) \tag{2.1}$$

$$\therefore R_3 \approx 3\,\text{k}\Omega$$

$$C_3 = \frac{1}{31 \times 10^3 \times R_3} \approx 11\,\text{nF} \tag{2.2}$$

2.3. Results

Table 2.1 summarises the values of interest obtained via simulation, and from the datasheets [3] and [4], for each regulator. It is clear that the LM7805 linear regulator has a higher power efficiency $\%_{eff} = \frac{P_{out}}{P_{in}} \times 100$ than the LM2595 switch-mode regulator. It also remains well below the maximum rated power dissipation $P_{D_{max}} = 750\,\text{mW}$, as its power dissipation ΔP is only 446 mW.

The dropout voltage V_D of the linear regulator is higher than that of the switch-mode regulator, but this is of no concern since the system will only ever be supplied by a 9 VDC battery, which is still much higher than the 1.7 VDC linear regulator dropout voltage.

Table 2.1: Comparison of linear and switch-mode regulators.

		LM7805 linear regulator	LM2595 switch-mode regulator	
I_{in}		105,06	101,44	mA
P_{in}	$\frac{I_{in}}{V_{9VDC}}$	946	913,05	mW
P_{out}	$\frac{I_{out}}{V_{5VDC}}$	500	348,15	mW
$\%_{eff}$	$\frac{P_{out}}{P_{in}} \times 100$	52,85	38,13	%
ΔP	$P_{in} - P_{out}$	446	528,91	mW
$V_{I_{max}}$		30 [3]	45 [4]	V
V_D		1,7 [3]	0.8 [4]	V
$P_{D_{max}}$		750 [3]	internally limited [4]	mW

Figure 2.2 compares the output voltages obtained from the linear and switch-mode regulators after each was simulated in LTSpice. The LM7805 regulator produces a near-perfect expected 5 VDC output, shown in Figures 2.2a and 2.2b. The LM2595 regulator produces a less satisfying output closer to 4.9 VDC, seen in Figures 2.2c and 2.2d, and has a considerable amount more noise than the linear output, as noted in Figure 2.2e.

2.4. Summary

As seen in Figure 2.2, the LM7805 linear regulator performs as expected and produces a useful 5 VDC voltage, with no additional cost or design complexity. Any power limitations of the regulator, as stipulated in [3], will not affect the operation of the greater system.

The LM2595 switch-mode regulator produces an output voltage slightly lower than desired, around 4.9 VDC. It also requires numerous additional components, which increases the overall

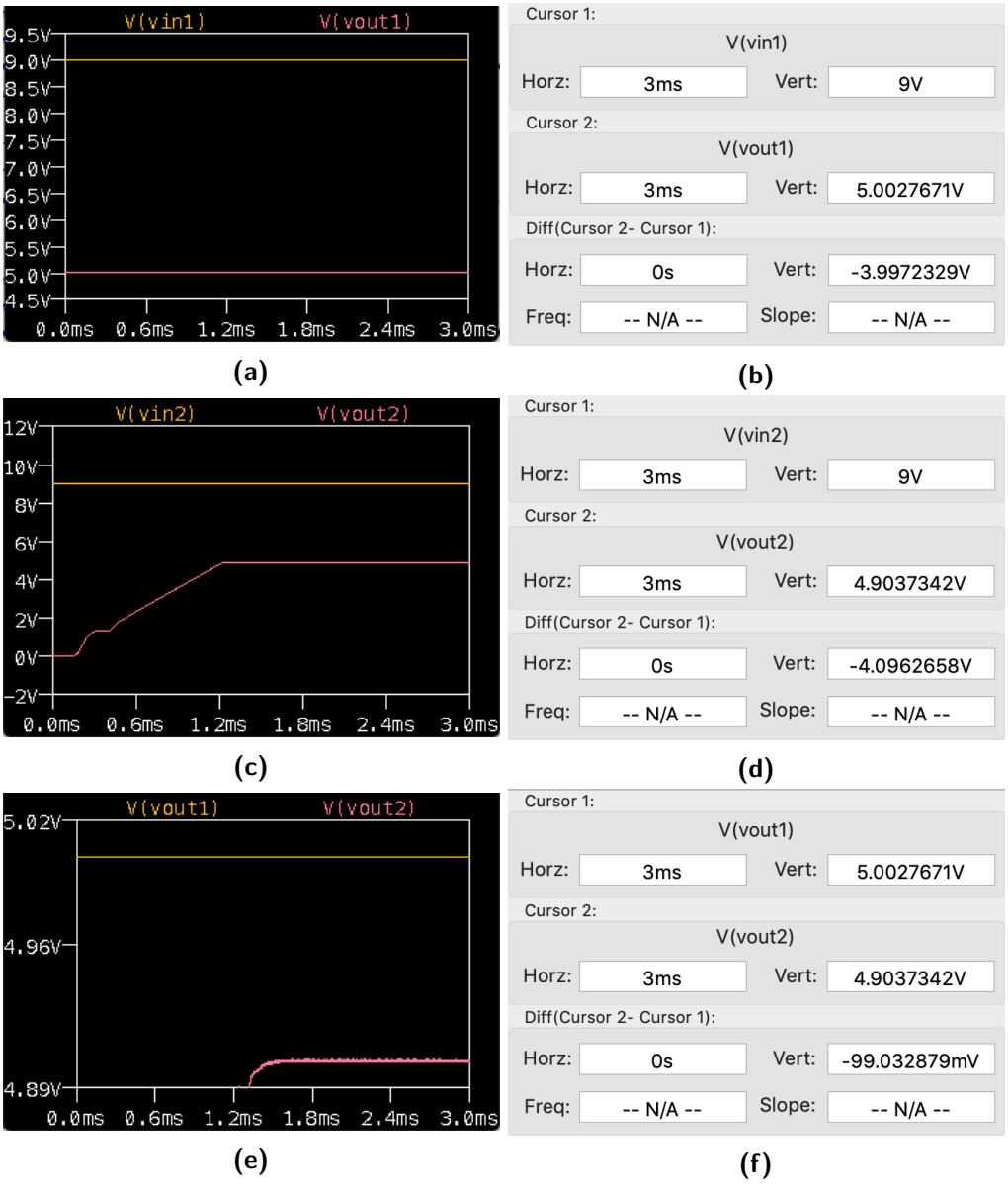


Figure 2.2: Comparing the linear and switch-mode regulators. (a), (b) LM7805 linear regulator input vs. output signals. (c), (d) LM2595 switch-mode regulator input vs. output signals. (e), (f) Linear regulator output vs. switch-mode regulator output.

cost and design complexity of the power supply. Most considerably, the switch-mode regulated signal produces far more noise than the linearly regulated signal, seen in Figure 2.2e.

For the above reasons, the LM7805 linear regulator is the chosen solution for the remainder of the system design.

Chapter 3

Temperature sensor conditioning circuit

3.1. Introduction

The conditioning circuit is given an output signal from a temperature sensor (the "stimulus"). This signal represents any temperature between 34°C and 42°C, but with significant noise and at an unusable voltage level range. This is because the sensor is capable of measuring temperatures starting at 0°C, equivalent to 0.5 VDC. The purpose of the conditioning circuit is to remove a majority of the noise and amplify the signal to a more useful range of voltage levels between 0.5 VDC and 4.5 VDC.

There are three stages to the conditioning circuit: an inversion stage, an amplification stage, and a noise filter stage. After all three stages, the output signal should reflect the temperature data in a proportional manner, as shown in Table 3.1. This is because the sensor measurement has a linear temperature coefficient of 20 mV/°C. The inversion and amplification stages are powered by the regulated voltage designed in Chapter 2.

Table 3.1: Temperature sensor data as stimulus and output voltages.

	Stimulus	Desired output	
34°C	1.18	0.50	[V]
36°C	1.22	1.50	[V]
38°C	1.26	2.50	[V]
40°C	1.30	3.50	[V]
42°C	1.34	4.50	[V]

3.2. Design

Figure C.1 in Appendix C shows the LTSpice model of the temperature sensor conditioning circuit.

All of the op-amps selected for this system are TLC2272 rail-to-rail amplifiers. The TL081 amplifier was also considered, but the TLC2272 has characteristics which are more suited to the system. The rail-to-rail op-amp can withstand a common-mode input voltage of equal value to the bottom rail, and only 1.5 V from the top rail [5]. In contrast, the TL081 recommends a common-mode voltage range [6] which allows for very little input range considering the system rails in accordance with [2]. The rails requirement stipulates that each op-amp in the circuit receives $V^+ = 5$ VDC and $V^- =$ GND.

3.2.1. Inversion stage

The inversion stage inverts the stimulus signal, and removes the DC offset created by the range of sensor values which will not be considered by this system (i.e. any temperature below 34°C or above 42°C). The signal is inverted in order to compensate for the inverting that occurs at the amplification stage. The DC offset is removed in order to simplify the calculations at the amplification stage, which adds a separate DC offset.

An inverting op-amp [7] with unity gain is used to design the inverting stage. In order to minimise the current drawn by the system, R_1 and R_2 are chosen as $100\,\text{k}\Omega$. The midpoint of the stimulus input is $1.6\,\text{V}$, and in order for the minimum value of the signal to be $\approx 0\,\text{V}$, the new midpoint needs to be $0.12\,\text{V}$. The necessary $V_{bias_{inv}}$ is calculated in Equation 3.1.

$$V_{bias_{inv}} = \frac{V_{stimulus} - V_{inv}}{2} - V_{inv} = \frac{1.6\,\text{V} - 0.12\,\text{V}}{2} - 0.12\,\text{V} = 0.69\,\text{V} \tag{3.1}$$

A voltage divider is needed to supply this $0.69\,\text{V}$ bias voltage. It is designed using Equation 3.2 and selecting $R_4 = 10\,\text{k}\Omega$. The input and bias voltages are between the maximum and minimum input and common-node voltages of the op-amp [5] of $V_{I_{max}} = V_{IC_{max}} = 5\,\text{V}$ and $V_{I_{min}} = V_{IC_{min}} = -0.3\,\text{V}$; this is confirmed during simulation.

$$V_{bias_{inv}} = \frac{5_{VDC} \times R_4}{R_3 + R_4} \tag{3.2}$$

$$\therefore R_3 = \frac{R_4 \times (5_{VDC} - V_{bias_{inv}})}{V_{bias_{inv}}} = \frac{10\,\text{k}\Omega \times (5\,\text{V} - 0.69\,\text{V})}{0.69\,\text{V}} = 62.5\,\text{k}\Omega$$

3.2.2. Amplification stage

The amplification stage increases the range of voltages used to represent the stimulus data. An inverting op-amp configuration [7] with a virtual ground is used. The desired output range is $3.5\,\text{V}$, so in accordance with [2], the ideal minimum and maximum output values are $0.5\,\text{V}$ and $4.5\,\text{V}$, respectively.

The midpoint of the inverted signal is $0.12\,\text{V}$, and the desired midpoint of the amplified signal is $2.5\,\text{V}$. The op-amp gain is therefore calculated by $\alpha = \frac{V_{amp}}{V_{inv}} = 20.8$. After several trial-and-error tests on LTSpice, $R_6 = 745\,\text{k}\Omega$ and $R_5 = 30\,\text{k}\Omega$ were selected to create this gain. In combination with the virtual ground bias voltage $V_{bias_{amp}}$ determined from Equation 3.3, this design proved to return the best results.

$$V_{amp} = \frac{R_6}{R_5} \times V_{inv} - V_{bias_{amp}} \tag{3.3}$$

$$\therefore V_{bias_{amp}} = \frac{R_6}{R_5} \times V_{inv} - V_{amp} = \frac{745\,\text{k}\Omega}{30\,\text{k}\Omega} \times 0.12\,\text{V} - 2.5\,\text{V} = 0.48\,\text{V}$$

Further tests on LTSpice show that the more ideal value for $V_{bias_{amp}}$ is proven to be $0.21\,\text{V}$. A voltage divider is needed to supply this bias voltage. The voltage divider is designed

using Equation 3.4 and selecting $R_9 = 10\,\text{k}\Omega$. The input and bias voltages are between the maximum and minimum input voltages of the op-amp [5] of $V_{I_{max}} = V_{IC_{max}} = 5\,\text{V}$ and $V_{I_{min}} = V_{IC_{min}} = -0.3\,\text{V}$; this is confirmed during simulation. The value for R_9 is adjusted slightly to $228\,\text{k}\Omega$ after further LTSpice simulation.

$$V_{bias_{amp}} = \frac{5_{VDC} \times R_9}{R_8 + R_9} \tag{3.4}$$

$$\therefore R_8 = \frac{R_9 \times (5_{VDC} - V_{bias_{amp}})}{V_{bias_{amp}}} = \frac{10\,\text{k}\Omega \times (5\,\text{V} - 0.21\,\text{V})}{0.21\,\text{V}} = 224\,\text{k}\Omega$$

3.2.3. Noise filter stage

The noise filter suppresses the sinusoidal 50 Hz noise on the sensor signal. A passive low-pass filter (LPF) is designed, in accordance with [8] and Equation 3.5. Select common capacitor value $C_1 = 0.2\,\mu\text{F}$ and design for a 3 dB bandwidth of $f_{3dB} = 4\,\text{Hz}$. The expected rise time $t_{90\%}$ is calculated by Equation 3.6.

$$f_{3dB} = \frac{1}{2\pi R_{10} C_1} \tag{3.5}$$

$$\therefore R_{10} = \frac{1}{2\pi f_{3dB} C_1} = \frac{1}{2\pi \times 4\,\text{Hz} \times 0.2\,\mu\text{F}} \approx 200\,\text{k}\Omega$$

$$t_{90\%} \cong \frac{0.35}{f_{3dB}} = \frac{0.35}{4} = 87.5\,\text{ms} \tag{3.6}$$

The total current of the conditioning circuit can now be calculated using Equation 4.5.

$$I_{tot} = \frac{5_{VDC}}{R_1 + R_2 + R_5 + R_6 + R_{10}} = 4.26\,\mu\text{A} \tag{3.7}$$

3.3. Results

Figure 3.1 depicts the simulation results obtained from the circuit in Figure C.1 from Appendix C. As stated in Section 3.2, some slight adjustments were made to the theoretical design of the conditioning circuit, particularly to the amplification and noise removal stages. It can be noted in Figure 3.1b that the minimum inverted signal value does not reach 0 V, which may be the reason why the virtual ground calculations for the amplification stage did not return complete accuracy in simulation and needed to be compensated for. The bode plot in Figure 3.1d shows that the 50 Hz noise has been significantly suppressed by the LPF.

Figure 3.2 depicts the simulation results for a 1°C step response. This was used to confirm that the rise time $t_{90\%}$ is less than 100 ms, as calculated in Equation 3.6. Cursors 1 and 2 in Figure 3.2b are 100 ms apart and show that there is voltage difference of $|\Delta V_{simul}| = 0.457\,\text{V}$. This is more than 0.450 V, which is 90% of $|\Delta V/1°C| = 0.5\,\text{V}$. This plot was also used to

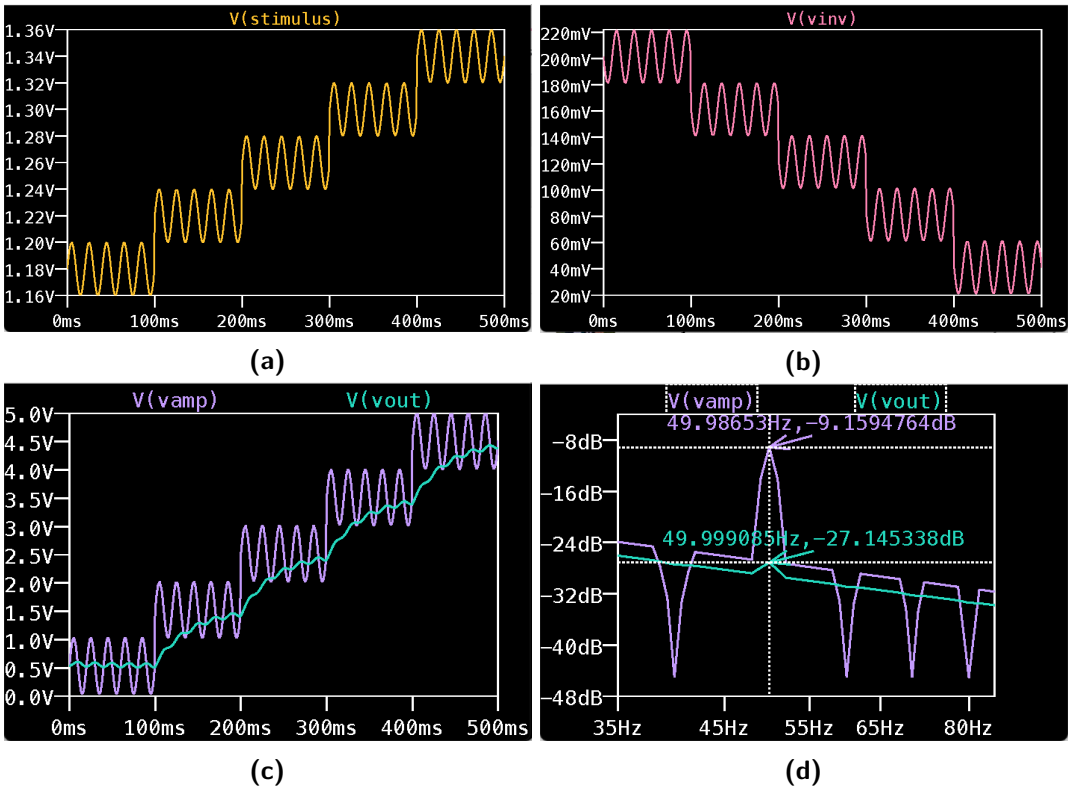


Figure 3.1: LTSpice simulation results. (a) Temperature sensor stimulus. (b) Inverting op-amp output. (c) Differential op-amp output and LPF output. (d) Bode plot of differential op-amp output and LPF output.

confirm that the 50 Hz sensor noise is indeed suppressed to less than 50 mV on the output.

3.4. Summary

The circuit in Figure C.1 performs as expected, within the specifications in [2]. Only slight adjustments needed to be made to the design in order to achieve the desired output. Sensor noise levels have been significantly reduced by the LPF and the final output signal successfully represents a range of temperature values as distinct voltage levels, as stipulated in Table 3.1.

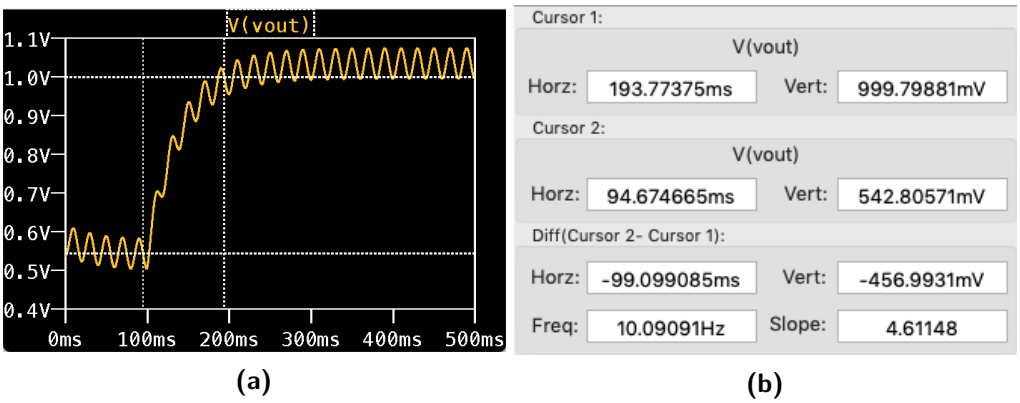


Figure 3.2: LTSpice simulation results. (a) 1°C step response plot. (b) Associated cursor values at 100 ms difference.

Chapter 4

Heart rate sensor

4.1. Introduction

The conditioning circuit is given an output signal from a heartbeat sensor (the "stimulus"). This signal represents any heart-rate from 50 bpm to 150 bpm, but contains significant noise and DC disturbance. The purpose of the conditioning circuit is to interpret the sensor output and return distinct pulses for each heartbeat so that the heart-rate can be determined.

There are three stages to the conditioning circuit: a filtering stage, an amplification stage, and a comparator stage. The filtering stage comprises of a third-order Butterworth low-pass filter and a second-order Sallen-Key high-pass filter. Both of these configurations were built in accordance with [9]. The inverting op-amp used for the amplification stage was configured using the theory in [7] and for the comparator, [10] was consulted.

The technical requirements of each component need to be considered in the design of the signal conditioning system. Particularly, the voltage limitations of each op-amp stipulated in [6] need to be carefully considered.

4.2. Design

Figure C.2 in Appendix C shows the heartbeat sensor conditioning circuit. This circuit was designed for a heartbeat signal with a DC component of 1.5 V and amplitude of 33.30 mVpk, and allows for a variation in these specifications of ±0.2 VDC and ±3.33 mVpk. TL081 op-amps were used for all op-amp applications of this design. This is because the TL081 is cost-effective, simple, and allows for efficient simulation for the circuit in LTSpice [6].

Table 4.1: Heartbeat signal frequency components.

$rate_{bpm}$	f	$2f$	$3f$	
50 bpm	0.83	1.67	2.50	[Hz]
60 bpm	1.00	2.00	3.00	[Hz]
90 bpm	1.50	3.00	4.50	[Hz]
120 bpm	2.00	4.00	6.00	[Hz]
150 bpm	2.50	5.00	7.50	[Hz]

Upon analysis of the given heartbeat signals using the FFT, it was determined that the heartbeat itself is comprised of three separate signals: one at the "base" frequency determined by the heart-rate in bpm ($f = \frac{rate_{bpm}}{60}$), and two additional signals at double and triple the base frequency. This is detailed in Table 4.1. The frequency information for a heart-rate of

50 bpm is also deduced, as this heart-rate also needs to be designed for. All other frequency components in the heartbeat signal are noise or disturbance components. These unwanted components are observed around 250 mHz, 20 Hz, 50 Hz and further even higher frequencies. All of this frequency information is considered in the conditioning circuit design below.

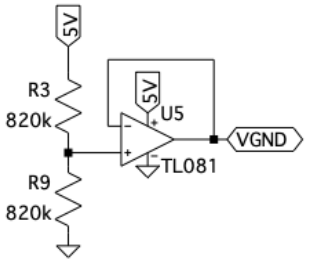


Figure 4.1: Virtual ground circuit.

In order to account for the 1.5 V DC offset of the heartbeat sensor signal, and to simplify the thresholding process in the comparator stage of the circuit, a **virtual ground** level is selected at half of the supply voltage. $V_{gnd} = \frac{V^+}{2} = 2.5\,\text{V}$. This virtual ground is created using voltage division and a voltage-follower op-amp as shown in Figure 4.1. Large common-value resistors $R = 820\,\text{k}\Omega$ are chosen to reduce the current usage of the circuit. Equation 4.1 explains how V_{gnd} is obtained.

$$V_{gnd} = \frac{R_3}{R_9} \times V^+ = \frac{820\,\text{k}\Omega}{820\,\text{k}\Omega} \times 5 = 2.5\,\text{V} \tag{4.1}$$

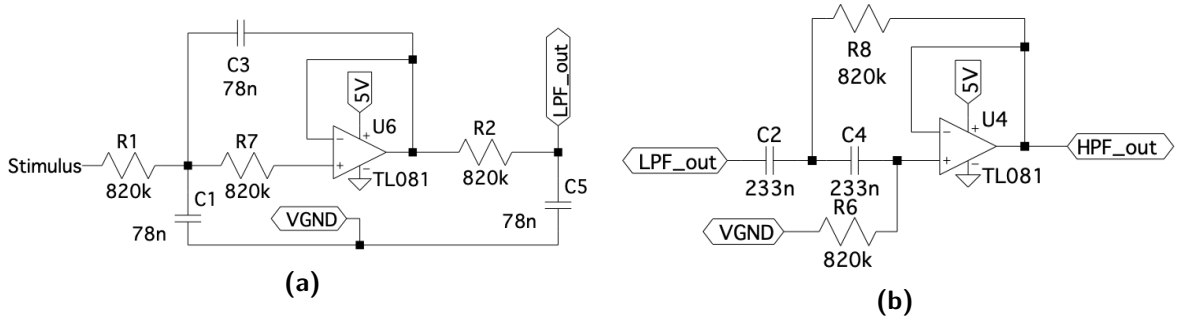


Figure 4.2: Filter stage. (a) Third-order Butterworth low-pass filter. (b) Second-order Sallen-Key high-pass filter.

The **filter stage** removes noise and DC disturbance from the heartbeat signal. Only the base frequencies (f) of each heart-rate were considered in the filter design. This is because sufficient information can be gathered from the base frequencies for further conditioning, and the design complexity of the filter stage will be reduced. Large common-value resistors $R = 820\,\text{k}\Omega$ are chosen to reduce the current usage of the circuit. As seen in Table 4.1, the highest allowable frequency is 2.5 Hz. The third-order Butterworth low-pass filter configuration [9] shown in Figure 4.2a is designed for this frequency. The capacitor values are calculated by Equation 4.2.

$$C_{LPF} = \frac{1}{2\pi R f_{LPF}} = \frac{1}{2\pi \times 820\,\text{k}\Omega \times 2.5\,\text{Hz}} = 78\,\text{nF} \tag{4.2}$$

As seen in Table 4.1, the lowest allowable frequency is 0.83 Hz. The second-order Sallen-Key high-pass filter configuration [9] shown in Figure 4.2b is designed for this frequency. The capacitor values are calculated by Equation 4.3.

$$C_{HPF} = \frac{1}{2\pi R f_{HPF}} = \frac{1}{2\pi \times 820\,\text{k}\Omega \times 0.83\,\text{Hz}} = 233\,\text{nF} \tag{4.3}$$

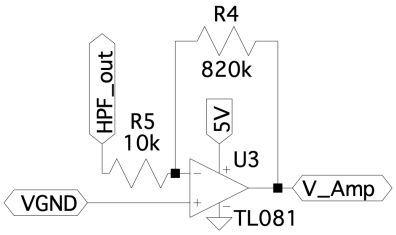


Figure 4.3: Inverting op-amp with gain.

The **amplification stage** applies a gain to the filtered heartbeat signal in order to allow for easier thresholding in the comparator stage. A large common-value feedback resistor $R_4 = 820\,\text{k}\Omega$ is chosen to reduce the current usage of the circuit. An analysis of the filtered signal shows that there is only a small AC variance ranging from 2.5 mVpk to 3.6 mVpk for the given heart-rates. To remain consistent in using common-value resistors and to prevent using too small of a resistor so as not to draw too much current, an input resistor $R_5 = 10\,\text{k}\Omega$ is chosen. The gain factor of this amplifier configuration is calculated by Equation 4.4 [**?**].

$$\alpha = -\frac{R_4}{R_5} = -\frac{820\,\text{k}\Omega}{10\,\text{k}\Omega} = 82 \tag{4.4}$$

This gain should return a heartbeat signal with an AC variance ranging from 0.205 Vpk to 0.295 Vpk for the given heart-rates. This range is sufficient for the thresholding functionality of the comparator stage.

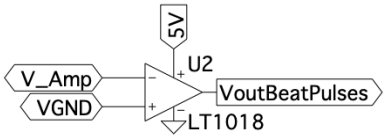


Figure 4.4: Op-amp comparator.

The **comparator stage** implements a simple op-amp comparator [10], shown in Figure 4.4, to output distinct square pulses for each heartbeat from the sensor signal. A reference voltage $V_{gnd} = 2.5\,\text{V}$ is compared to the filtered and inverse-amplified sensor signal V_{amp}. If $V_{amp} < V_{gnd}$, then $V_{out} = V^+ = 5\,\text{V}$. If $V_{amp} > V_{gnd}$, then $V_{out} = V^- = 0\,\text{V}$.

In accordance with [1], the pulse duration for each heartbeat needs to be 150 ms or longer. Table 4.2 indicates the period for each signal determined by the heart-rate in bpm ($T = \frac{60}{rate_{bpm}}$). From this, it is found that the smallest period is that of the 150 bpm signal, and so this signal needs to be most closely considered when designing the pulse length of the output. Notably, one can deduce that as long as the comparator identifies around half of the

Table 4.2: Period of each heartbeat signal.

$rate_{bpm}$	T	$\frac{1}{2}T$	
50 bpm	1.20	0.60	[s]
60 bpm	1.00	0.50	[s]
90 bpm	0.67	0.33	[s]
120 bpm	0.50	0.25	[s]
150 bpm	0.40	0.20	[s]

signal as surpassing the reference voltage, the pulse should be longer than 150 ms. This is because $\frac{1}{2}T_{150_{bpm}} = 200\,\text{ms} > 150\,\text{ms}$. For this reason, the reference voltage is chosen as the value around which the filtered and amplified signal is centered, i.e. 2.5 V. This threshold voltage should also account for the allowed specification deviations mentioned in Section 4.2.

The total current of the conditioning circuit can now be calculated using Equation 4.5. The current draw of the virtual ground stage is not included as this stage is present in the temperature sensor conditioning circuit from Chapter 3 and so has already been accounted for.

$$I_{tot} = \frac{V^+}{R_1 + R_2 + R_4 + R_5 + R_6 + R_8} = 1.22\,\mu\text{A} \tag{4.5}$$

4.3. Results

Figure 4.5 shows that the **full range** of heart-rates from 60 bpm to 150 bpm can be measured and conditioned by the system in Figure C.2 Appendix C. One can note in Figure 4.5c and Figure 4.5d that the **pulse duration** of both the 60 bpm and 150 bpm conditioned signals is longer than 150 ms, which is in accordance with [1].

Upon simulation of the circuit in Appendix C, the current through R_{sense} is determined to be 15.3 mA. This current represents the **total current of the circuit**, and is well within the specifications in [1].

All **op-amps** perform as expected. The input signal for the virtual ground voltage divider, filter stage and amplification stage remains within the TL081 common-node voltages (1 V to 4 V) [6]. The datasheet does not specify a value for $V_{IN_{min}}$ but at 15 V, $V_{IN_{max}}$ is significantly larger than our signal which is centered tightly around 2.5 V. The differential input voltage $V_{ID} = 30\,\text{V}$ is also far larger than any of the voltage values being handled in this system.

Figure D.1 in Appendix D depicts the **frequency response** of the filter stage. It is clear when analysing the cursor values that the noise and disturbance of the heartbeat signal is sufficiently filtered.

The **thresholding** of the comparator stage was measured and is shown in Figure E.1 in Appendix E. The maximum and minimum allowable specification deviations as mentioned in Section 4.2 were applied to the 60 bpm and 150 bpm signals respectively to obtain these plots. From this, it is clear that even with the most extreme deviations from the original heartbeat sensor signal, the thresholding around 2.5 V proves successful.

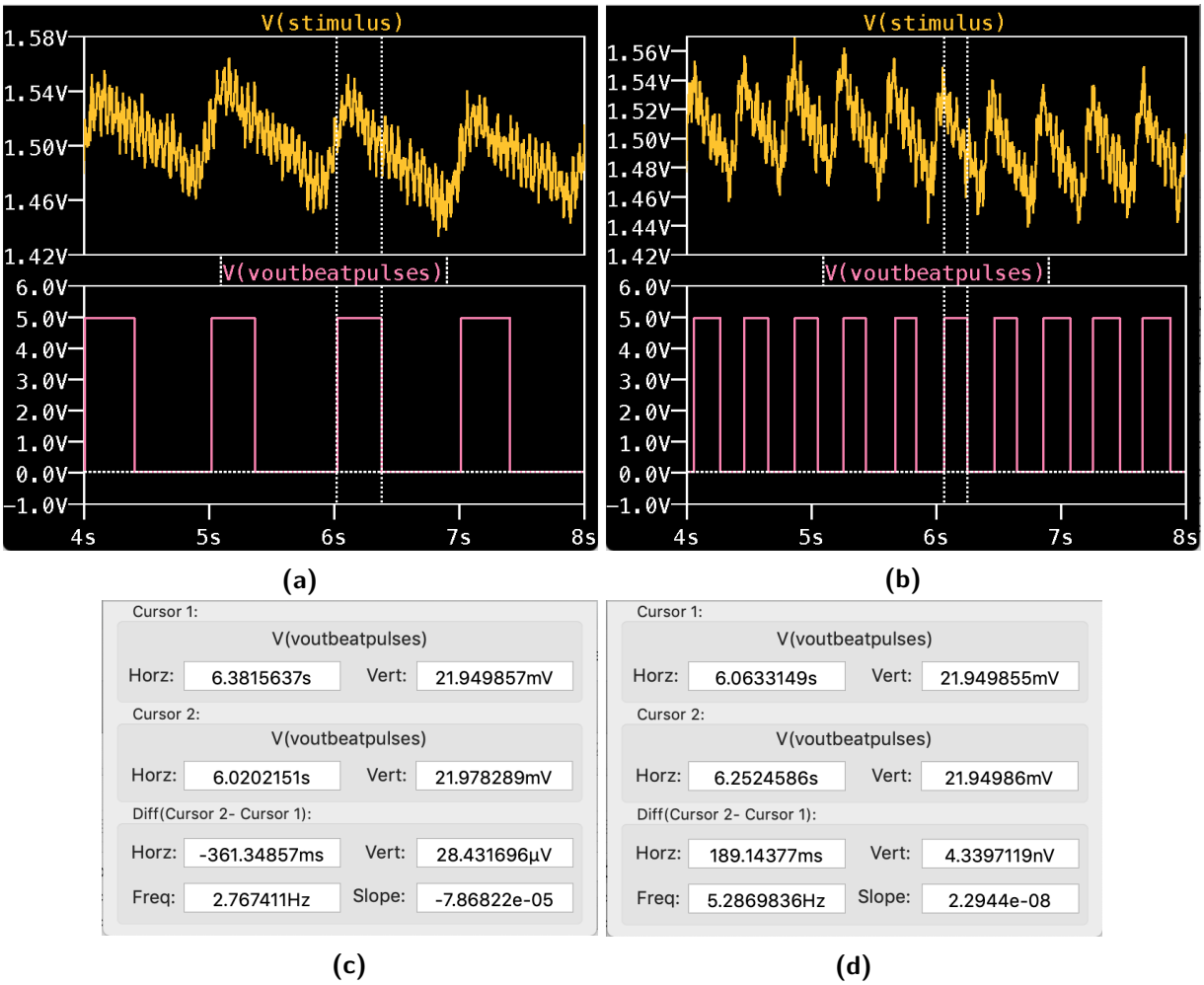


Figure 4.5: Conditioning circuit input and output simulation results. (a) Input and output at 60 bpm. (b) Input and output at 150 bpm. (c) Pulse duration at 60 bpm. (d) Pulse duration at 150 bpm.

4.4. Summary

The conditioning circuit in Appendix C performs as expected, and within the specifications of [1]. This includes the allowable specification variations of $\pm 0.2\,\text{VDC}$ and $\pm 3.33\,\text{mVpk}$ on the heartbeat sensor signals.

The circuit has been designed to be able to process all heart-rates from 50 bpm to 150 bpm. Although simulation and testing was only done on heart-rates as low as 60 bpm, theoretical calculations do support the same functionality for a heart-rate of 50 bpm. In practical applications this will need to be further investigated before implementation.

After simulation, the total current drawn from the conditioning circuit, while well within specifications, is significantly higher than the calculated value. This is likely due to assumptions made in the theoretical calculation, but could be due to a design or component error. This also would require further investigation before practical application.

Chapter 5

Calibration and digitisation

5.1. Temperature sensor

5.1.1. Analytical design

This system has access to a 10-bit ADC. Since the range of output values for the full range of temperatures is 4 V and the temperature gradient is 500 mV/°C, the temperature resolution can be calculated as in Equation 5.1.

$$res_{ADC} = \frac{V_{range}}{2^{10} \times \Delta T} = \frac{4000\,\text{mV}}{2^{10} \times 500\,\text{mV}} = 0.007\,812\,5\,\text{°C/bit} \tag{5.1}$$

We expect the temperature to have a linear relationship with the circuit output voltage, and therefore having an equation of the form $y = mx + c$, or $T = m \times V + c$. The unknown constants in this equation are calculated in Equations 5.2 and 5.3 using the maximum and minimum known temperature and voltage values as depicted in Table 3.1.

$$m = \frac{T_{max} - T_{min}}{V_{max} - Vmin} = \frac{42\,\text{°C} - 34\,\text{°C}}{4.5\,\text{V} - 0.5\,\text{V}} = 2\,\text{°C/V} \tag{5.2}$$

$$c = T_{max} - m \times V_{max} = 42\,\text{°C} - 2 \times 4.5\,\text{V} = 33\,\text{°C} \tag{5.3}$$

Hence, the analytical calibration relationship is $T = 2 \times V + 33$.

5.1.2. Empirical design

The steady-state output values of the temperature sensor conditioning circuit are obtained and compared to the analytical values in Table 5.1. This table shows a slight error margin, likely due to noise compensation, circuit component non-idealities and rounding off of values during the design of the circuit. However, the linear calibration equation obtained from the measured values is $T = 2.014 \times V + 32.916$, which is not very far off of the analytically obtained equation. This equation is implemented as a short Python script, described briefly by Algorithm 5.1. Upon assessment of the Python script, the values in the last column of Table 5.1 are obtained, showing that calibration is accurate within 1 °C.

Algorithm 5.1: Temperature calibration pseudocode

1: Calculate mean value of *amplitude*
2: Calculate and return *temperature* as an integer

Table 5.1: Analytical, empirical and assessment results for temperature calibration.

$T_{in}[°C]$	$V_{ana}[V]$	$V_{emp}[V]$	$V_{error}[\%]$	$T_{out}[°C]$
34	0.5	0.538	7.6	34
36	1.5	1.531	2.1	36
38	2.5	2.524	1.0	38
40	3.5	3.517	0.5	40
42	4.5	4.510	0.2	42

5.2. Heart rate sensor

Algorithm 5.2: Heart-rate calibration pseudocode

```
for 6 seconds at 1ms intervals do
    Set amplitude to current amplitude
    if amplitude is larger than (amplitude_prev + 4) then
        if n is 0 then
            Set t_start to current time
        end if
        Increase n
        Set t_end to current time
    end if
    Set amplitude_prev to amplitude
end for
Calculate and return rate_BPM as an integer
```

From the circuit, we can obtain the number of heartbeats observed in a time period n, the time at the first rising edge of a heartbeat t_{start} and the time at the last rising edge of a heartbeat t_{end}. This allows us to calculate the heart-rate as follows: $rate_{bpm} = \frac{n-1}{t_{end}-t_{start}} \times 60$. This equation is implemented in a short Python script, described briefly by Algorithm 5.2. Upon assessment of the Python script, the values in Table 5.2 are obtained, showing that calibration is accurate within 2 bpm.

Table 5.2: Assessment results for heart-rate calibration.

$rate_{in}$	$rate_{out}$	
80	80	[bpm]
100	99	[bpm]
120	119	[bpm]

Chapter 6

System and conclusion

6.1. System

The system in Figure C.1 from Appendix C successfully meets all design specifications in [2], [1] and [11]. The full range of temperature values are measured and returned in accordance with Table 3.1. The 50 Hz sensor noise is sufficiently suppressed to less than 50 mV on the output. The 1°C step response time $t_{90\%}$ is less than 100 ms, as shown in Figure 3.2a.

The reported temperature meets the accuracy requirement well within 2 seconds and is accurate to 1 °C for any temperature within the valid input range. The temperature digitisation can successfully be performed using a 10-bit ADC.

The circuit in Figure C.2 from Appendix C meets all design specifications in [1]. The full range of heart-rate values are measured and returned as distinct pulses for each heartbeat. These pulses can potentially be used to determine an analogue heart-rate using a transducer. Each pulse has a duration of 150 ms or higher.

The reported heart-rate meets the accuracy requirement well within 6s and is accurate to 2 bpm for the full input range. The heartbeat conditioning system was designed for a very particular type of sensor input, and might need significant adjustment to accommodate sensor input which does not have a DC component of 1.5 V or a heartbeat signal amplitude of 33.30 mVpk. Additionally, if there is a new noise signal which falls in the range of 0.8 Hz to 2.5 Hz, it is likely to distort the signal and may prevent accurate conditioning and interpretation of the heart-rate.

The voltage regulator will integrate seamlessly with the temperature and heart-rate sensor conditioning circuits. The current drawn from this system does not exceed $|I_{sense_{max}}| = 14.7 + 15.3 = 30\,\text{mA}$, as measured during simulation. Therefore the current limitation of 0 mA is adhered to and $\Delta I = 100 - 30 = 70\,\text{mA}$ remains for any further interfacing or additional functionality of the system.

6.2. Lessons learnt

1. There is a key balance between prioritising system accuracy and considering cost and scalability of a product.

2. It is helpful to make tangible records of every step of the design process to refer back to, no matter how insignificant it may seem in the moment.

3. Python does not work very well on a Mac.

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Appendix A

Social contract

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E-design 344 Social Contract

2020

The purpose of this document is to establish commitment between the student and the organisers of E344. Beyond the commitment made here, it is not binding.

In the months preceeding the term, the lecturer (Thinus Booysen) and the Teaching Assistant (Michael Ritchie) spent countless hours to prepare for E344 to ensure that you get your money's worth and that you are enabled to learn from the module and demonstrate and be assessed on your skills. We commit to prepare for the module, to set the tests and assessments fairly, to be reasonably available, and to provide feedback and support as best and fast we can. We will work hard to give you the best opportunity to learn from and pass analogue electronic design E344.

Signature: ..... Date: 13 July 2020 .....

.....

I, ... have registered for E344 of my own volition with the intention to learn of and be assessed on the principals of analogue electronic design. Despite the potential publication of supplementary videos on specific topics, I acknowledge that I am expected to attend the lectures and lab sessions to make the most of these appointments and learning opportunities. Moreover, I realise I am expected to spend the additional requisite number of hours on E344 as specified in the yearbook.

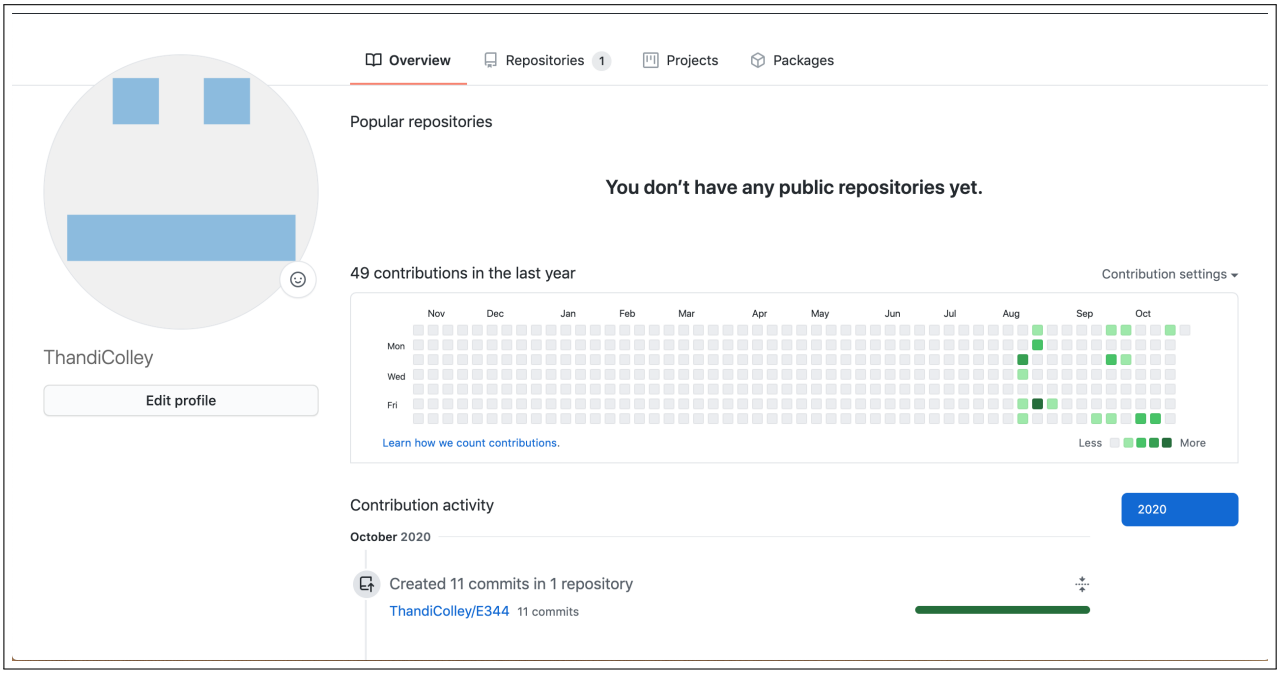
I acknowledge that E344 is an important part of my journey to becoming a professional engineer, and that my conduct should be reflective thereof. This includes doing and submitting my own work, working hard, starting on time, and assimilating as much information as possible. It also includes showing respect towards the University's equipment, staff, and their time.

Signature: ..... Date: .....

1

Appendix B

GitHub Activity Heatmap



Appendix C

Circuit diagrams

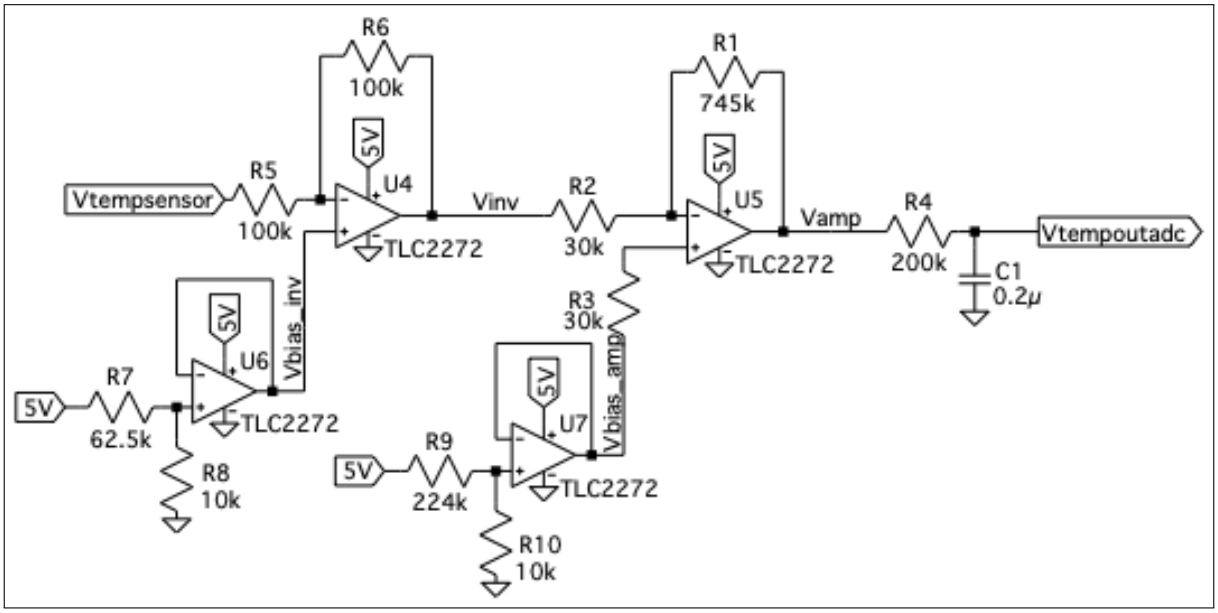


Figure C.1: Temperature conditioning circuit

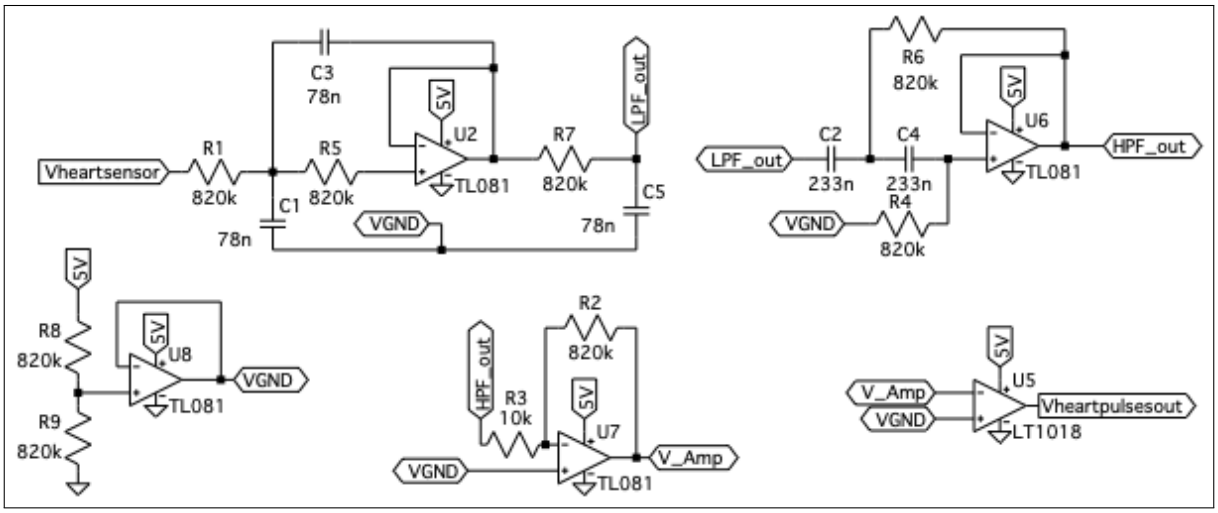


Figure C.2: Heartbeat conditioning circuit

Appendix D

Simulation results: frequency analysis

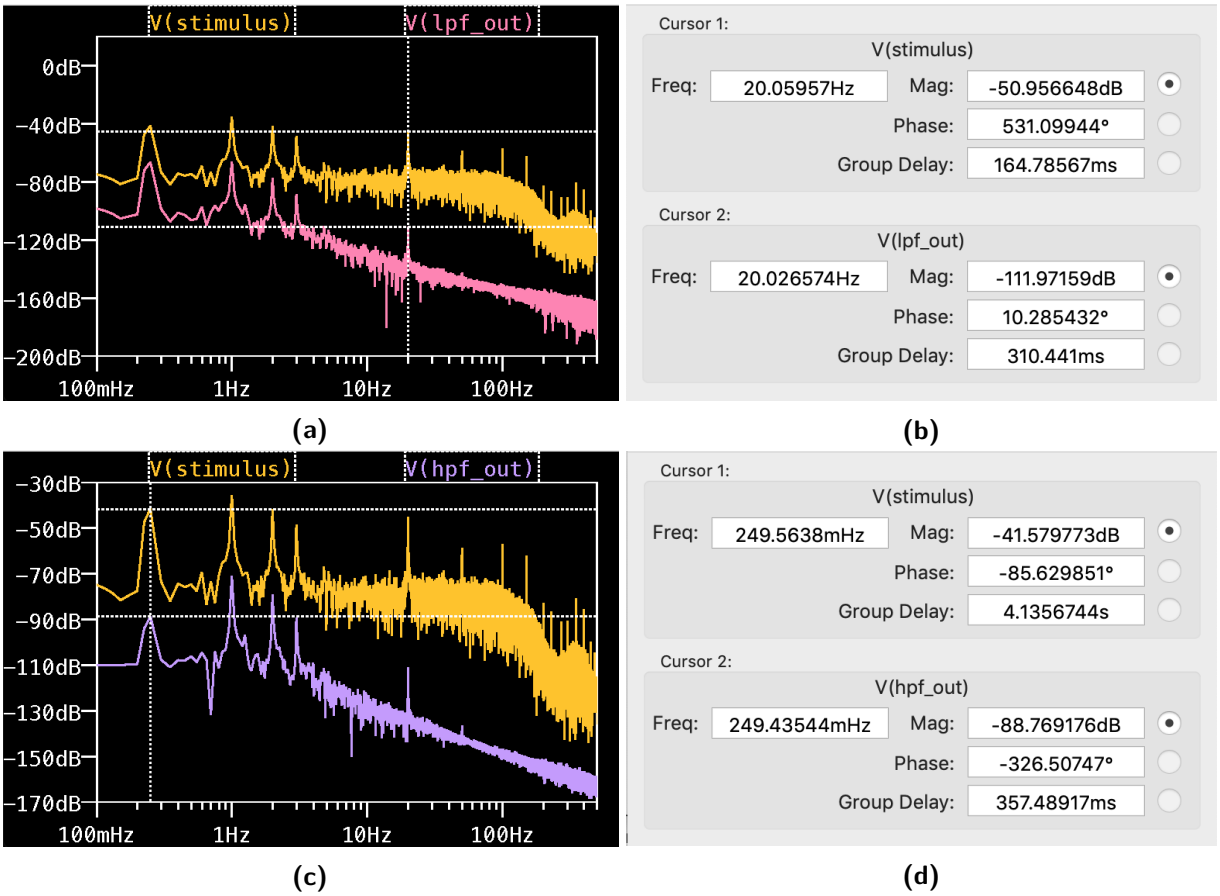


Figure D.1: Frequency analysis of low-pass and high-pass filters. (a) Frequency response of low-pass filter. (b) Plot values at 20 Hz. (c) Frequency response of high-pass filter. (d) Plot values at 250 mHz.

Appendix E

Simulation results: thresholding analysis

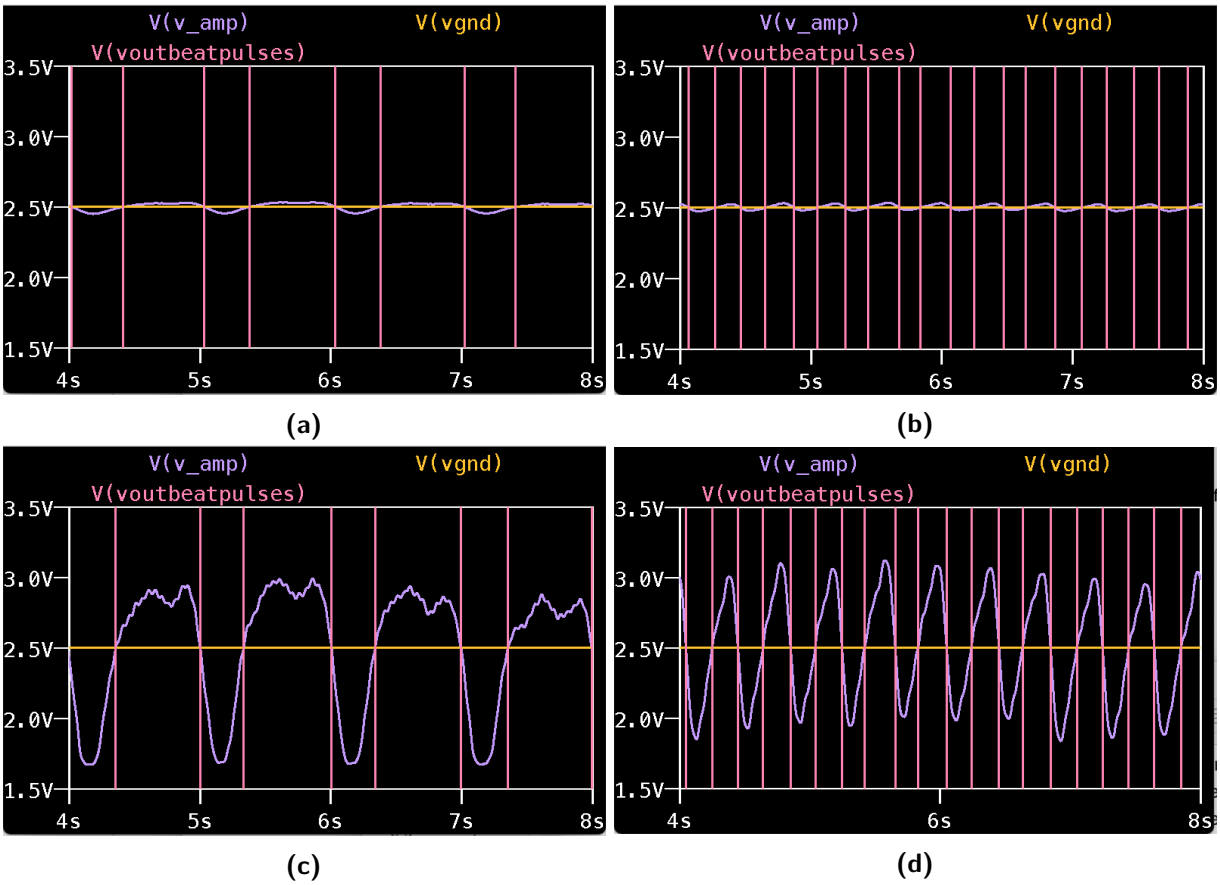


Figure E.1: Thresholding demonstration with specification deviations. (a) Negative deviation applied at 60 bpm. (b) Negative deviation applied at 150 bpm. (c) Positive deviation applied at 60 bpm. (d) Positive deviation applied at 150 bpm.