

SWINBURNE UNIVERSITY

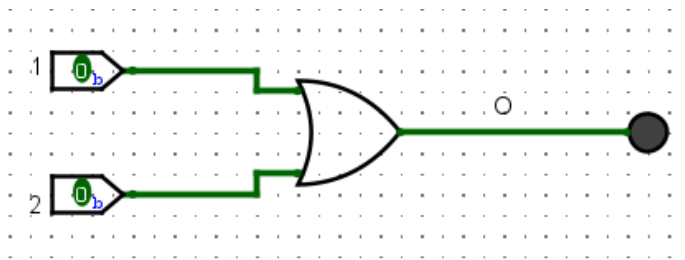
LAB 01

COS10004 – Computer System

CONG THANH NGO

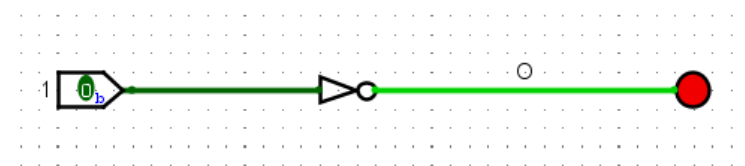
9/10/2021

OR Gate



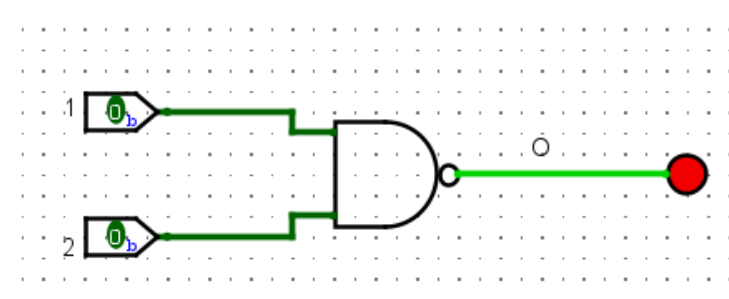
Pin 1	Pin 2	Output
1	0	1
1	1	1
0	1	1
0	0	0

NOT Gate



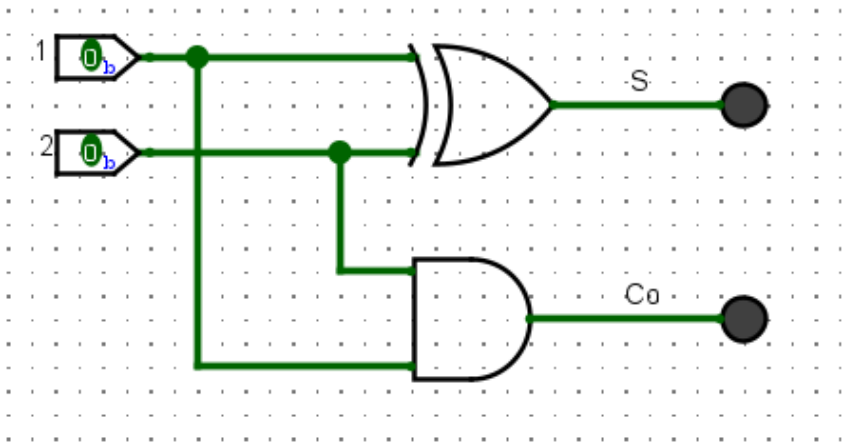
Pin 1	Output
0	1
1	0

NAND Gate



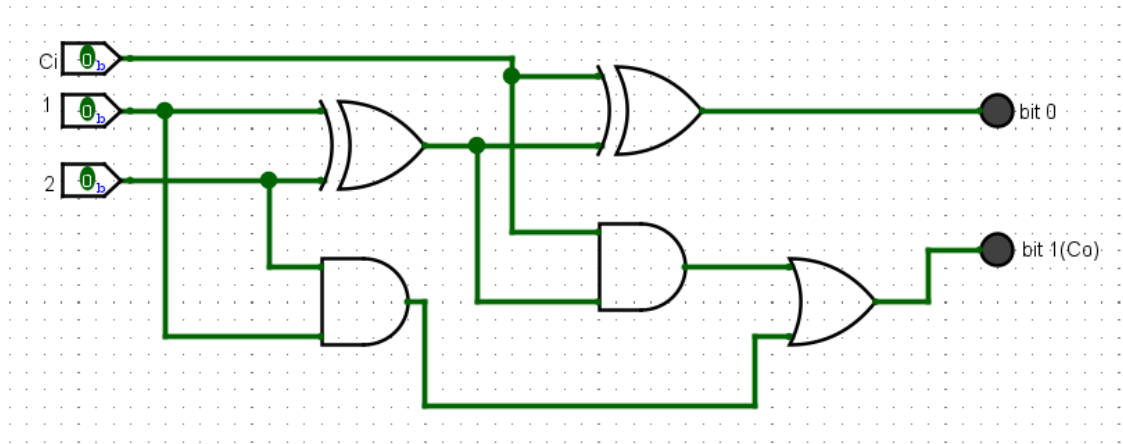
Pin 1	Pin 2	Output
0	0	1
0	1	1
1	1	0
1	0	1

Half Adder



Input 1	Input 2	Sum Output	Carry Output
1	1	0	1
1	0	1	0
0	1	1	0
0	0	0	0

Full Adder



Input 1	Input 2	Carry In	Sum Output	Carry Output
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1