# ANALYSIS OF TRAP CHARGES FOR TFET DEVICE

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***Abstract:*** ***An overview of the many sources of trap charges in TFETs, such as interface states, oxide defects, and bulk traps, is given in the study's opening section. This study suggests a novel analytical approach to calculate the trap charge density in TFETs. The paper also covers methods to lessen the effect of trap charges on TFET reliability and performance. This research study concludes with a full examination of trap charges in TFET devices, covering their causes, consequences, techniques of characterization, and mitigation tactics. The results of this study help to clarify trap-related problems in TFETs and offer helpful recommendations for designing and enhancing TFET devices for improved performance and dependability in low-power electronic applications***

**Index Terms—**Work-function engineering, tunnel field effect transistor, interface trap charges, gate-oxide stack

## I. INTRODUCTION

Metal-oxide semiconductor field-effect transistors (MOSFETs) have been viewed as a promising technology in the era of microelectronic

the fundamental components of VLSI circuitry. The MOSFET technology can be scaled down with a number of benefits, including lower costs, better high-frequency performance, and higher packing densities. Despite these benefits, ongoing MOSFET reduction has a number of fundamental problems, including subthreshold swing (SS) limitations of 60 mV/decade, increased leakage current, and short-channel effects [1].

These limitations of MOSFETs may be solved by tunnel field effect transistors (TFETs) [2] through [7].

Due to its capabilities, TFET is a good choice for a number of applications, including low-power and analog/RF ones [8] through [10]. However, ambipolar conduction, a reduced ON-state current, and subpar performance at higher frequencies are issues that TFETs must deal with. Numerous architectures, including as strained-Si, electrically doped, hetero-gate dielectric, and pocket doping, have been considered to address these problems [11]–[19]. These structural alterations have been found to be more effective at suppressing ambipolar conduction, but they also have significant costs and lattice mismatch. Additionally, the use of work function engineering in TFETs lowers ambipolarity but also impairs their performance in the analogue and RF spectrum [20].
A new dual-material gate-oxide-stack double-gate TFET (DMGOSDG-TFET) has been researched in [21] for the improvement of the ON-state current and superior performance in terms of linearity parameters.

The DMGOSDG-TFET uses high-k dielectric (HfO2) to improve the electric field between the gate and its sil icon. The ambipolarity current is suppressed when a dual work function is used at the gate [20].However, there is also a significant issue with device dependability brought on by interface trap charges (ITCs).

When a device is being manufactured or exposed to radiation, which causes damage or stress to the device, these ITCs begin to form at the semiconductor-oxide interface [22]–[23]. The electric field at the tunnelling junction is impacted by the presence of these trap charges at the interface. The electric field determines the TFET's tunnelling probability, and it is extremely sensitive to changes in the electric field.

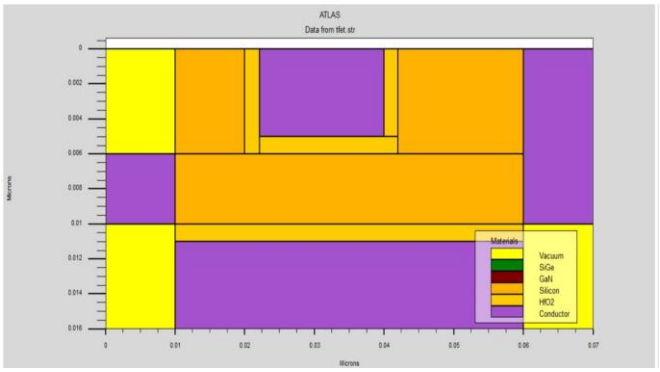
The electric field at the junction is, however, diminished by the addition of the interface trap charges to the channel. ITCs lower device reliability and performance as a result. Positive (donor) and negative (acceptor) ITCs are two categories that can be used to separate the trap charges.Positive ITCs are found above the valance band while negative ITCs are found below the conduction band, according to the energy band diagram [24].

Numerous researchers have looked into how ITCs affect different types of structures, yet the analog/RF and linearity performances show significant diversity among ITCs. Additionally, although to a limited extent, the issue of ambipolarity has been addressed in hetero TFET [25]. Furthermore, hetero TFETs have been discovered to be less dependable in the presence of various ITCs due to reduced electrostatic coupling [26].

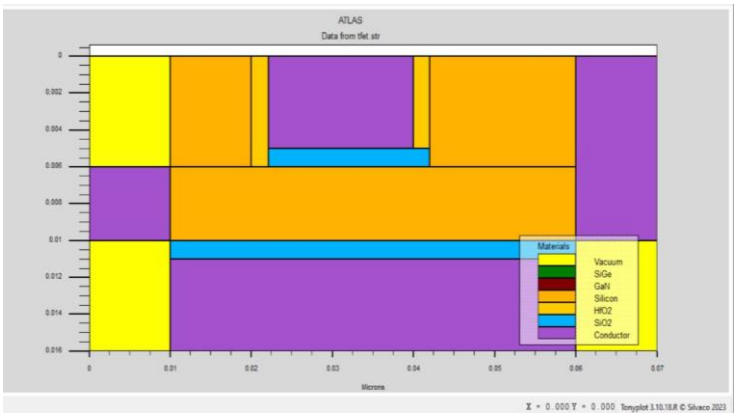
Therefore, the impact of various ITCs on the dual-material gate-oxide stack double-gate TFET has been published for the first time and contrasted with the traditional dual

## III. DEVICE STRUCTURE OF PROPOSED AND CONVENTIONAL TFET

### a) Proposed TFET Device Structure




### b) Conventional TFET Device Structure




The structure of the research paper consists of specific materials and dimensions. The source region with SiGe, measuring 10nm , drain region with GaN measuring 10nm and serve as the electrodes for injecting and collecting charge carriers. The channel region, with an 50nm length, and second channel with 10nm and third with 18nm is composed of silicon (Si) and acts as the semiconductor material responsible for the flow of charge carriers between the source and drain regions.

For control and modulation of the charge carrier flow, the TFET includes two gates. The first gate, called "Gate 1," is made of HfO2 Hafnium oxide and has a width of 18nm. It acts as one of the control electrodes. The second gate, known as "Gate 2," is made of HfO2 and also has a width of 50nm. It works in conjunction with gate 1 to further manipulate the flow of charge carriers in the channel region.

To ensure insulation and optimize the gate-channel interface, an oxide layer of hafnium dioxide (HfO2) with a thickness of 1nm is present and other oxide layer is 6nm, This oxide layer serves as a dielectric material, reducing leakage currents and enhancing the control of charge carrier flow.

The source was doped with p-type at a concentration of 6x10^22 cm^-3, while the drain was doped with n-type at a concentration of 5x10^18 cm^-3.
Table 1 represents the device parameters used for the simulation.

advanced device modeling capabilities, enabling researchers to accurately represent the intricate structure and physical behavior of TFETs [12].
It allows for the creation of detailed device models incorporating specific material properties, dimensions, and doping

| **Design parameters** | **Value** |
|---|---|
| Gate1 length ($L_{G1}$) nm | 18 |
| Gate2 length ($L_{G1}$) nm | 50 |
| Drain length ($L_D$) nm | 10 |
| Source length ($L_S$) nm | 10 |
| Thickness of the oxide, ($T_{ox}$) nm | 6 |
| Drain doping, N-Type, $cm^{-3}$ | $5\times 10^{18}$ |
| Source doping, P-type, $cm^{-3}$ | $6\times 10^{22}$ |

This paper is organised in three sections.
Section III describes the device structure and simulation parameters.

In Section IV, simulation results are investigated in three parts.
First part part deals with the linearity figures

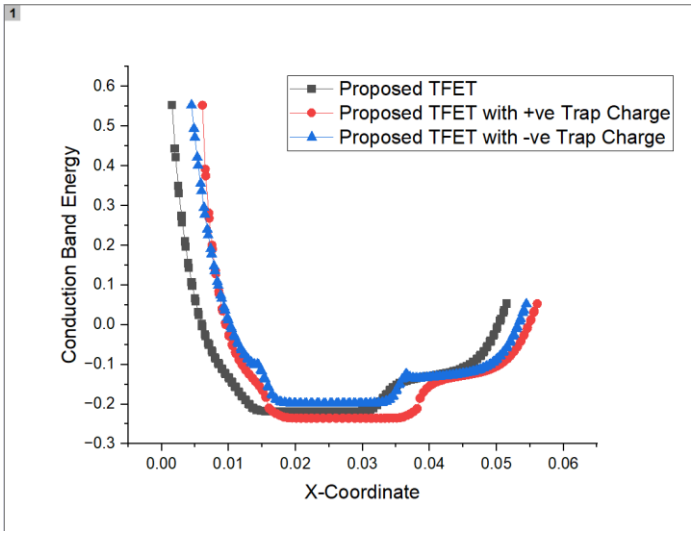
second part involves includes DC analysis, ana log/RF performance

Section IV,concludes this paper

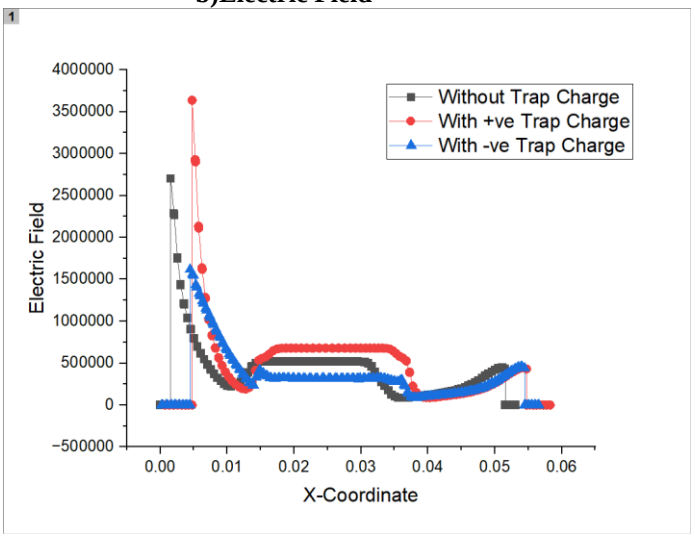
**SECTION-IV: simulation results are investigated in three parts.**
**First part part deals with the linearity figures:**

**PROPOSED TFET DEVICE:**

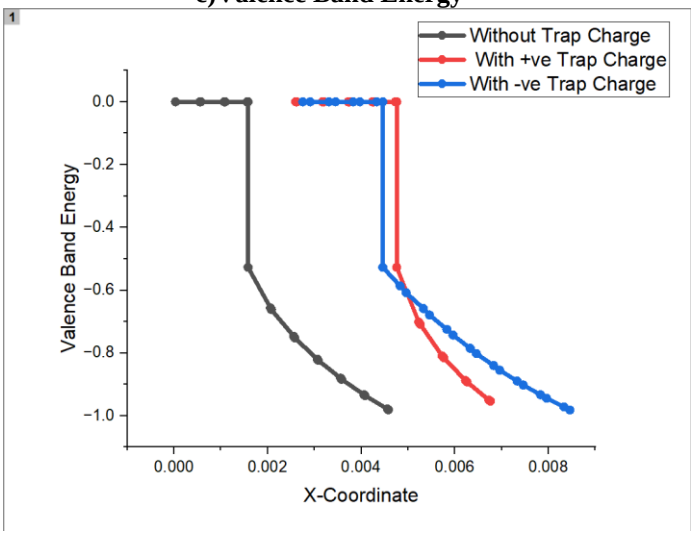
**a)Conduction Band Energy**




**b)Electric Field**

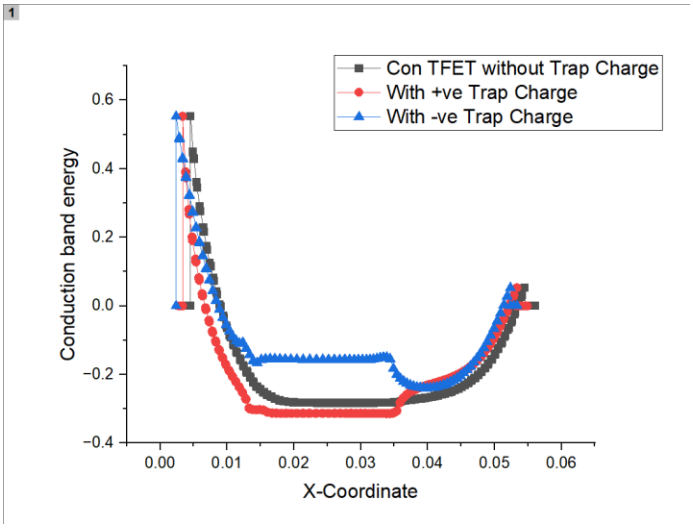



**c)Valence Band Energy**

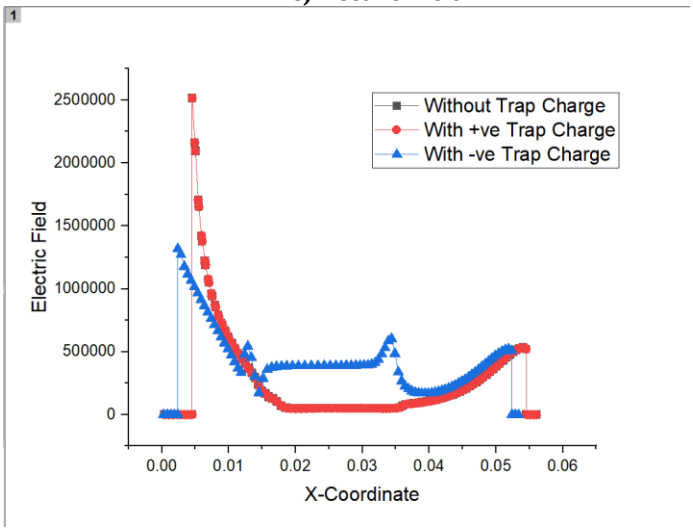



**CONVENTIONAL TFET DEVICE:**

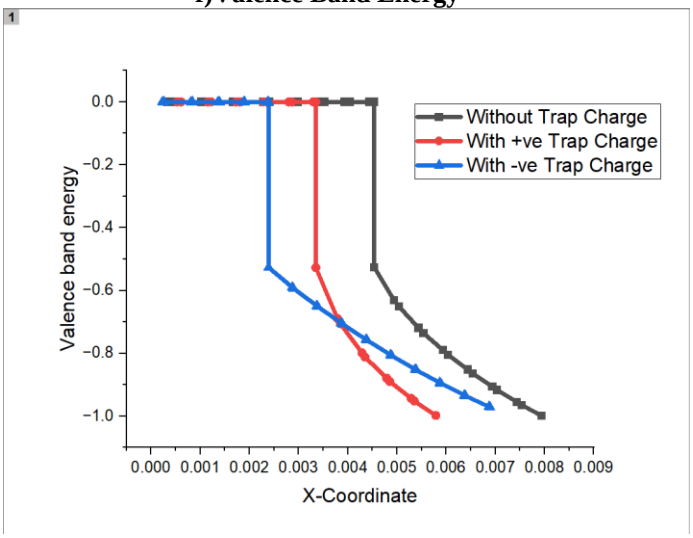
**d)Conduction Band Energy**




**e)Electric Field**




**f)Valence Band Energy**



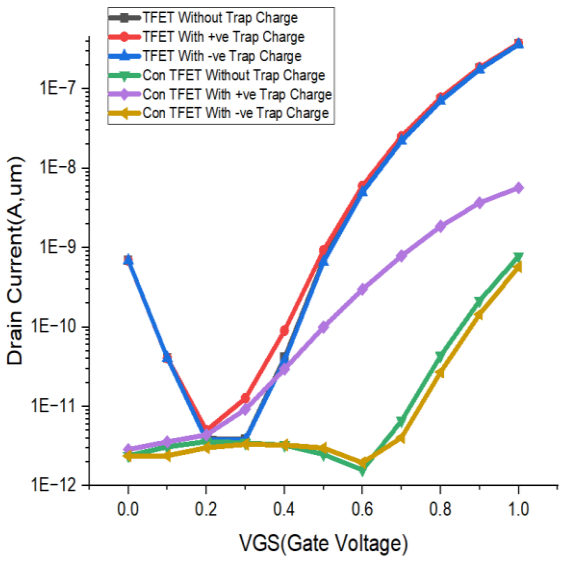
because use of the high-k dielectric (HfO2), which provides better capacitive coupling at source-channel interface [8]. This figure also demonstrates the smaller variation in ID−Vgs characteristics in case of Proposed -TFET as compared to the conventional-TFET for different ITCs. The decrease (increase) in ON-state current (ION) is found with negative ITCs (positive ITCs) for both the devices.

A comparative analysis of DC parameters for the conventional-TFET and proposed-TFET is shown in above figures, it has also been noticed that the leakage current in the case of negative ITCs is higher as compared to positive ITCs for both the devices. Furthermore, Fig. (a) and (d) presents the variations of comduction band energy for both proposed-TFET and conventional-TFET. From this figure it can be stated that, conventional-TFET presents the larger variations in the threshold voltage for different interface trap charge densities as compared to proposed-TFET. Fig. (b) and (e) shows the variation of electric field From this figure it can be observed that proposed-TFET is less affected by positive and negative interface trap charges as compared to the conventional-TFET. Fig. (c) and (f) shows the variation of valence band From this figure it can be observed that proposed-TFET is less affected by positive and negative interface trap charges as compared to the conventional-TFET. From all aforementioned analysis, it can be stated that proposed-TFET is less susceptible to positive and negative interface trap charges as compared to the conventional-TFET

**Second part:**

DC analysis performance

a) Variation of ID versus Vgs characteristics for conventional-TFET and proposed-TFET in the presence of different trap charges




The variation of ID (drain current) versus Vgs (gate-to-source voltage) characteristics is an important aspect to consider when studying the performance of Tunnel Field-Effect Transistors (TFETs). In the presence of different trap charges, the behavior of TFETs can differ significantly.

Comparing the conventional-TFET and proposed-TFET, it has been observed that the proposed-TFET exhibits less variation in its ID versus Vgs characteristics when subjected to different trap charges. On the other hand, the conventional-TFET shows a greater degree of variation, particularly when subjected to positive trap charges compared to negative trap charges.

This difference in behavior can be attributed to the design and structure of the proposed-TFET. It is likely that the proposed-TFET incorporates features or modifications that help mitigate the impact of trap charges, resulting in more consistent performance across different gate-to-source voltage levels.

Understanding the impact of trap charges on TFET performance is crucial for optimizing device design and enhancing device reliability. By studying the variation in ID versus Vgs characteristics, researchers and engineers can gain insights into the behavior of TFETs under different operating conditions, leading to improvements in their performance and overall functionality.

## V.CONCLUSION

The research paper titled "Analysis of Trap Charges for TFET Device" focuses on investigating the impact of trap charges on Tunnel Field-Effect Transistor (TFET) devices. After analyzing and studying the behavior of TFETs in the presence of trap charges, the following conclusions can be drawn:

Trap Charges Influence TFET Performance: The presence of trap charges significantly affects the performance of TFET devices. Trap charges can introduce additional states within the device, altering its electrical characteristics and behavior.

Positive Trap Charges vs. Negative Trap Charges: The analysis reveals that TFET devices are more sensitive to positive trap charges compared to negative trap charges. Positive trap charges lead to greater variation in the device's ID versus Vgs characteristics, potentially affecting its overall performance.

Proposed-TFET Shows Improved Stability: A comparison between conventional-TFET and proposed-TFET indicates that the proposed-TFET design exhibits improved stability in the presence of trap charges. The proposed design minimizes the variation in ID versus Vgs characteristics, suggesting better reliability and consistent performance across different gate-to-source voltage levels.

Device Optimization Strategies: The research highlights the importance of understanding trap charges and their impact on TFET performance. It suggests that device optimization strategies should be implemented to mitigate the effects of trap charges and enhance overall device reliability.

In conclusion, this research paper provides valuable insights into the analysis of trap charges for TFET devices. The findings emphasize the need for further exploration and optimization of TFET designs to reduce the influence of trap charges, ultimately leading to improved device performance and reliability.

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