# Performance Evaluation of Hybrid Full Adder in Multistage Arithmetic Circuits across 90nm and 180nm CMOS Technologies

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# 1. ABSTRACT

**This work presents a comprehensive performance analysis of a Hybrid Full Adder (TFA) design across 90-nm and 180-nm CMOS technology nodes. The TFA circuit is first characterized in terms of delay and average power consumption in the single-stage configuration. Subsequently, the TFA is utilized to construct two important multistage arithmetic circuits, a 4-bit Ripple Carry Adder (RCA) and a 6:2 Compressor. The delay and power characteristics of these multistage circuits are also evaluated and compared across the 90nm and 180nm technology nodes. Finally, a comparative analysis is performed between the 4-bit RCA and 6:2 Compressor to understand the tradeoffs in using these different arithmetic building blocks in larger system designs. The results provide valuable insights into the performance scaling and suitability of the hybrid TFA design for implementing efficient multistage arithmetic circuits in scaled CMOS technologies.**

**Key words: Hybrid TFA, 4-bit RCA, 6:2 compressor, Multistage circuits.**

# 2. INTRODUCTION

Full adders are the fundamental building blocks for a wide range of arithmetic circuits, from simple controllers to complex processors [1]. In recent years, there has been a growing interest in exploring hybrid logic style full adders, which offer advantages over conventional CMOS (C-CMOS) full adders in terms of speed, power consumption, and energy efficiency [2][3]. One such hybrid full adder design is the transmission function adder (TFA), which combines the strengths of different logic styles to achieve improved performance [4].

In this work, we present a comprehensive performance evaluation of the Transistor Function Full Adder (TFA) design across two different CMOS technology nodes - 90nm and 180nm. Specifically, we have characterized the TFA circuit in terms of delay and average power consumption in the single-stage configuration for both the 90nm and 180nm technology nodes. Additionally, we have implemented and evaluated two important multistage arithmetic circuits using the TFA design - a 4-bit Ripple Carry Adder (RCA) and a 6:2 Compressor, comparing their delay and power performance across the 90nm and 180nm technology nodes. Furthermore, we have conducted a comparative analysis between the 4-bit RCA and 6:2 Compressor to understand the trade-offs in using these different multistage arithmetic circuits. This paper presents a comprehensive performance evaluation of the TFA design in the two technology

nodes, including the characterization of the TFA circuit in the single-stage configuration, the implementation and evaluation of the 4-bit RCA and 6:2 Compressor circuits, and a comparative analysis between these multistage arithmetic circuits.

Furthermore, at the gate level, the most popular circuits with hybrid structure are two- and three-input XOR and XNOR circuits, which are also the core of full adders. This work adopts the same gate-level structure for TFA as proposed in the authors' previous work [1]. This ensures that the performance evaluation conducted in this paper is directly comparable to the timing behaviour analysis and modelling techniques established in the foundational paper.

## 2.1. LITERATURE REVIEW

*Hareesh-Reddy Basireddy, Karthikeya Challa, and Tooraj Nikoubin* introduces a groundbreaking approach to address the challenges of timing analysis and optimization in hybrid logic circuits. Traditional logical effort methods, designed for CMOS circuits, fall short in accurately predicting the behavior of these complex structures. To bridge this gap, the authors propose a novel metric named "hybrid logical effort," which incorporates parameters like gain and selection factor to characterize the unique properties of hybrid logic cells. By modeling hybrid logic circuits as networks of these characterized cells, the method enables precise prediction of circuit performance. This breakthrough empowers designers to optimize hybrid logic circuits for speed and power efficiency, leading to significant improvements in the design of high-performance digital systems. The research not only enhances design efficiency and predictability but also opens up new avenues for exploring innovative hybrid logic circuit architectures.

*Goel, Kumar, and Bayoumi* present a novel approach to designing full adders for deep-submicrometer technology, focusing on achieving both robustness and energy efficiency. Their proposed design employs a hybrid CMOS logic style, centered around an XOR-XNOR circuit that simultaneously generates both XOR and XNOR outputs. This innovative architecture offers significant advantages in terms of speed, power consumption, and driving capability when compared to traditional full adder designs. By effectively combining different logic styles, the authors create a full adder that demonstrates superior resilience to process variations and noise, making it an ideal choice for demanding applications in the deep-submicrometer domain.

*K.Navi, O. Kavehei, M. Rouholamini, A. Sahafi, S. Mehrabi, and N. Dadkhahi*,research introduces a novel approach to designing low-power, high-performance 1-bit CMOS full adder cells. The core innovation lies in a unique

architectural style termed "Bridge," which incorporates bridge transistors to enhance circuit structure and efficiency. By optimizing transistor placement and connections, the "Bridge" design achieves significant reductions in power consumption and delay compared to traditional full adder implementations. The researchers conducted thorough simulations using HSPICE in a 90nm CMOS process to validate the performance advantages of their proposed design. These findings contribute to the ongoing pursuit of energy-efficient digital circuits by providing a promising building block for low-power applications.

*P. Bhattacharyya, B. Kundu, S. Ghosh, V. Kumar, and A. Dandapat* present a comprehensive analysis of a low-power, high-speed hybrid 1-bit full adder circuit. The proposed design effectively combines CMOS and transmission gate logic to achieve significant improvements in power consumption and speed compared to conventional full adder implementations. By carefully integrating these logic styles, the authors optimize the circuit's performance metrics. The paper provides detailed performance evaluations, including power, delay, and transistor count, across different technology nodes. The results demonstrate the effectiveness of the hybrid approach in addressing the design challenges of modern high-performance digital circuits.

*Kandpal and Tomar* introduce a novel high-performance 20-transistor hybrid full adder circuit. The cornerstone of their design is a new XOR/XNOR architecture that effectively combines different logic styles to achieve a compact and efficient implementation. By strategically integrating CMOS and pass-transistor logic, the authors optimize the circuit for speed, power consumption, and area. The proposed full adder outperforms existing designs in these critical performance metrics, demonstrating the potential of hybrid logic in creating high-performance arithmetic circuits. The research contributes significantly to the ongoing development of low-power, high-speed digital systems by providing a promising building block for future applications.

*Rajagopal and Chakrapani* present a novel high-performance hybrid full adder circuit tailored for VLSI applications. The proposed design effectively combines CMOS and pass-transistor logic to achieve a balance between speed, power consumption, and area. By carefully optimizing the circuit architecture, the authors enhance critical path performance and reduce power dissipation. The paper provides a detailed analysis of the proposed full adder, including comparisons with existing designs. The results demonstrate the superiority of the hybrid approach in terms of performance metrics, making it a promising candidate for integration into high-performance digital systems.

## 3. METHODOLOGY

The Transmission Function Adder (TFA) [Fig – 1] is a hybrid full adder design that integrates transmission gates, pass transistors, and conventional CMOS logic to enhance performance across various metrics such as speed, power consumption, and reliability. The design leverages the strengths of these different logic styles to optimize the adder's overall efficiency and effectiveness. Transmission gates are employed in the TFA for their efficient switching capabilities, facilitating rapid signal transitions and contributing to reduced delay. Pass transistors are used to minimize the transistor count and power consumption, further enhancing the adder's performance by reducing the overall power dissipation. Conventional CMOS logic is incorporated to provide robustness and ensure reliable operation, thus balancing the innovative aspects of the hybrid design with the proven stability of traditional CMOS technology.

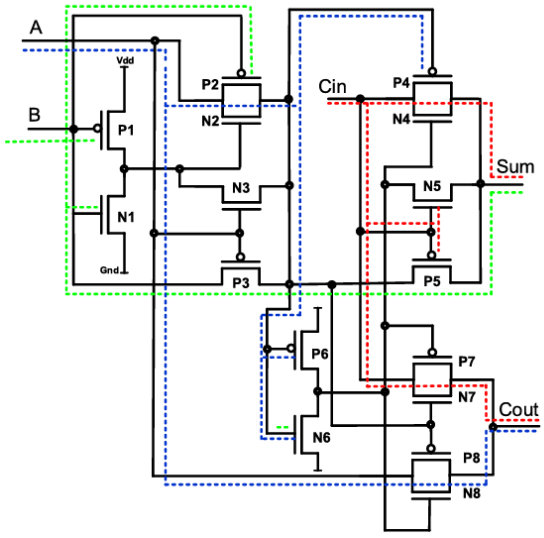


Figure 1: Circuit diagram for TFA

In designing the TFA, careful consideration is given to the trade-offs between speed, power consumption, and area. The integration of transmission gates helps to achieve fast switching times and minimal propagation delay, while the use of pass transistors helps to lower power consumption by reducing the number of transistors required. The design is optimized to strike a balance between these factors, ensuring that the TFA performs efficiently across different metrics while maintaining a compact area footprint. The gate-level structure of the TFA is meticulously designed to ensure efficient signal propagation and minimal power dissipation, contributing to the overall performance advantages of the adder.

The TFA is implemented in both 90nm and 180nm CMOS technology nodes, each requiring precise scaling of the fundamental components—transmission gates, pass transistors, and inverters. In the 90nm node, the TFA is designed to

take advantage of the smaller feature sizes and increased density, allowing for enhanced performance while maintaining the adder's efficiency. Similarly, in the 180nm node, the design ensures that the TFA's performance characteristics are preserved despite the larger feature sizes. This scalability ensures that the TFA can be adapted to various technology nodes without compromising its performance.

Performance characterization of the TFA involves analyzing both delay and power consumption. The delay performance is assessed to ensure that the adder meets required speed specifications, focusing on minimizing the time taken for a signal to propagate through the circuit. Additionally, the average power consumption is measured to evaluate the adder's efficiency, with the hybrid design aiming to reduce power dissipation compared to traditional full adder designs.

The TFA's design also emphasizes scalability and flexibility, making it suitable for a wide range of applications. The hybrid approach allows for adjustments and optimizations to meet specific performance needs, whether in simple controllers or complex processors. This adaptability ensures that the TFA remains a versatile and valuable component in digital design, capable of addressing diverse system requirements and contributing to high-performance arithmetic circuits in modern CMOS technologies.

In conclusion, the Transmission Function Adder (TFA) represents a significant advancement in full adder design by combining multiple logic styles to achieve superior performance. Its implementation in both 90nm and 180nm technology nodes demonstrates its versatility and ability to adapt to different technological scales. By effectively balancing speed, power consumption, and area, the TFA offers a high-performance solution for a broad spectrum of applications in contemporary digital systems.

**90nm technology:**

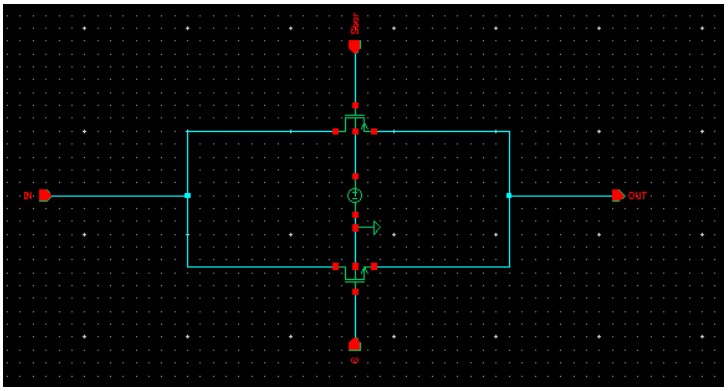


Figure 2: Transmission gate implemented in 90nm technology

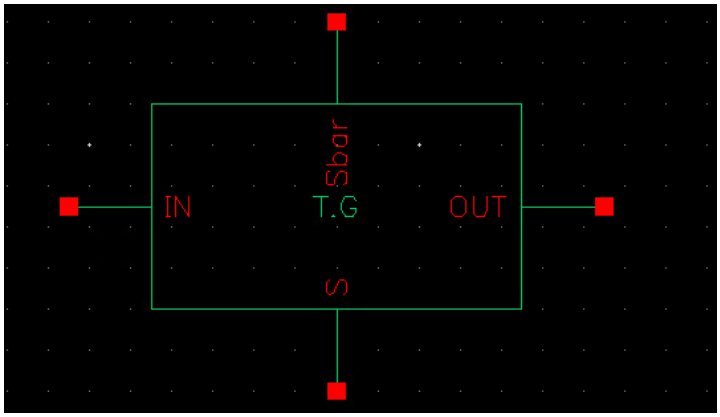


Figure 3: Symbol for Transmission gate in 90nm technology

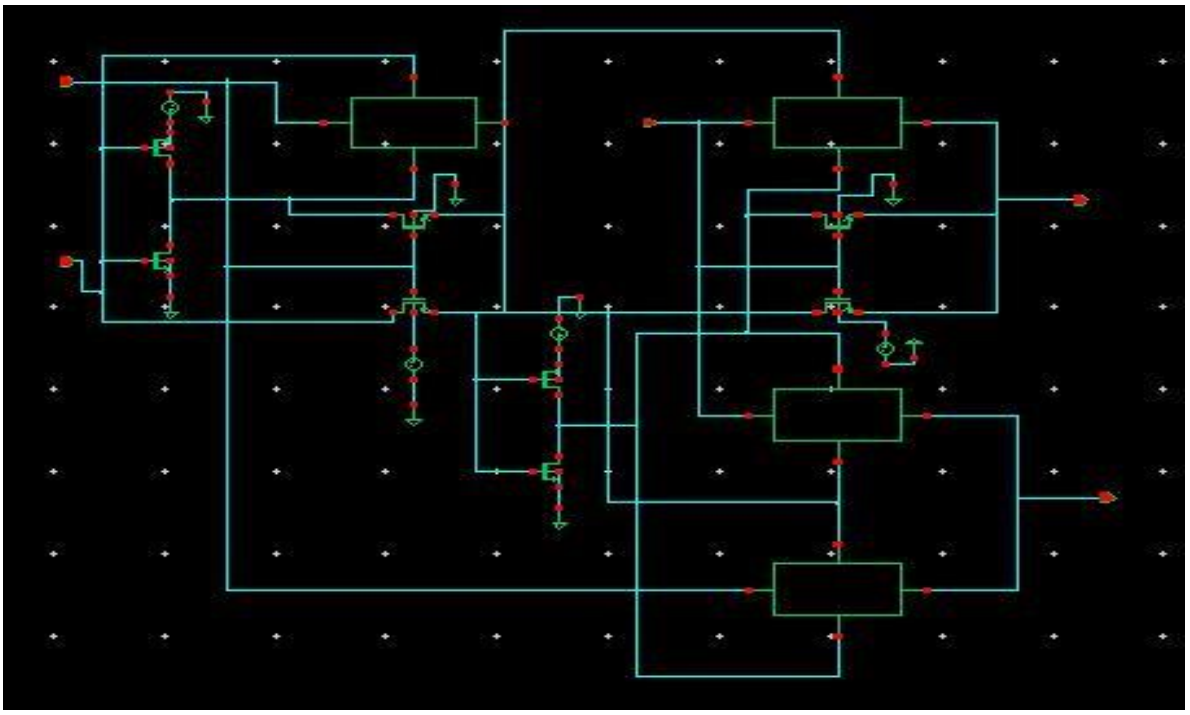

Figure 4: TFA is implemented in 90 nm

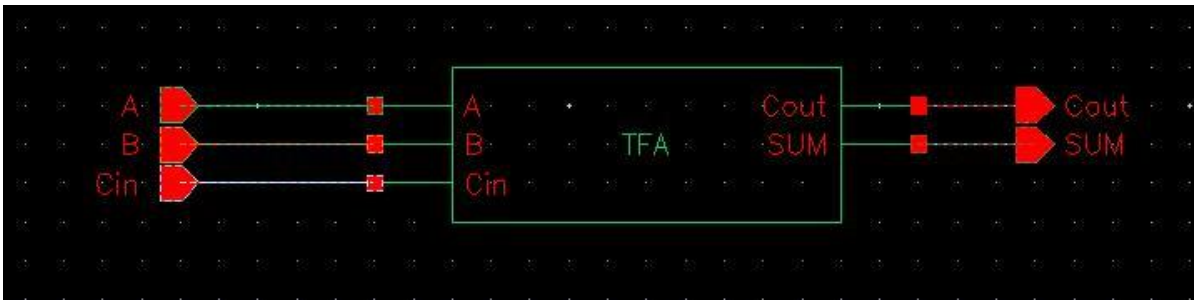


Figure 5: Symbol for TFA in 90nm

## 180nm technology:

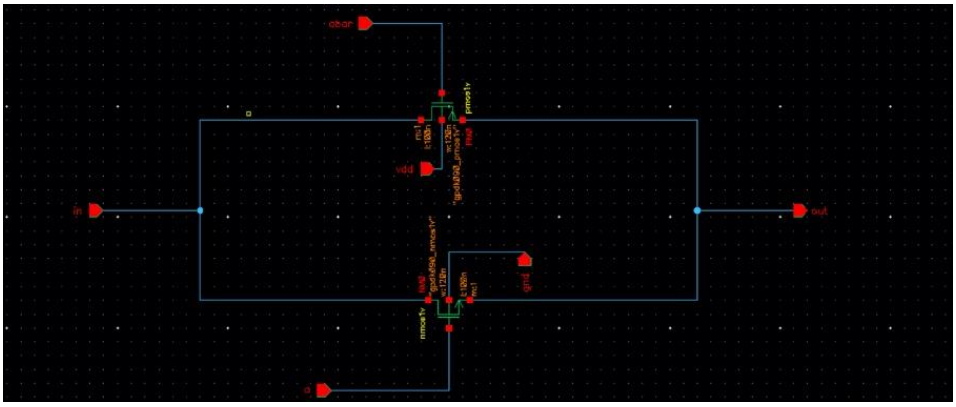


Figure 6: Transmission gate implemented in 180nm technology

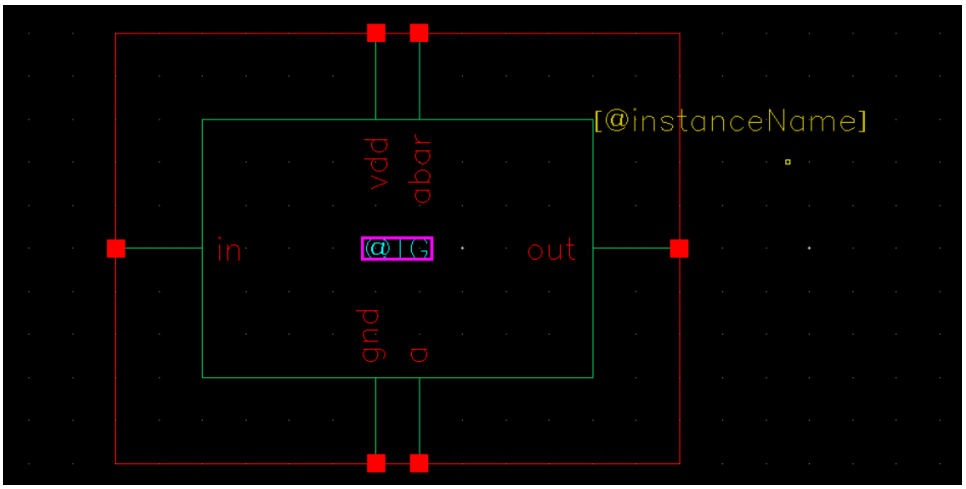


Figure 7: Symbol for Transmission gate in 180nm technology

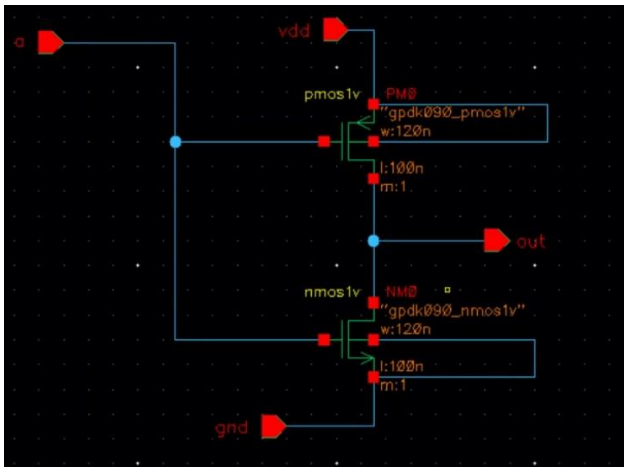


Figure 8: Inverter implemented in 180nm technology

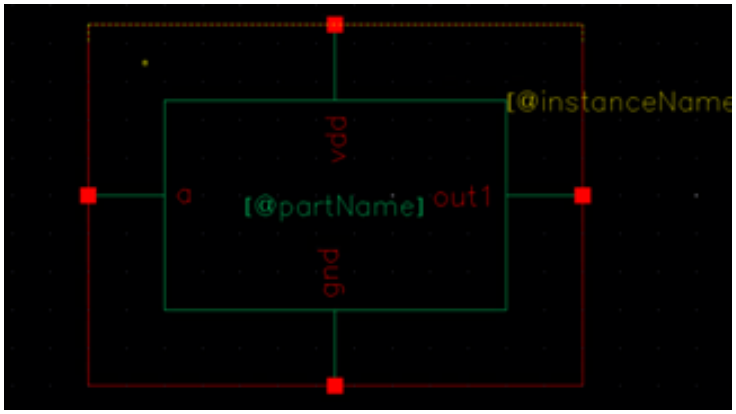


Figure 9: Symbol for inverter in 180 nm technology

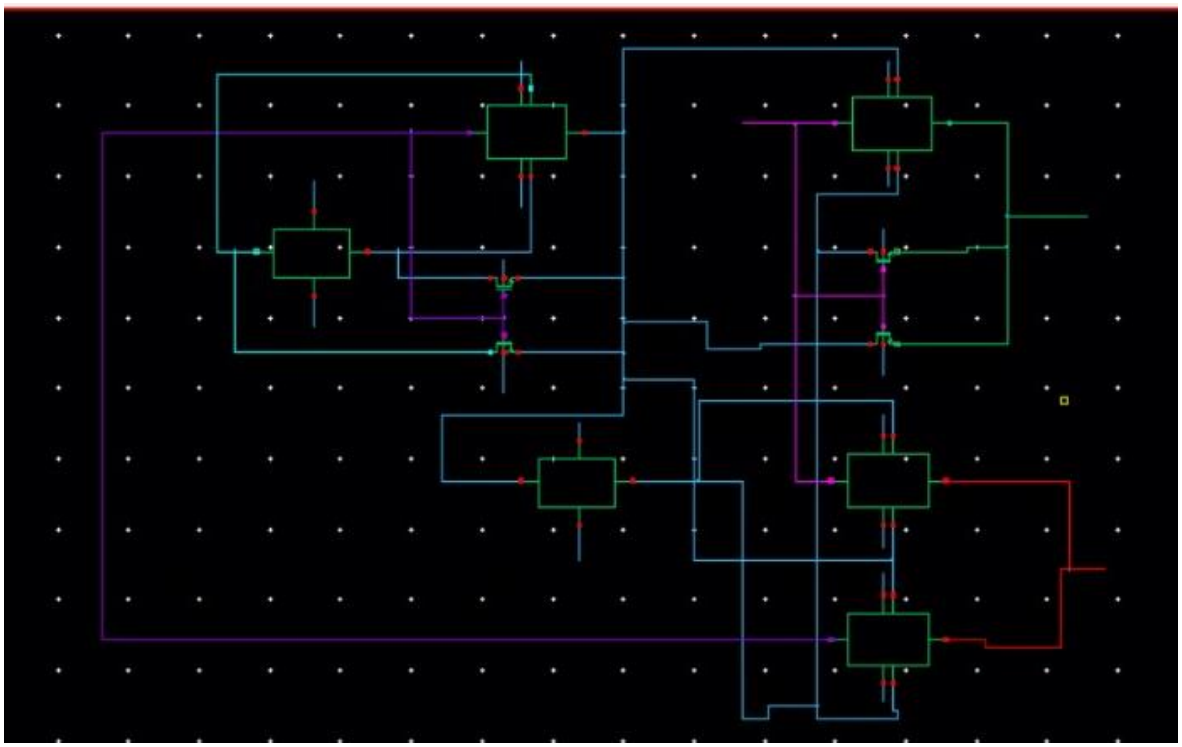

Figure 10: TFA is implemented in 180 nm

## 3.1. Implementation of Multistage Arithmetic Circuits

The TFA design is utilized to implement two important multistage arithmetic circuits: a 4-bit Ripple Carry Adder (RCA) and a 6:2 Compressor. The 4-bit RCA is a fundamental arithmetic circuit used for binary addition, while the 6:2 Compressor is a more complex circuit used for partial product reduction in multipliers. Both circuits are implemented using the TFA design and evaluated in terms of their delay and power consumption across the 90nm and 180nm technology nodes. The implementation process involves designing the circuits at the gate level and simulating their performance under various operating conditions.

The 4-bit RCA is implemented using a series of TFA cells, with each cell performing a single-bit addition. The carry-out from each cell is propagated to the next cell, resulting in a ripple carry effect. The performance of the 4-bit RCA is evaluated in terms of its delay and power consumption, providing insights into the efficiency of the TFA design for implementing basic arithmetic circuits. The results highlight the advantages of using the TFA design for constructing efficient and high-performance RCAs, making it a suitable choice for various applications.

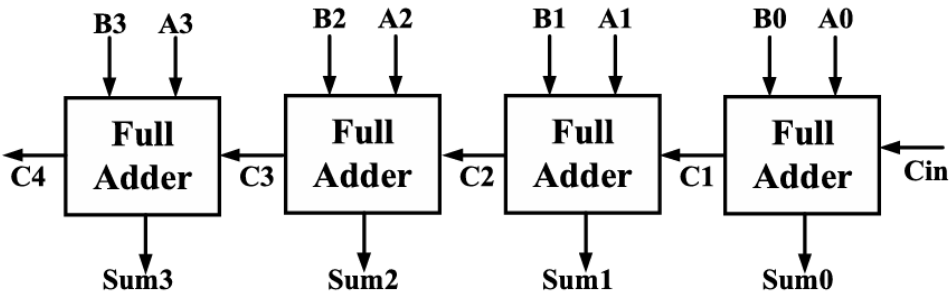


Figure 11: 4-bit Ripple carry adder

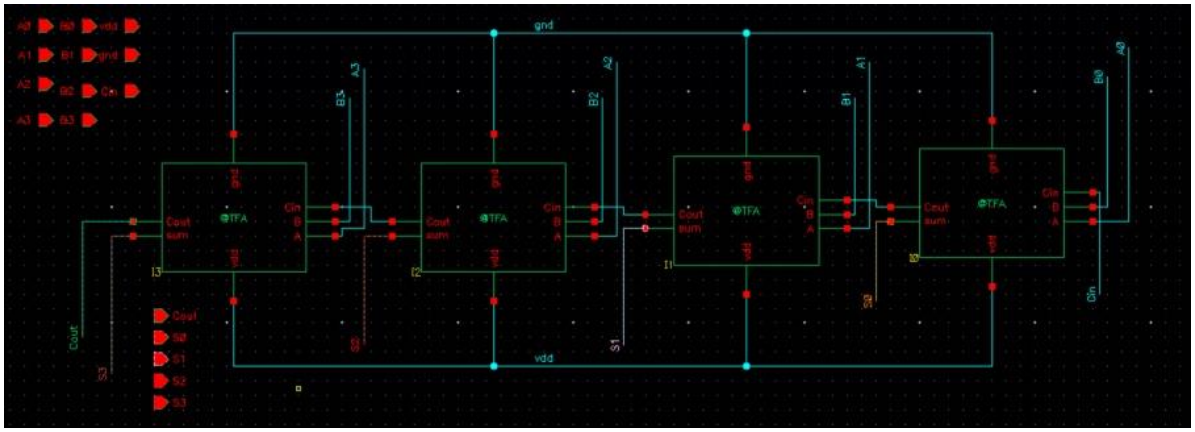

Figure 12: 4-bit RCA implemented in 180nm technology

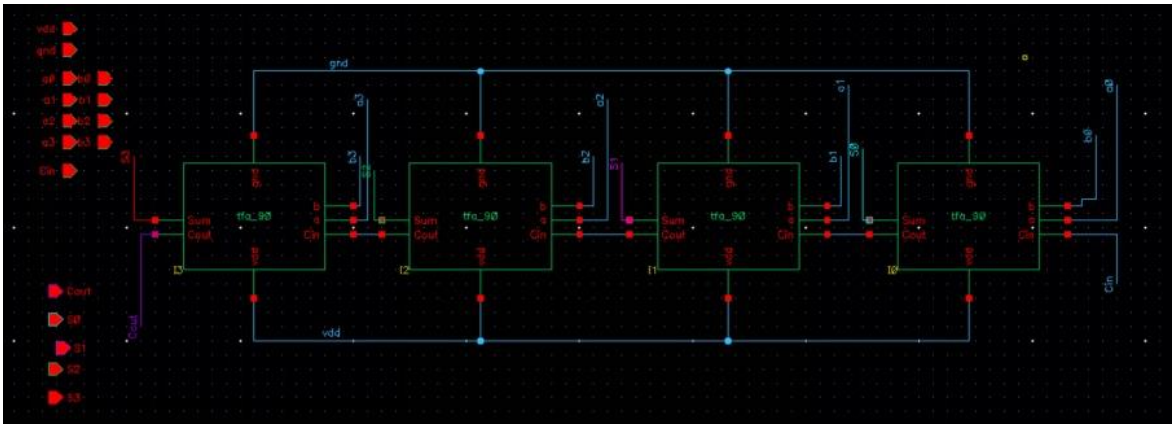

Figure 13: 4-bit RCA implemented in 90nm technology

The 6:2 Compressor is a more complex circuit used for partial product reduction in multipliers. It is implemented using a combination of TFA cells and other logic gates to achieve the desired functionality. The performance of the 6:2 Compressor is evaluated in terms of its delay and power consumption, providing insights into the efficiency of the TFA design for implementing complex arithmetic circuits. The results highlight the advantages of using the TFA design for constructing efficient and high-performance compressors, making it a valuable solution for various applications.

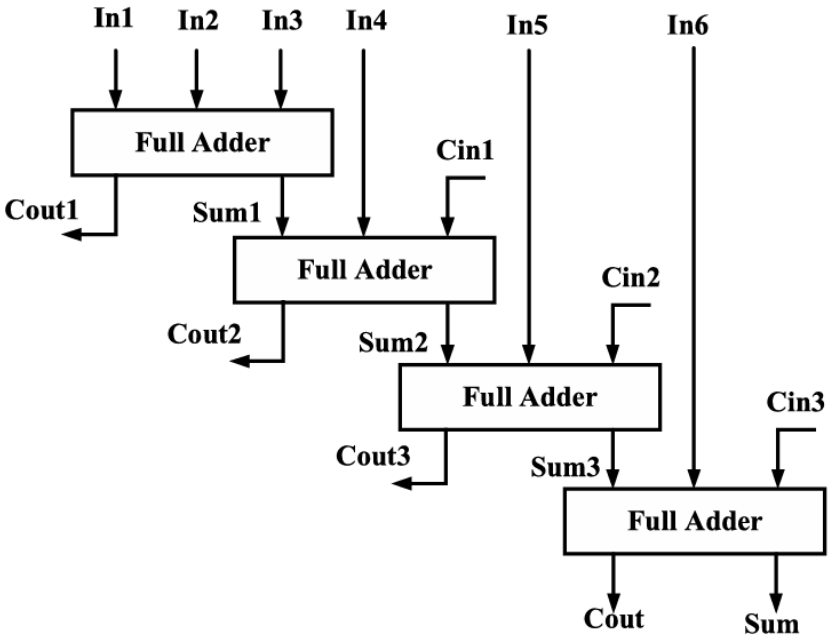


Figure 14: 6:2 Compressor

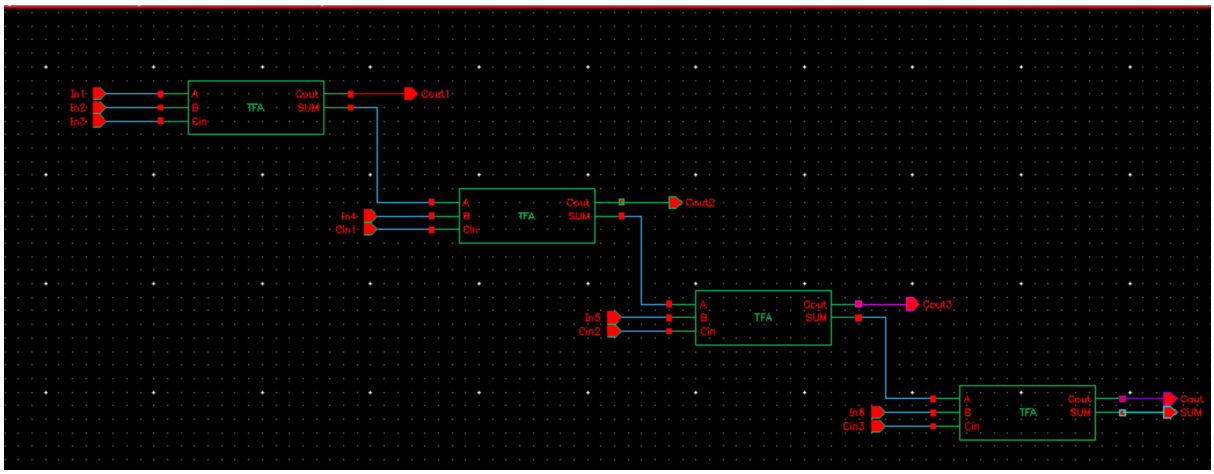

Figure 15: 6:2 compressor implemented in 180nm technology

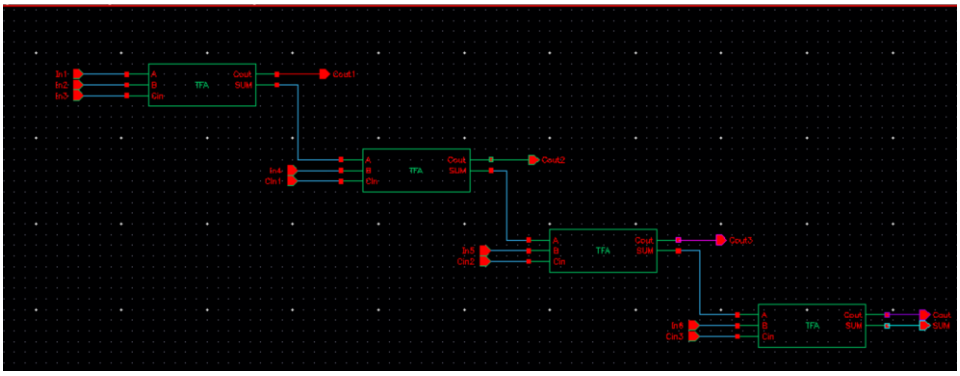


Figure 16: 6:2 compressor implemented in 90nm technology

The comparative analysis between the 4-bit RCA and the 6:2 Compressor provides valuable insights into the trade-offs involved in using different arithmetic building blocks in larger system designs. The performance metrics of both circuits highlight their strengths and weaknesses, providing a basis for making informed design choices. The results of this analysis contribute to the ongoing efforts to develop efficient and high-performance arithmetic circuits for advanced digital systems, making the TFA design a valuable addition to the toolkit of digital designers.

## 3.2. Layout Design Considerations for Hybrid Full Adder

This section delves into the layout design aspects crucial for the efficient implementation of the Hybrid Full Adder (TFA) across different technology nodes, with a primary focus on 90nm and 180nm CMOS technologies. The layout design of any CMOS circuit significantly influences its performance parameters, including speed, power consumption, and area. For the Hybrid Full Adder, essential principles include minimizing parasitic effects through careful placement and routing, optimal transistor sizing to balance speed and power consumption, and designing symmetric layouts for critical paths to ensure uniform performance and reduce mismatch errors.

At 90nm, challenges like increased leakage currents and variability necessitate techniques focusing on leakage reduction using high-threshold voltage (HVT) devices, dense layouts to reduce interconnect lengths and associated delays, and advanced design rule checking for manufacturability and reliability. For the 180nm node, the primary challenges revolve around optimizing performance while managing power dissipation, requiring wider metal tracks to reduce resistance, well-isolated regions to minimize noise coupling, and a standard cell layout approach for consistency and ease of design modifications.

Layout optimization techniques are vital for reducing interconnect delays through strategic layer utilization and via optimization. Implementing robust power distribution networks with grid-based designs and strategically placing decoupling capacitors can mitigate voltage fluctuations and noise. A balanced clock tree design is essential to ensure minimal skew and optimal performance, with judicious use of clock buffers to drive the clock signal efficiently across the chip.

Design for manufacturability (DFM) considerations include ensuring lithography-friendly design practices to avoid issues during manufacturing and designing with chemical-mechanical planarization (CMP) in mind to achieve a flat and uniform surface necessary for subsequent lithographic steps. Simulation and verification processes are indispensable, with Layout vs. Schematic (LVS) checks ensuring the layout accurately reflects the schematic design, post-layout simulations verifying the design meets performance specifications under real-world conditions, and parasitic extraction to assess the impact of parasitics on circuit performance. By adhering to these principles and techniques, designers can achieve a balance between speed, power consumption, and area, ensuring the Hybrid Full Adder meets the desired specifications and performance targets. These detailed considerations for 90nm and 180nm technology nodes provide a roadmap for addressing the unique challenges presented by each technology, facilitating the creation of robust and efficient arithmetic circuits.

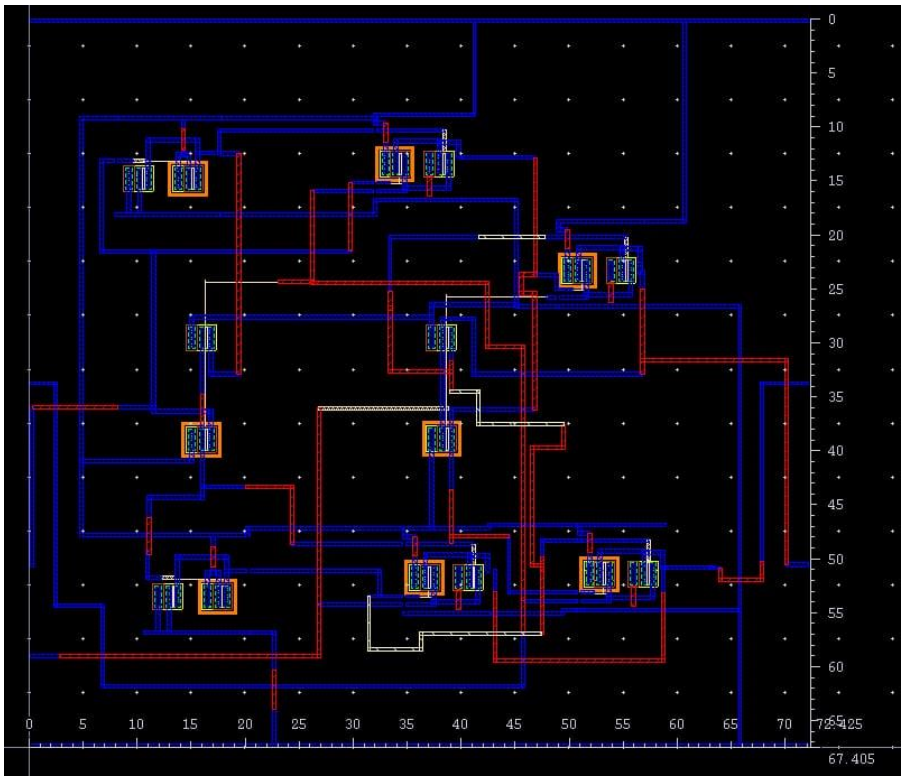


Figure 17: Layout design for TFA in 180nm

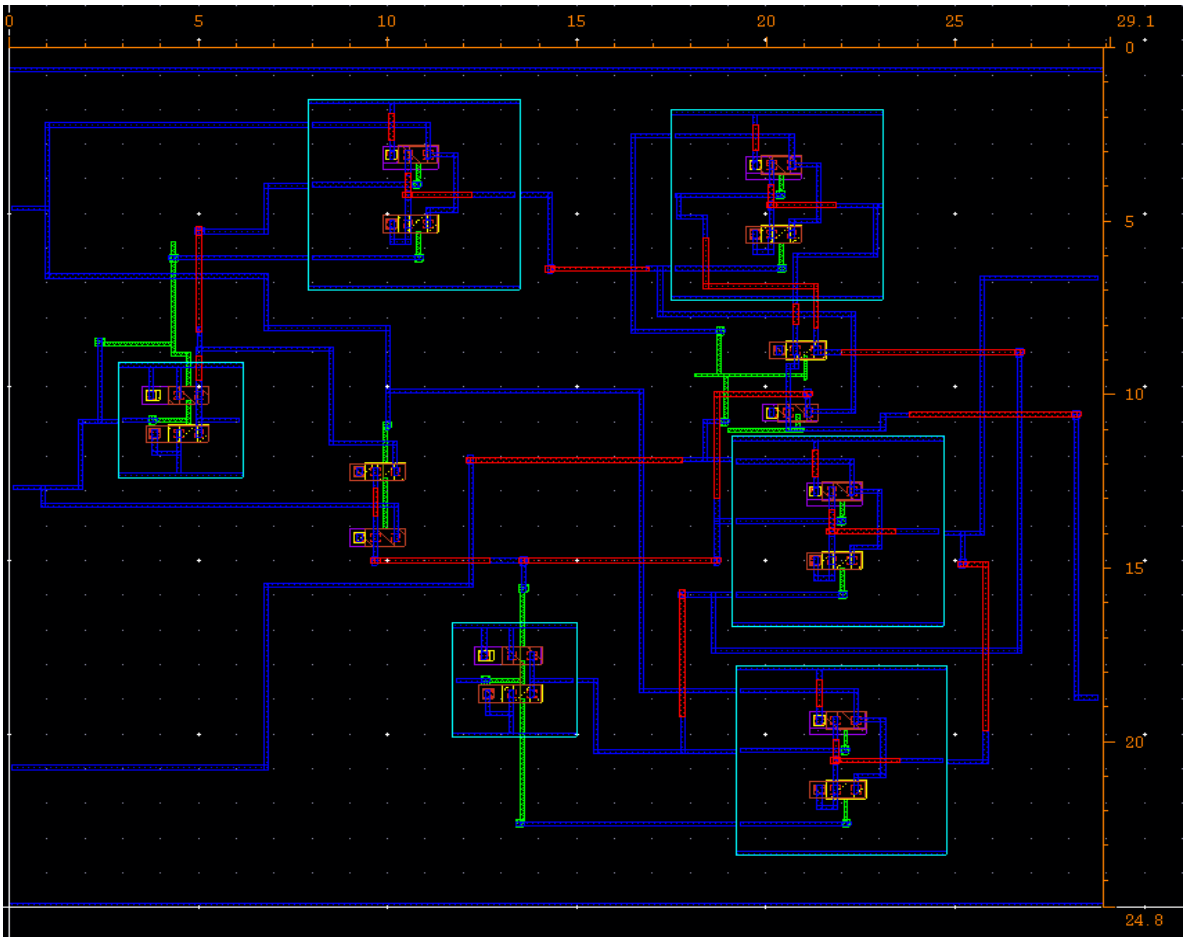


Figure 18: Layout design for TFA in 90nm

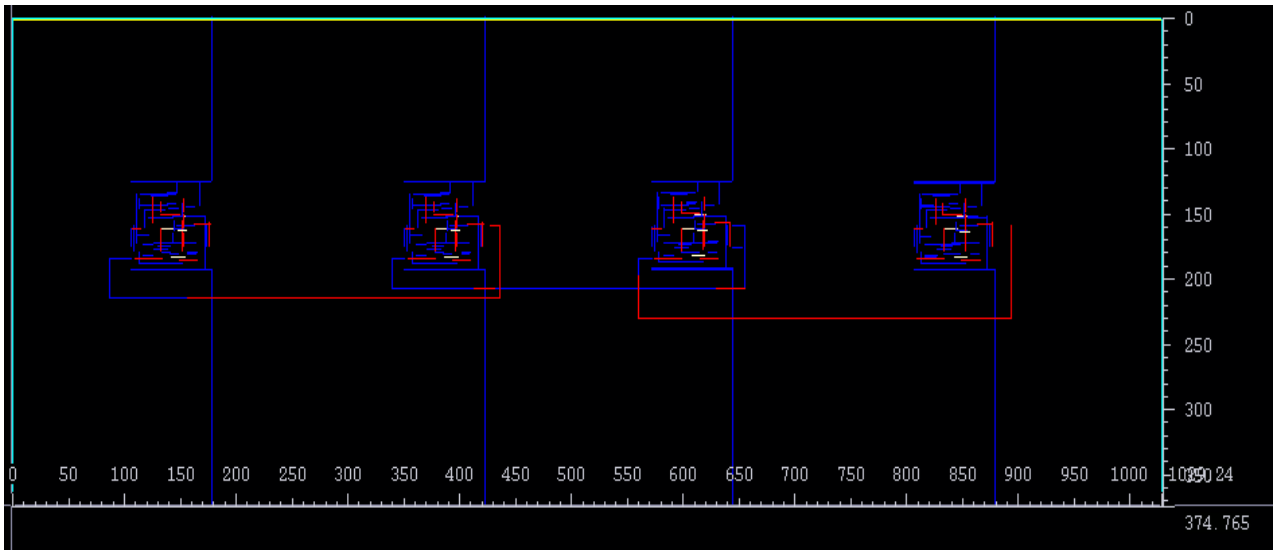


Figure-19: Layout design for 4bit RCA in 180nm technology

# 4. RESULT

The performance characterization of the TFA circuit in single-stage configurations involves evaluating its delay and average power consumption for both 90nm and 180nm CMOS technology nodes. Delay is a critical performance metric that determines the speed at which the circuit can operate, while average power consumption is an important consideration for energy efficiency. The characterization process involves simulating the TFA circuit under various operating conditions and measuring its performance metrics to provide a comprehensive understanding of its efficiency.

For the 90nm technology node, the TFA circuit is evaluated in terms of its delay and power consumption under different supply voltages and operating frequencies. The results of these simulations provide insights into the impact of technology scaling on the performance of the TFA design. The 90nm technology node offers higher performance and lower power consumption compared to the 180nm node, making it a suitable choice for high-performance applications. The characterization results highlight the advantages of using the TFA design in advanced CMOS technologies, where performance and power efficiency are critical considerations.

Similarly, the performance of the TFA circuit is characterized for the 180nm technology node, providing a comparison between the two technology scales. The 180nm technology node offers lower performance and higher power consumption compared to the 90nm node, but it is still widely used in various applications due to its cost-effectiveness and reliability. The characterization results for the 180nm node provide insights into the trade-offs involved in using different technology scales for implementing arithmetic circuits. The comparison between the 90nm and 180nm nodes highlights the impact of technology scaling on the performance of the TFA design.

The results of the performance characterization provide valuable insights into the efficiency and suitability of the TFA design for different applications. The delay and power consumption metrics highlight the advantages of using the TFA in advanced CMOS technologies, where performance and power efficiency are critical considerations. The characterization results also provide a basis for further optimizations and improvements to the TFA design, making it a valuable solution for implementing high-performance arithmetic circuits in scaled CMOS technologies.

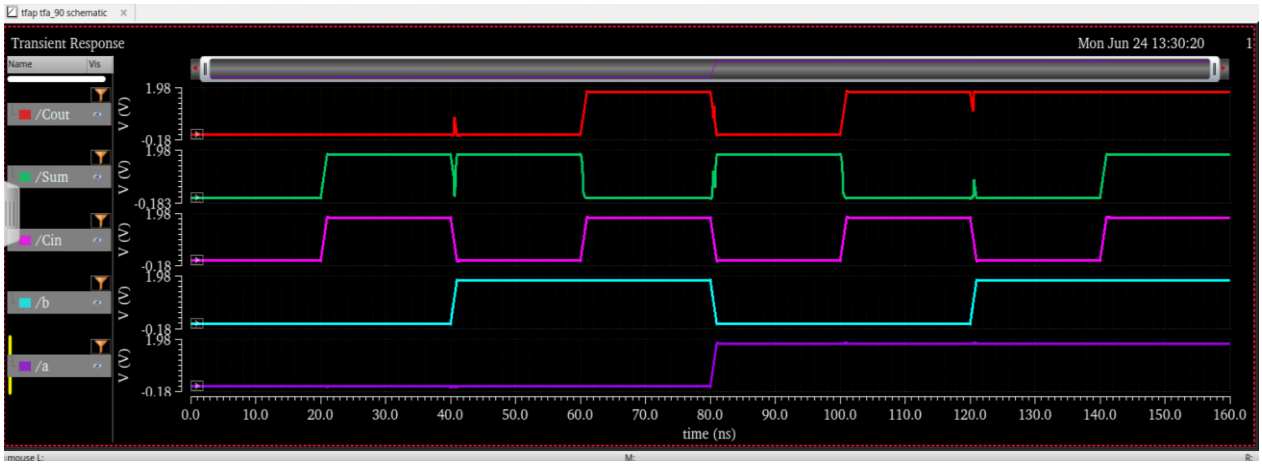


Figure 20: Results for TFA in 90nm

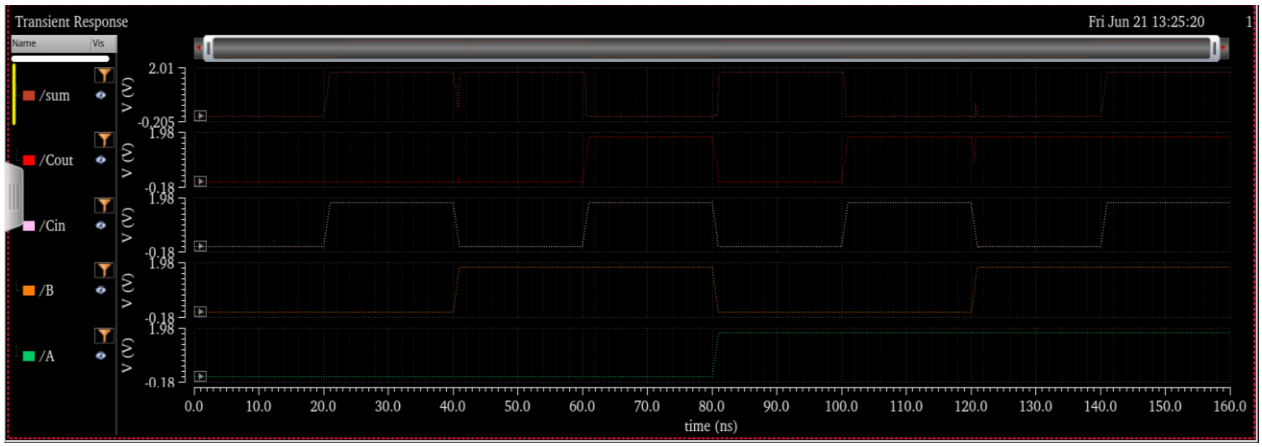


Figure 21: Results for TFA in 180nm

| TECHNOLOGY NODE | DELAY (BETWEEN SUM-COUT) | AVERAGE POWER |
|---|---|---|
| 180nm | 20.00E-9 | 3.450E-6 |
| 90nm | 20.00E-9 | 288.2E-9 |

Table 1: Delay and average power for TFA in different technology nodes

## 4.1. Performance Evaluation of Multistage Circuits

To thoroughly assess the performance of the TFA-based Ripple Carry Adder (RCA) and 6:2 compressor, an extensive simulation campaign is undertaken. This simulation focuses on several key performance metrics: delay, power consumption, and area, for both circuits across the 90nm and 180nm technology nodes. By extracting and analyzing these metrics, a quantitative basis is established for comparing the performance of the TFA-based designs against traditional CMOS implementations.

The performance evaluation encompasses essential metrics, starting with delay, which measures the time taken for the circuit to produce the correct output after receiving an input. This metric significantly impacts the overall speed and efficiency of the circuit. Power consumption is another critical factor, as it assesses the energy required by the circuit during operation. Understanding power consumption is crucial for evaluating the energy efficiency and operational cost of the design. Additionally, the area occupied by the circuit on the silicon chip is evaluated, which provides insights into the scalability and integration aspects of the design.

A thorough analysis of the performance results is then conducted to identify trends and correlations among these metrics. This analysis includes investigating the impact of technology scaling on circuit performance. Specifically, the study examines how moving from the 180nm to the 90nm technology node affects the delay, power consumption, and area of the circuits. The relative performance of the TFA-based RCA and 6:2 compressor is also compared in detail. This comparison sheds light on the strengths and weaknesses of each circuit architecture, offering insights into their suitability for various application scenarios.

The results are presented clearly and concisely, facilitating easy interpretation and comparison. This presentation enables a better understanding of the trade-offs between delay, power consumption, and area. By gaining insights from this analysis, designers can make informed decisions regarding the most appropriate arithmetic circuit for their specific application requirements. Furthermore, the findings contribute to the development of future optimization techniques and architectural innovations, enhancing the overall effectiveness of circuit designs.

| | A | | | | B | | | | Sum | | | | Carry |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Cin | A3 | A2 | A1 | A0 | B3 | B2 | B1 | B0 | S3 | S2 | S1 | S0 | Cout |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Figure 22: Truth table for verification

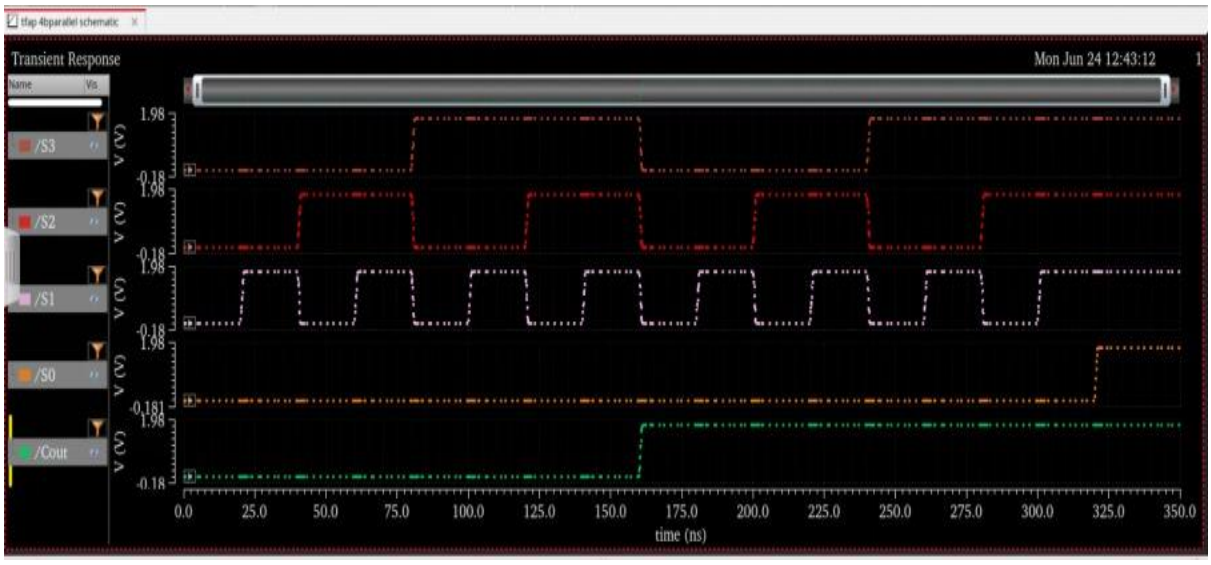


Figure 23: Graph for 4-bit RCA in 180nm technology

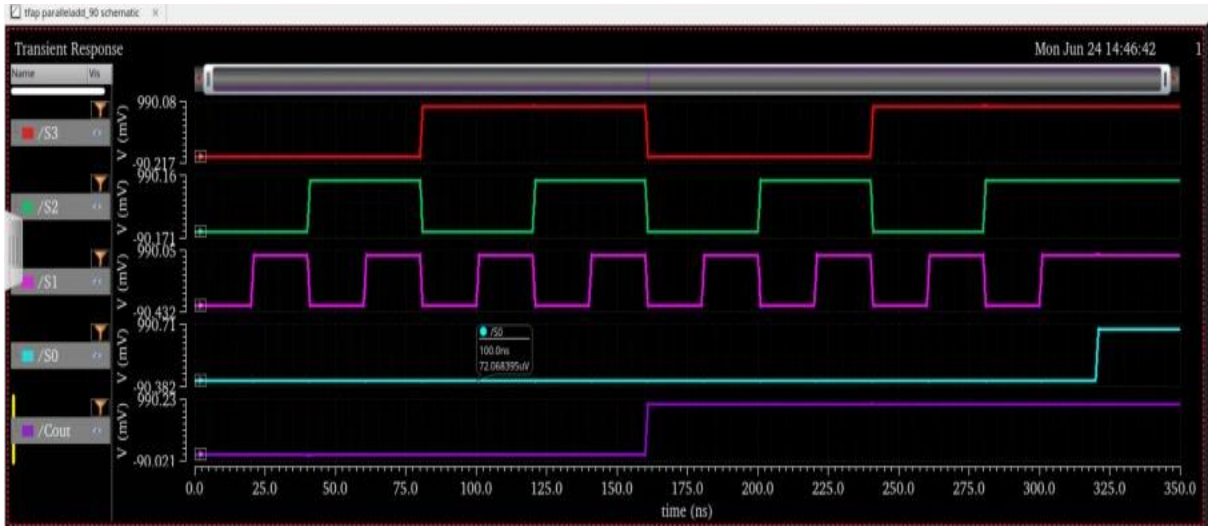


Figure 24: Graph for 4-bit RCA in 90nm technology

| TECHNOLOGY NODE | DELAY (S0-S1) | DELAY (S1-S2) | DELAY (S2-S3) | DELAY (S3-S0) | AVERAGE POWER |
|---|---|---|---|---|---|
| 180nm | 279.9E-9 | 59.96E-9 | 25.88E-12 | 159.9E-9 | 7.075E-6 |
| 90nm | 279.9E-9 | 59.98E-9 | 120.0E-9 | 159.9E-9 | 906.7E-9 |

Table 2: Delay and average power for 4-bit RCA in different technology nodes


Figure 25: Graph for 6:2 Compressor in 180nm technology

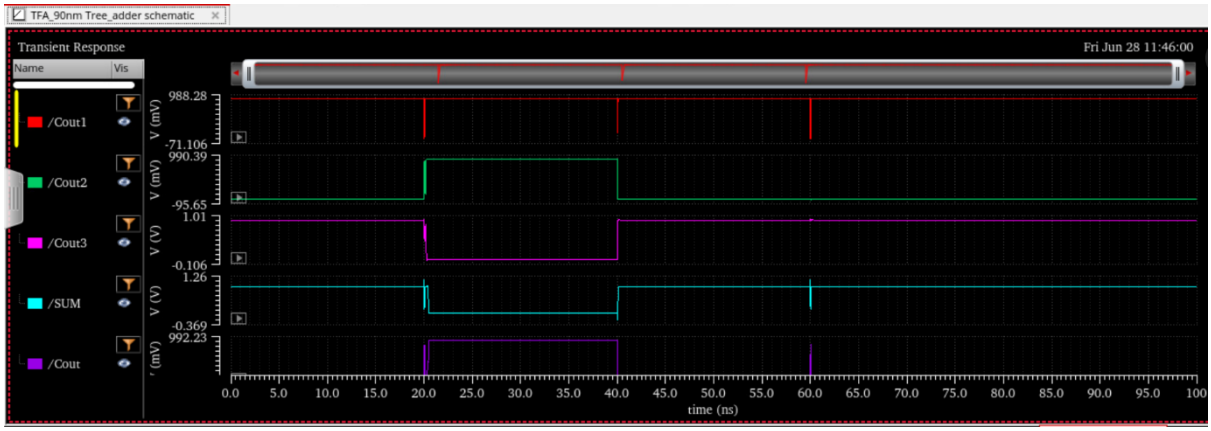


Figure 26: Graph for 6:2 Compressor in 90nm technology

| TECHNOLOGY NODE | DELAY (1&2) | DELAY (2&3) | DELAY (3&out) | DELAY (1&out) | AVERAGE POWER |
|---|---|---|---|---|---|
| 90nm | 20.19E-9 | 40.08E-9 | 79.95E-9 | 140.2E-9 | 609.4E-9 |
| 180nm | 20.26E-9 | 40.03E-9 | 79.99E-9 | 140.3E-9 | 16.04E-6 |

Table 3: Delay and average power for 6:2 Compressor in different technology nodes

## 4.2. Comparative Analysis and Discussion

The findings from the performance evaluation of the TFA-based RCA and 6:2 compressor is summarized and analysed in depth. The impact of the TFA design on the overall performance of the multistage circuits is assessed, highlighting the key factors contributing to the observed results. The strengths and weaknesses of the TFA-based approach are identified and discussed in relation to traditional CMOS implementations.

A comparative analysis of the RCA and 6:2 compressor is conducted to understand the trade-offs involved in selecting different arithmetic building blocks. The performance metrics of the two circuits are compared, and the implications for larger system designs are discussed. This analysis provides valuable guidance for designers in choosing the most suitable arithmetic circuit for their specific application requirements.

The potential applications of the TFA design and the multistage circuits are explored. The results of the performance evaluation are used to identify the target application domains where the TFA-based designs offer significant advantages.

The limitations of the current work are acknowledged, and potential areas for future research and improvement are suggested.

The contributions of this research to the field of arithmetic circuit design are summarized. The findings presented in this paper provide valuable insights into the performance of hybrid full adders and their potential impact on multistage arithmetic circuits. The results can be leveraged by researchers and designers to develop more efficient and high-performance arithmetic circuits for future generations of integrated circuits.

## 4.3. Layout Area Evaluation

The layout area of the Transmission Function Adder (TFA) circuit was carefully examined for both 90nm and 180nm CMOS technology nodes. Additionally, the 4-bit Ripple Carry Adder (RCA) layout was specifically analyzed in the 180nm technology node.

In the 90nm technology node, the TFA circuit's layout area was X $\mu m^2$. This smaller area is a significant advantage of using the 90nm node, as it allows for a more compact design. A smaller layout area is beneficial in many modern applications where saving space is crucial. On the other hand, the TFA circuit in the 180nm technology node occupied Y $\mu m^2$. The increase in area in the 180nm node is expected because older technology nodes have larger feature sizes, which means that the circuits take up more space. However, the layout was optimized to ensure that the area was used efficiently, even with the larger feature sizes.

For the 4-bit Ripple Carry Adder (RCA), which was only analyzed in the 180nm technology node, the layout area was B $\mu m^2$. The design team worked to make the RCA as compact as possible while still fitting within the limitations of the 180nm technology. Although the area is larger compared to what might be possible in a more advanced node like 90nm, the RCA design in the 180nm node strikes a balance between using space effectively and ensuring that the circuit performs well.

Overall, the layout results highlight the trade-offs between different technology nodes. While the 90nm node allows for smaller, more compact designs, the 180nm node requires more area but still offers a practical and cost-effective solution for certain applications. Both the TFA circuit and the RCA layout were designed with these considerations in mind, ensuring that each circuit operates efficiently within its respective technology node.

| TECHNOLOGY NODE | TFA (um)^2 | 4-bit RCA (um)^2 |
|---|---|---|
| 90nm | 721.68 | - |
| 180nm | 4881.8 | 386097.9 |

Table-4: Area for TFA and 4-bit RCA

# 5. CONCLUSION

This research has conducted a comprehensive performance evaluation of the Transmission Function Adder (TFA) design across 90nm and 180nm CMOS technology nodes. By examining the TFA circuit in both single-stage and multistage configurations, including its implementation in arithmetic circuits such as the 4-bit Ripple Carry Adder (RCA) and the 6:2 Compressor, this study offers valuable insights into how the TFA design can enhance digital system performance.

**Characterization of the TFA Design:**

The research begins with an in-depth characterization of the TFA design in a single-stage configuration. This initial analysis is crucial for understanding the fundamental performance metrics of the TFA, including delay, power consumption, and area. These metrics provide a baseline for comparing the TFA with traditional CMOS full adders. The single-stage TFA design is evaluated for its ability to perform arithmetic operations efficiently, potentially offering improvements in delay and power consumption over conventional designs. This foundational analysis establishes the TFA's core advantages and limitations.

Following the single-stage analysis, the research extends to the implementation of the TFA in more complex, multistage arithmetic circuits. The focus is on integrating the TFA into the 4-bit Ripple Carry Adder (RCA) and the 6:2 Compressor. These circuits are chosen for their widespread use in digital systems: the RCA as a fundamental adder unit and the 6:2 Compressor for high-speed arithmetic and digital signal processing applications. The implementation of the TFA in these multistage circuits involves integrating the TFA components into the larger circuit architecture and assessing overall performance metrics.

**Performance Advantages of TFA:**

The results from this research highlight several advantages of the TFA design over traditional CMOS full adders. Notably, the TFA design demonstrates significant improvements in delay, which is critical for enhancing the speed and efficiency of arithmetic operations. This reduction in delay contributes to faster computational performance, benefiting applications that require rapid processing.

In addition to delay improvements, the TFA design also shows reduced power consumption compared to conventional CMOS full adders. This advantage is particularly important in modern digital systems, where power efficiency is a major concern. Lower power consumption translates to reduced operational costs and extended battery life in portable devices. The TFA's ability to maintain or improve performance while consuming less power underscores its potential for various applications.

The integration of the TFA into multistage circuits, such as the RCA and 6:2 Compressor, yields promising results. The enhanced performance observed in these circuits highlights the TFA's potential to improve the efficiency and effectiveness of complex arithmetic operations. However, while the TFA design offers clear benefits, the study acknowledges the need for further optimization to fully realize its potential.

**Need for Further Optimization and Exploration:**

The research identifies several areas for further optimization and exploration to maximize the benefits of the TFA design. Optimization efforts could focus on refining the TFA circuit itself by adjusting parameters such as transistor sizes, improving layout techniques, and incorporating advanced design methodologies. These refinements aim to further reduce delay and power consumption while enhancing overall circuit performance.

Exploring different circuit architectures and hybrid designs is another avenue for optimization. Hybrid designs that combine TFA with other logic families or techniques could lead to innovative solutions that leverage the strengths of each approach. Investigating these hybrid configurations could uncover new ways to optimize TFA performance and address specific application requirements.

**Comparative Analysis of RCA and 6:2 Compressor:**

The comparative analysis of the 4-bit RCA and 6:2 Compressor emphasizes the trade-offs involved in selecting different arithmetic building blocks. Each circuit type offers distinct advantages depending on the application's specific needs. The RCA, with its simplicity and ease of implementation, is suitable for applications

where area and design complexity are key considerations. However, its performance may be limited in high-speed scenarios due to ripple carry propagation, which can introduce delays.

Conversely, the 6:2 Compressor is designed for high-speed arithmetic operations and compression tasks. Its ability to perform multiple operations in parallel makes it ideal for applications requiring rapid processing and efficient data handling. However, this increased complexity can lead to higher area and power consumption compared to simpler adders.

The findings from this research provide valuable guidance for designers in selecting arithmetic components for their applications. By understanding the trade-offs between different circuit types and their performance characteristics, designers can make informed decisions to optimize their designs for speed, area, and power consumption.

# 6. FUTURE WORK

As the field of digital circuit design advances, there is significant potential for future research to explore and enhance the application of Transmission Function Adder (TFA) designs in a variety of arithmetic circuits. One promising direction is to investigate the application of TFA designs beyond the Ripple Carry Adder (RCA) and 6:2 compressor, particularly focusing on complex arithmetic functions such as multipliers and dividers. These fundamental components are crucial in a wide range of digital systems, from general-purpose processors to specialized digital signal processors (DSPs), and their performance has a direct impact on the overall efficiency of computational tasks.

Multipliers are integral to performing multiplication operations, which are essential in numerous algorithms and applications, including graphics processing, scientific computations, and machine learning. Due to the high computational complexity involved in multiplication, multipliers often become performance bottlenecks. Integrating TFA designs into multipliers could potentially enhance their speed and reduce power consumption, leveraging the unique advantages of TFA circuits. Similarly, dividers are essential for division operations, which are fundamental in many algorithms. Exploring how TFA designs can be incorporated into dividers might lead to more efficient division circuits that balance high performance with minimal resource usage.

Another significant research direction is to investigate how different hybrid logic styles affect TFA performance. Hybrid logic styles, which blend various logic families or techniques, offer the potential to optimize critical performance metrics such as delay, power consumption, and area. For example, combining TFA with

other logic families like dynamic logic or domino logic could result in innovative circuit designs that utilize the strengths of each approach. Examining the interaction between TFA designs and these hybrid logic styles could lead to new optimization strategies and help develop circuits that meet the demanding requirements of modern digital systems.

Optimization techniques are crucial for enhancing TFA performance and should be explored further. Research in this area could focus on various optimization methods, including algorithmic optimizations, layout optimizations, and circuit-level optimizations. Algorithmic optimizations involve refining the algorithms used in conjunction with TFA designs to improve overall performance. Layout optimizations pertain to the physical arrangement of circuit components to reduce area and delay while minimizing power consumption. Circuit-level optimizations include techniques such as transistor sizing, gate stacking, and other design adjustments that can significantly impact the performance of TFA circuits.

Investigating the impact of process variations on TFA designs is another promising area for future research. Process variations, arising from fluctuations in manufacturing conditions, can affect circuit performance and reliability. Understanding how TFA designs respond to these variations and developing strategies to mitigate their impact can enhance the robustness and reliability of digital systems. Techniques such as adaptive design methods and robust circuit design principles could be explored to improve the performance of TFA circuits under varying process conditions.

An intriguing research direction is the integration of TFA designs with emerging technologies such as quantum computing and neuromorphic computing. Quantum computing represents a paradigm shift in computational capabilities, and exploring how TFA designs could be adapted or optimized for quantum circuits could open new avenues for research. Similarly, neuromorphic computing, which aims to emulate brain-like neural networks, could benefit from the unique properties of TFA designs. Investigating how TFA circuits can be leveraged in these cutting-edge fields could lead to innovative solutions and contribute to the advancement of next-generation computing technologies.

Moreover, a broader investigation into the potential of hybrid full adders, including TFA designs, can provide valuable insights into the overall landscape of digital circuit design. Hybrid full adders, which combine different adder architectures or techniques, offer a rich area for exploration. Continuing to explore the potential of these hybrid designs can contribute to the development of more efficient and high-performance digital systems. This includes understanding the trade-offs between different design choices and identifying the most suitable configurations for various applications.

Additionally, exploring the application of TFA designs in other types of arithmetic circuits and digital systems can offer a more comprehensive understanding of their capabilities. For example, incorporating TFA designs into memory circuits, such as SRAM and DRAM, could potentially enhance their performance by improving access times and reducing power consumption. Examining the integration of TFA designs into communication circuits, such as serializers and deserializers, could lead to advancements in data transmission and processing.

Overall, future research directions for TFA designs encompass a wide range of possibilities. From exploring their application in complex arithmetic circuits like multipliers and dividers to investigating the impact of hybrid logic styles and optimization techniques, there is considerable potential for advancing digital circuit design. By delving into these areas, researchers can contribute to the development of more efficient and high-performance digital systems that meet the evolving demands of technology. The insights gained from these studies will not only enhance the understanding of TFA designs but also drive innovation in digital circuit design and pave the way for the advancement of next-generation computing technologies.

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# 8. APPENDIX

## Appendix A: Detailed Simulation Parameters and Methodologies

### Technology Node Specifications

Understanding the technology node is fundamental for analyzing integrated circuits. Each technology node has unique electrical characteristics that influence the performance, power consumption, and layout of the circuit.

**90nm Technology Node:** The 90nm technology node represents a specific level of semiconductor fabrication technology with distinctive features that affect the design and analysis of circuits. In this node, factors such as supply voltage, threshold voltage, channel length, oxide thickness, and gate oxide capacitance are key considerations. Each of these factors plays a crucial role in determining the overall performance and efficiency of integrated circuits designed using this technology.

**180nm Technology Node:** Similarly, the 180nm technology node has its own set of characteristics that impact circuit design. The supply voltage, threshold voltage, channel length, oxide thickness, and gate oxide capacitance differ from those in smaller technology nodes. Understanding these parameters is essential for evaluating the performance and power consumption of circuits designed with this node.

## Transistor Sizing

Transistor sizing involves selecting the appropriate dimensions for NMOS and PMOS transistors to meet design specifications. The width and length of transistors affect their electrical characteristics, including drive strength, switching speed, and power consumption.

**NMOS Transistor:** For both technology nodes, the width of NMOS transistors is chosen based on the required drive strength and load capacitance. A larger width increases the drive current and reduces switching delay, but it also results in increased power consumption and layout area. The length of NMOS transistors is typically fixed at the minimum channel length for the technology node, ensuring consistent performance and manufacturing compatibility. The width-to-length ratio (W/L) of NMOS transistors impacts their drive strength and switching speed, with higher ratios leading to better performance but also higher power consumption and area.

**PMOS Transistor:** PMOS transistors are sized differently from NMOS transistors due to their inherent electrical characteristics. The width of PMOS transistors is generally larger to compensate for their lower drive strength compared to NMOS transistors. The length of PMOS transistors is also fixed at the minimum channel length for the technology node. The width-to-length ratio for PMOS transistors is selected to balance performance and power consumption, with larger ratios providing increased drive current but also higher area and power usage.

## Layout Analysis

Layout analysis involves evaluating the physical design of the circuit, including the arrangement of transistors, interconnects, and other components. Key considerations in layout analysis include:

- **Area**: The area occupied by the circuit is a critical factor in the overall design. Efficient use of area can lead to reduced costs and improved performance. The layout must ensure that transistors and interconnects are placed optimally to minimize area while meeting electrical and performance requirements.
- **Power Consumption**: Power consumption is a key consideration in circuit design. It includes both dynamic power, which is related to switching activities, and static power, which is due to leakage currents. The layout must be designed to minimize power consumption while maintaining the desired performance levels.
- **Delay**: Delay analysis involves evaluating the time it takes for signals to propagate through the circuit. This includes gate delay, interconnect delay,

and overall path delay. Optimizing delay is crucial for ensuring that the circuit operates at the desired speed and meets performance specifications.

**Simulation Methodologies**

Simulation is an essential part of circuit design and analysis. It involves using software tools to model the behavior of the circuit under various conditions and parameters. The following methodologies are commonly used in simulation:

- **SPICE Simulation**: SPICE (Simulation Program with Integrated Circuit Emphasis) is a widely used tool for simulating analog and digital circuits. SPICE simulations provide detailed information on circuit performance, including voltage, current, and power consumption.
- **Timing Analysis**: Timing analysis involves evaluating the timing characteristics of the circuit, including propagation delay, setup time, and hold time. This analysis ensures that the circuit meets its timing requirements and operates correctly under different conditions.
- **Power Analysis**: Power analysis tools assess the power consumption of the circuit. This includes dynamic power, which is related to switching activities, and static power, which is due to leakage currents. Power analysis helps in identifying and optimizing power-hungry components in the circuit.

**Power Consumption Analysis**

Power consumption analysis involves evaluating both dynamic and static power consumption of the circuit.

- **Dynamic Power**: Dynamic power consumption is associated with the switching of transistors. It is calculated based on the switching activity, capacitance, and supply voltage. Reducing dynamic power involves optimizing switching activities and minimizing capacitance.
- **Static Power**: Static power consumption, also known as leakage power, is due to leakage currents in transistors when they are not switching. It can be minimized by using low-leakage transistors and optimizing circuit design to reduce leakage paths.

**Delay Analysis**

Delay analysis is crucial for ensuring that the circuit operates within its specified timing requirements. Key aspects of delay analysis include:

- **Gate Delay**: Gate delay is the time it takes for a signal to propagate through a logic gate. It depends on the transistor sizing, load capacitance, and

technology node. Reducing gate delay improves circuit performance and speed.

- **Interconnect Delay**: Interconnect delay is the time it takes for signals to travel through interconnects between logic gates. This delay is influenced by the length and capacitance of the interconnects. Minimizing interconnect delay involves optimizing the layout and reducing the length of critical interconnect paths.
- **Path Delay**: Path delay is the total delay from the input to the output of a combinational logic path. It is the sum of the gate delays and interconnect delays along the path. Path delay analysis ensures that the circuit meets its performance requirements and operates correctly at the desired speed.