UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5 Examination in Engineering: August 2024

Module Number: EE5201 **Module Name: Computer Architecture**

[Three Hours]

[Answer **all questions**, each question carries 10 marks]
[You are not allowed use calculators]

Q1 a) Describe the fetch cycle and the execute cycle of the Von Neumann Machine.

[2 Marks]

b) Describe the Data flow analysis techniques built into processors to improve the performance.

[2 Marks]

c) List TWO design modifications implemented to balance the performance disparity between the main memory and the processor.

[2 Marks]

d) List TWO challenges in increasing the processor's clock speed.

[1 Mark]

e) Describe the steps done by the processor when an interrupt is pending.

[2 Marks]

f) Briefly explain the operation of Direct Memory Access (DMA).

[1 Mark]

Q2 a) Describe the solution for the bottleneck caused by devices with growing data rates in bus-based computer systems.

[2 Marks]

b) What are the advantages of using point-to-point interconnect than shared buses?

[2 Marks]

c) What is difference between PCI and PCI Express protocol?

[1 Mark]

d) Describe how a memory word is transferred between the CPU and the main memory in the presence of a single cache memory.

[2 Marks]

e) What is the main purpose of the Hardware Memory Management Unit of a cache system?

[1 Mark]

f) Assume in a direct mapping cache system the memory is addressed using 24-bits. A 4-bit word number is used to select one of the 16 words in that cache line. The cache line are indexed using 14-bit line number. Calculate the number of bocks that map into one cache line.

[2 Marks]

Q3 a) Describe how the set-associative mapping has overcome the issues with direct and associative mapping.

[2 Marks]

b) List TWO advantages of multi-level cache.

[1 Mark]

c) Describe the locality of reference principle in relation to cache memory.

[1 Mark]

d) Assume the processor has access to two levels of memory. Level 1 contains 10,000 words with an access time of 0.02 µs, and Level 2 contains 100,000 words with an access time of 0.2 µs. Ignore the time required for the processor to determine whether the word is in Level 1 or Level 2. Given that 95% of memory accesses are found in Level 1. Calculate the average time to access a word.

[2 Marks]

e) Draw a circuit diagram of a dynamic RAM cell and describe the write operation.

[2 Marks]

f) Draw a circuit diagram and explain how a flip-flop is used to hold the logic state 1 and 0 in a static RAM.

[2 Marks]

Q4 a) Compare and contrast SRAM and DRAM in terms of structure, speed, cost and applications.

[2 Marks]

b) Assume 8-bit word 10111011 is stored in semiconductor main memory Use the following equations to calculate the check bits. In the equations D1 is the least significant bit and D8 is the most significant bit. Calculate the syndrome word if D1 is changed from 1 to 0.

$C1 = D1 \oplus D2 \oplus D4 \oplus D5 \oplus D7$
$C2 = D1 \oplus D3 \oplus D4 \oplus D6 \oplus D7$
$C4 = D2 \oplus D3 \oplus D4 \oplus D8$
$C8 = D5 \oplus D6 \oplus D7 \oplus D8$

[2 Marks]

c) Describe the write operation of a magnetic disk write head.

[2 Marks]

d) What is the difference of Redundant Array of Independent Disks (RAID) Level 0 and 1?

[2 Marks]

e) What are the practical challenges associated with the performance of Solid-State Drives (SSDs)?

[2 Marks]

Q5 a) Use unsigned binary multiplication to multiply two numbers stored in Q=1111 and M=1010 registers. Assume that the accumulator (A) register and carry (C) flag are initialized to zero. Show all the steps in your answer.

[2 Marks]

b) Use twos complement division to divide a number stored in Q = 0111 register by 0010. Assume that the accumulator (A) register is initialized to zero. Show all steps in your answer.

[2 Marks]

c) Describe the data flow of the interrupt cycle.

[2 Marks]

d) Describe how data hazards reduces the performance of a instruction pipeline.

[2 Marks]

e) Describe the problem of cache coherence problem in a multiprocessor system.

[2 Marks]