January 2024

Computer Architecture and Organization

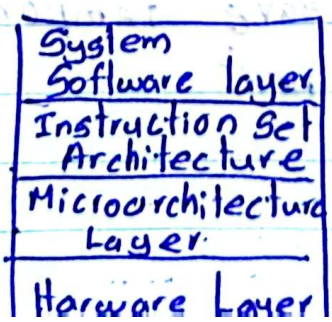
Q1

(a) (i) RISC (Reduced Instruction Set Computer)
This processors use a small set of simple instructions, each executing in a single clock cycle. This allows for faster processing and simpler instruction decoding.

CISC (Complex Instruction Set Computer).
This processors have larger set of more complex instructions, which can execute multiple low-level operations in a single instructions. This can reduce the number of instructions needed for a task, though each instruction may take multiple cycles to execute

(i) Micro Architecture
The cpu executes these instructions, which involve moving data to memory and storage

Instruction Set Architecture
The operating system uses the ISA to send instructions to the CPU



(b) Memory wall

This is a processor desing constraint that refers to the growing disparity between CPU speed and memory speed.

* ~~Eto~~ Cache memory
* Prefetching
* Piperlining and out of Order Execution
* Memory Hierchies

(c) Right Instruction executes first

PC : 5208

PC sends memory address to MAR, fetching data from memory

PC → MAR

Data from memory is stored in MBR

MBR is split into two part

MBR (20:27) → IR opcode 00010 10

MBR (28,39) → MAR operand address (000000000000)

opcode → IR

operand address → MAR

left instruction save temporally at IBR to execute next

IBT (0:7) → opcode
IBR (8:19) → operand address

Once the opcode is In the IR, the execut cycle is performed
IR will send data to control circuit for execution

IR → Control circuit

MAR loads the operand address

After execution of righ instruction, left instruction opcode will load to IR and address will load to MAR

PC increment to PC+1
PC ← PC + 1 (5209)

(ii) 5208
MBR → 0

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d)

(i) Quantum computers have the potential to solve certain types of problems much faster than classical computers by using quantum bits and leveraging principles like superposition, ~~and entanglement~~. This allows to explore multiple solutions simultaneously.

(ii) major challenge in this is quantum computing. Because Qbits are more sensitive to their environment. So building stable error-free quantum computers extremely difficult

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Q2

a) We add the extra bit to the msg and recordes it. After the resiving msg we calculate the extra added bits and compare it with first one. If there is any changes. The ~~msg~~ signal was changed. We can find the change position using Hammig code

b) main memory : 16 Gbytes
: $2^4 \times 2^{30}$
: 2^{34} bytes

cache = 8 kbytes
= $2^3 \times 2^{10}$ bytes
= 2^{13} bytes

offset = 16 bytes
= 2^4 bytes

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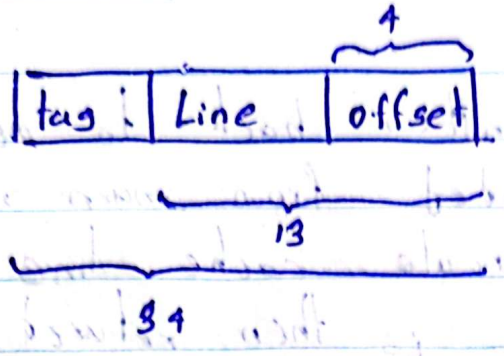
(i)



number of cache lines: 13 - 4
= 9 bit

(ii) 0x ABCD 1234

↓

Binary

00 1010 1011 1100 1101 0001 0010 0011 0100

offset 0100

line: 1 0010 00

$2^9\ 2^8\ 2^7\ 2^6\ 2^5\ 2^4\ 2^3\ 2^2\ 2^1\ 2^0$

line = 291

(iii) First processor check the memory address. check the corresponding line using the index bits. If cache miss It will need to be loaded from the main memory into the cache If already data in the cache line that needs to be replaced and the data has been modified

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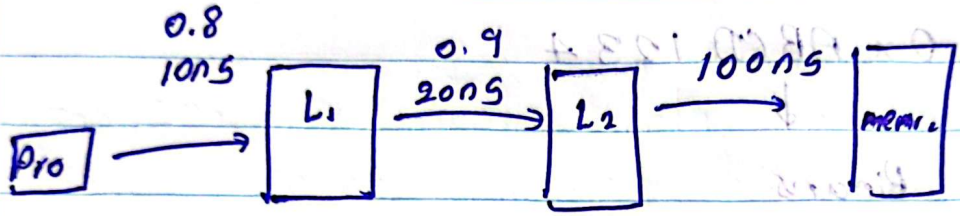
(iii) If will be written back to memory The data loaded from main memory into the appropriate cache line. The value 0x31 is then relwed to the CPU for processing

c)

(i)



time = 0.8 (10) + 0.9 × 0.2 (20+10) + 0.1 × 0.2 (10+20+1

= 16 ns

(ii) Increased Latency
A large cache takes longer to search and acces due to its siz, which can slow down the average access time. By having multiple levels of smaller caches, frequently accesed data can be found more quickly in the smaller, faster L1 cache improving performance

(iii) Increased complexity in cache management

The system needs to manage data consistency between cache levels, and additional logic is required to handle cache misses and decide which level to access. This complexity can add to the design and maintenance cost of the processor

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Q3

(a)

(i) If we added more devices we can see bottlenecks and propogtion delay

(ii) Not effective with high performance I/O devices

(i.) Systems increasingly rely on point-to point interconnectivr rather than shared buses

(b) instructions — 100
stage — 5
10 clock cycles to compl

(i) with out pinelinnig : $100 \times 5 \times 10$
$= 5000$ clock cycles

with pineliniy : $5 \times 10 + 99 \times 10$
$= 50 + 990$
$= 1040$

speed up : $\frac{5000}{1040}$

=

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(ii) branch instructions = 20 x 5 x 10
= 1000

first instructions = 5 x 10
= 50

pipeline = 10 x (100 - 20 - 1)
= 10 x 79
= 790

speed up = $\frac{5000}{790 + 50 + 1000}$ = 2.72

branche = 20 x $\frac{90}{100}$
= 18

branche instruction = 18 x ~~5~~ 10 = ~~900~~ 180

$\begin{array}{r} 18 \\ 5 \\ \hline 90 \end{array}$ 4

first instruction = 5 x 10
= 50

pipeline = 10 x (100 - 20 - 1)
= 790

error = 2 x 10 x 5
= ~~20~~ 100

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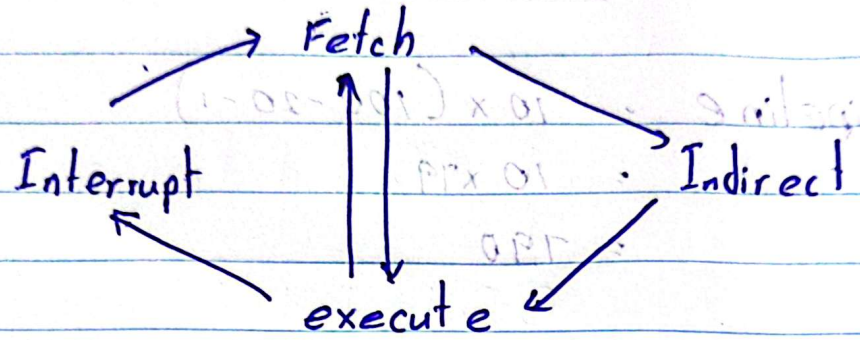
$$\text{speed up} = \frac{5000}{180+100+790+50}$$

$$= 4.46$$

(iv)



c)

(i) An interrupt service Routine is a function or code segment that executes when an interrupt is triggered.

(ii) Fetch → CPU retrives the next instruction from mem
Decode → The instruction is decoded to understand th
Execute → The cpu performs the operation specified by the instruction.

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d)

(i) High Bandwidth Low latency
Scalability
Reduced Bottlenecks

Q4

(a) +65

0 1000001
1 0 1 1 1 1 0 ← 1s complement
+ 1
1 0 1 1 1 1 1 1

-65 0 1 1 1 1 1 1

(i) 35 - (-65)

-(-65) 0 1 1 1 1 1 1
1 0 0 0 0 0 0
+ 1
1 0 0 0 0 0 1

35 ⇒ 1 0 0 0 1 1

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Q3 $35 - (-65)$

$$
\begin{array}{r}
1000\,11 \\
+\ 100001 \\
\hline
(1)\,1000100 \\
\hline
\end{array}
\qquad \text{(1 carried to the left)}
$$

$$
\begin{array}{r}
111011 \\
+\qquad\ 1 \\
\hline
111100 \\
\hline
\end{array}
$$

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(iii)

```
        0 0 0 1 0 0
1011 | 1 1 0 1 0 1 1
       0
       ---
       1 1
       0
       ---
       0 0
       0
       ---
       1 1 0
       0 0 0
       -------
       1 1 0 1
       1 0 1 1
       -------
       0 0 1 0 0
         0 0 0
         -------
           1 0 0 1
```

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