UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5 Examination in Engineering: January 2024

Module Number: EE5250 **Module Name: Computer Architecture and Organization**

[Three Hours]

[Answer **all questions**, each question carries **12.5 marks**]

Answer all the questions in point form unless otherwise specified.

Q1 a) Briefly describe the following.

i) Difference between RISC and CISC architecture.

ii) Difference between Micro Architecture and Instruction Set Architecture.

[2 x 1 Marks]

b) Briefly explain the processor design constraint "Memory Wall" and how the processor designer has overcome this problem.

[2 Marks]

c) The architecture of an IAS computer is given in Figure Q1a and the format of an instruction is given in Figure Q1b. Further, the memory occupancy is given in Figure Q1c. Suppose that the Program Counter consists of the value 5208 and the right-hand side instruction is executed first.

i) Discuss the operation of one instruction cycle using associated registers and provide value of each of those registers. You may use any number of stages in the instruction cycle.

[4 Marks]

ii) Evaluate the two instruction cycles and identify the two signals received at the Control circuits.

[1 Mark]

iii) If the two signals to Control circuits mean load MQ to AC and transfer M(X) to MQ, respectively, identify the memory address accessed through the Control circuit operation.

[0.5 Marks]

d) Quantum computers are known to be superior over the classical computers.

i) Briefly describe the superiority of quantum computers over the classical computers and how it is achieved.

[2 Marks]

ii) Explain one challenge in implementing quantum computers.

[1 Mark]

Q2 a) Briefly describe Hamming codes in the context of their error detection and correction ability.

[1.5 Marks]

b) Consider a computer system with a processor equipped with 8 Kbytes cache, connected to a main memory of 16 Gbytes. The offset is 16 bytes and uses a direct-mapped cache mapping technique.

i) Identify the number of cache lines in the cache memory. Clearly outline each step in your calculation.

[1 Mark]

ii) Given a memory address of 0xABCD1234 containing the value 0x56, identify the specific cache line this address would map. Show your calculation steps.

[1 Mark]

iii) Suppose that the memory address 0xDBAD9237 containing the value 0x31 is to be read from the memory. Briefly explain each step of the process along with the values stored at/removed from relevant memory locations, if the write back cache write policy is used.

[3 Marks]

c) Consider a computer system with a processor that has two levels of cache. The first-level cache (L1) has a hit ratio of 0.8 and an access time of 10ns, while the second-level cache (L2) has a hit ratio of 0.9 and an access time of 20ns. The main memory access time is 100ns.

i) Calculate the effective cache access time showing all your steps.

[2 Marks]

ii) Discuss one disadvantage of having larger size of single cache than having multiple levels of smaller cache.

[1 Mark]

iii) Discuss one disadvantage of having multiple levels of cache.

[1 Mark]

d) Consider the following code segment written to calculate the sum of all elements in 'values' array, which consists of M rows and N columns. The term **values[i][j]** gives the element of i^{th} row j^{th} column. Discuss the code in terms of its effect on memory access time.

```
int i, j, sum = 0;
  while (j < N) {
    while (i < M) {
      sum += values[i][j];
      i += 1 ;
    }
    j += 1;
  }
```

[2 Marks]

Q3 a) Figure Q3a illustrates a traditional bus architecture having an Expansion bus. Briefly explain the following.

i) A problem which is being addressed by introducing an expansion bus.

ii) A problem associated with this bus architecture.

iii) A solution to the problem described in part ii).

[3 x 1 Marks]

b) A program consists of 100 instructions running on a processor with a 5-stage pipeline. Suppose that each stage of the pipeline requires 10 clock cycles to complete.

i) Calculate the speedup of the processor due to pipelining compared to a processor without pipelining, assuming there are no branch instructions.

ii) Calculate the speedup of the processor when 20 of the instructions are branch instructions.

iii) Suppose that the branch prediction is occupied and the prediction accuracy is 90%. Calculate the speedup of the processor compared to a processor without pipelining.

[3 x 1.5 Marks]

iv) Draw a block diagram of the instruction cycle of this five-stage pipeline. Mention any assumption you make.

[1 Mark]

c) Interrupts are used to improve the efficiency of program execution in terms of the execution time.

i) Briefly explain what is an interrupt service routine.

ii) Considering a 3-stage instruction cycle, briefly explain when will the interrupt service routine be triggered.

[2 x 1 Marks]

d) Physical interface of Intel Quick Path Interconnect (QPI) is shown in Figure Q3b. Briefly explain the following.

i) What is the advantage of QPI over bus architecture.

ii) How does the physical unit of transmission of QPI become 20 bits?

[2 x 1 Marks]

Q4 a) Two's (2's) complement representation is commonly used in computer arithmetic. Respond to the following questions by outlining the operational steps.

i) Represent -65 as a 2's complement binary number.

[1 Mark]

ii) Carry out the binary subtraction 35 – (-65) using 2's complement representation.

[1.5 Marks]

iii) Carry out the binary division 1101011/1011

[1 Mark]

iv) Carry out the binary multiplication 8 x 9 using the algorithm given in Figure Q4a and the template given in Figure Q4b. Clearly show each step of your calculation.

[2 Marks]

b) List two differences between processes and threads.

[1 Marks]

c) Consider a symmetric multiprocessor system as shown in Figure Q4c. Assume that six numbers are stored in adjacent memory locations in the main memory. The task is to calculate the sum of these six numbers.

i) Briefly discuss how the symmetric multiprocessor system achieves speedup in calculating the sum of the given six numbers.

[2 Marks]

ii) Using the knowledge in cache memory, discuss how a single processor might outperform multiple processors in this specific summation.

[2 Marks]

d) Briefly explain how cache coherent Non-uniform Memory Access works.

[2 Marks]

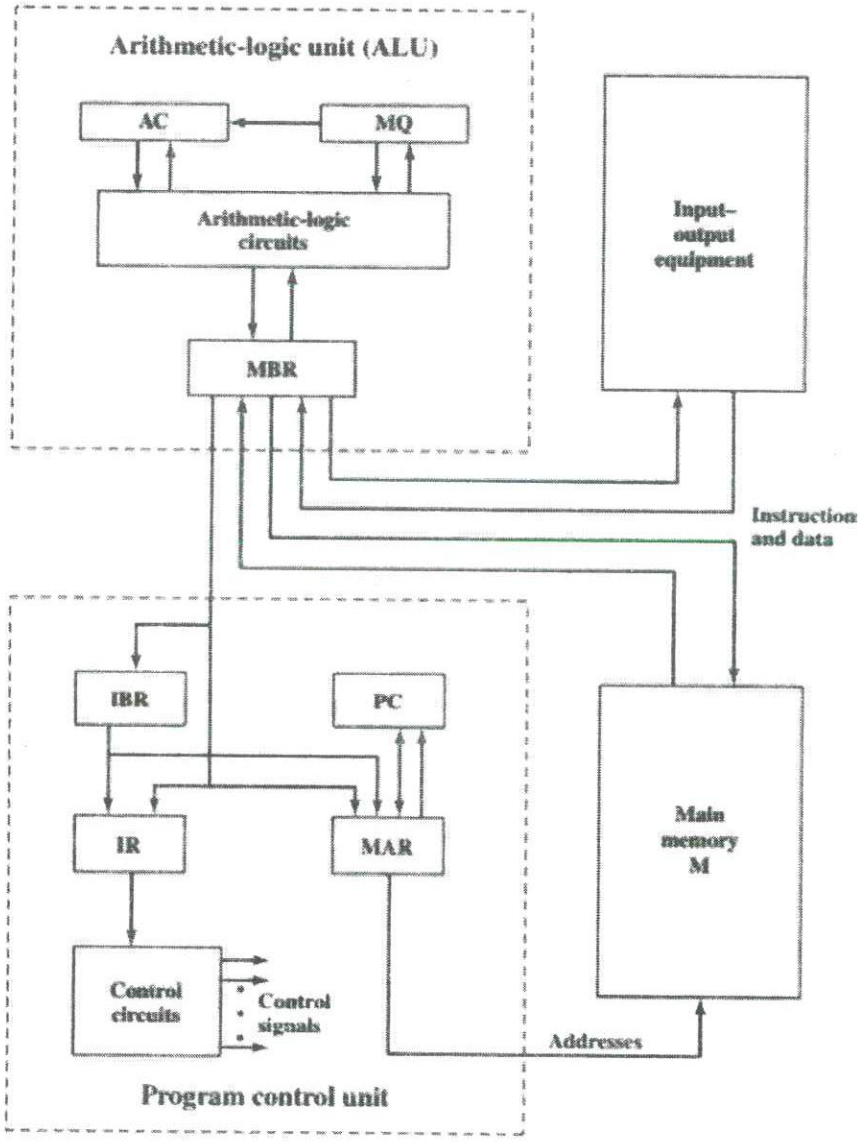

Figure Q1a: The architecture of an IAS computer

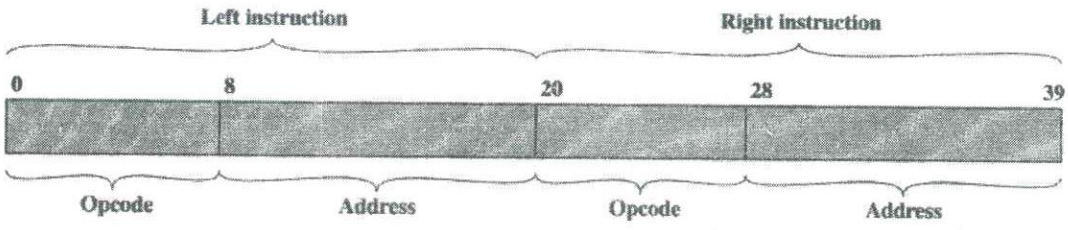

Figure Q1b: Word Format of an IAS computer

Address	Data
5208	0x0988A0A000
5209	0x060882108A

Figure Q1c: Memory occupancy

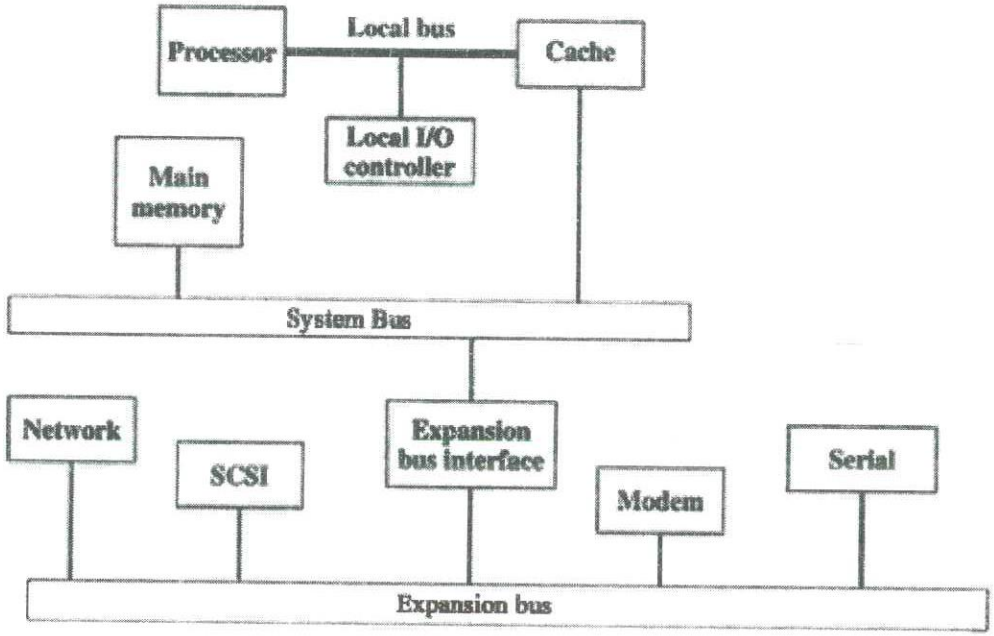

Figure Q3a: Traditional Bus Architecture

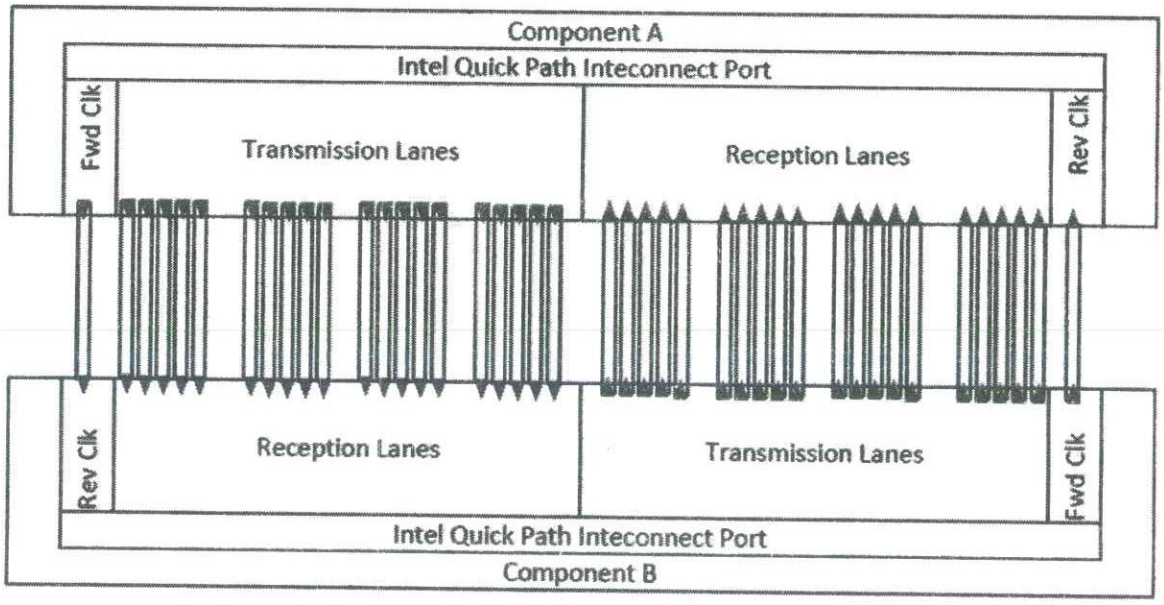

Figure Q3b: Physical Interface of Intel Quick Path Interconnect

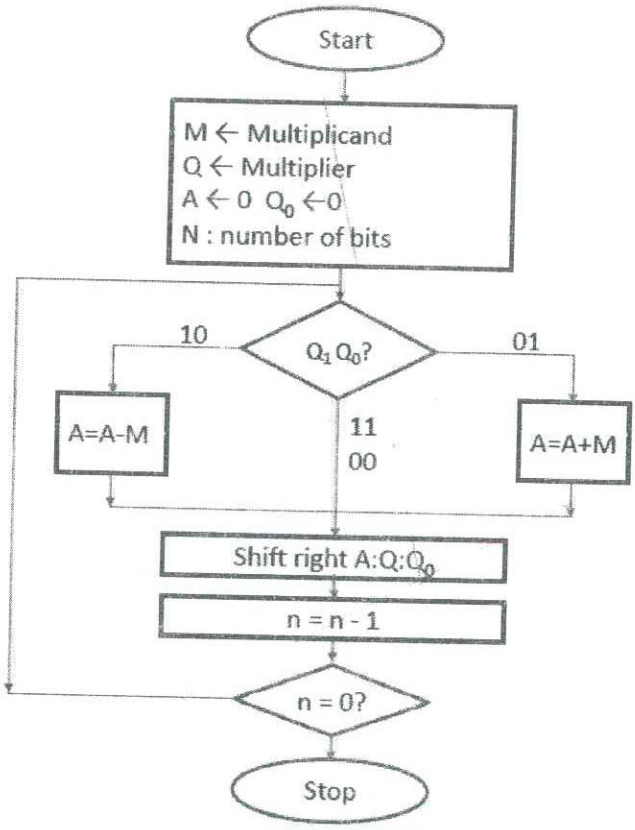

Figure Q4a: Booth's Algorithm for Multiplication

n	A	Q_4 Q_3 Q_2 Q_1	Q_0	M

Figure Q4b: Template of the calculation

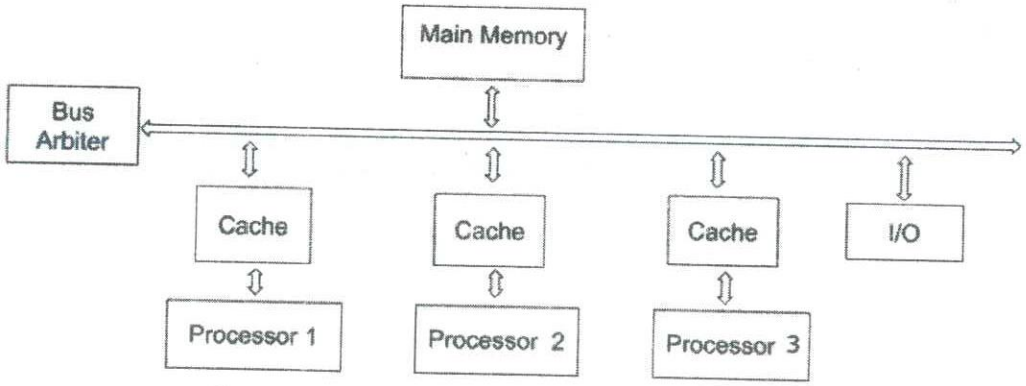

Figure Q4c: Symmetric multiprocessor system