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| --- | --- | --- | --- |
| **Instruction** | **Opcode** | **Operand (16 bit)** | **Operation** |
| loadac | 0000 0100 | - | ac <= DM[ac] |
| movacr | 0000 1000 | - | r <= ac |
| movacr1 | 0000 1001 | - | r1 <= ac |
| movacr2 | 0000 1010 | - | r2 <= ac |
| movacr3 | 0000 1011 | - | r3 <= ac |
| movacr4 | 0000 1100 | - | r4 <= ac |
| movacr5 | 0000 1101 | - | r5 <= ac |
| movacdar | 0000 1110 | - | dar <= ac |
| movrac | 0000 1111 | - | ac <= r |
| movr1ac | 0001 0000 | - | ac <= r1 |
| movr2ac | 0001 0001 | - | ac <= r2 |
| movr3ac | 0001 0010 | - | ac <= r3 |
| movr4ac | 0001 0011 | - | ac <= r4 |
| movr5ac | 0001 0100 | - | ac <= r5 |
| movdarac | 0001 0101 | - | ac <= dar |
| stac | 0001 0110 | - | DM[ac] <= ac |
| add | 0001 1001 | - | ac <= ac + r |
| sub | 0001 1011 | - | ac <= ac – r |
| lshift | 0001 1101 | - | ac <= r << ac |
| rshift | 0001 1111 | - | ac <= r >> ac |
| incac | 0010 0001 | - | ac <= ac + 1 |
| incdar | 0010 0010 | - | dar <= dar +1 |
| incr1 | 0010 0011 | - | r1 <= r1 +1 |
| incr2 | 0010 0100 | - | r2 <= r2 +1 |
| incr3 | 0010 0101 | - | r3 <= r3 + 1 |
| loadim | 0010 0110 | imm | ac <= imm |
| jumpz | 0010 1001 | imm | if z == 1, go to instruction IM[imm] |
| jumpnz | 0011 0000 | imm | if z == 0, go to instruction IM[imm] |
| jump | 0011 0001 | imm | go to instruction IM[imm] |
| nop | 0011 0010 | - | no operation |
| endop | 0011 0011 | - | end process |