COMP262-01 LAB3 CH12.4-PROCESSOR STRUCTURE/FUNCTION PIPELINE Execution Performance and Analysis

A certain Processor has the following relevant specs:

Clock cycle: 1 time unit

Pipelined: yes Pipeline Stages: 6

Assume that the **Pipeline STAGES** are **NOT** all of equal duration, with the following values

per stage duration: FI, FO, WO = 3 cycles, EI = 2 cycles, DI, CO = 1 cycle.

Memory access: **MULTIPLE PORTS**, thus allowing for multiple memory access operations to occur

(overlap), per clock cycle.

Instructions: assume ALL instructions go through ALL stages, stalling (causing a pipeline bubble) if necessary

Registers: N/A Cache: N/A Bus: N/A

Given the following program segment written in (a certain) Assembly language:

```
SUB A, B, C
                             (subs operand B from A and stores result in operand C)
        SUB D, E, F
        SUB G, H, I
                             (branches, conditionally, to 'location' if the 'negative' status flag is on)
        BRNEG ISNEG
        SUB J. K. L
        SUB M, N, O
        SUB P, Q, R
        BR CONT
                             (branches, unconditionally, to 'location')
ISNEG: SUB S, T, U
        SUB V, W, X
        SUB Y, Z, AA
CONT: NOOP
                             (no operation, place holder)
```

1) Assume that the CONDITIONAL BRANCH **IS** TAKEN.

Complete the provided MS-EXCEL BOOK, LAB3, sheet1 by filling out the rows (instructions) with the six stages.

```
Given the following program segment written in (a certain) Assembly language:
BEG:
        SUB A, B, C
                             (subs operand B from A and stores result in operand C)
        SUB D. E. F
        SUB G, H, I
        BRNEG ISNEG
                              (branches, conditionally, to 'location' if the 'negative' status flag is on)
        SUB J, K, L
        SUB M, N, O
        SUB P, Q, R
        BR BEG
                             (branches, unconditionally, to 'location')
ISNEG: SUB S, T, U
        SUB V, W, X
        SUB Y, Z, AA
        BR BEG
                             (branches, unconditionally, to 'location')
```

2) Assume that the conditional branch (BRNEG) occurs (the branch takes) 20% of the time(one out of five). **SHOW ALL THE STEPS NEEDED TO CALCULATE** the 'AVERAGE' TOTAL number of cycles used by the pipelining, assuming that the code segment (LOOP) is executed 10 times... i.e.: 20% at X cycles + 80% at Y cycles. Use the provided MS-EXCEL BOOK, LAB3, sheet2 and paste the calculations and result on sheet3.

NOTE: because the number of instructions is RELATIVELY small, DO NOT DISMISS/DISREGARD the initial filling and emptying of the pipeline...