COMP262-01 LAB2-2 CH12.4

PROCESSOR STRUCTURE/FUNCTION

PIPELINE Execution Performance and Analysis

A certain Processor has the following relevant specs:
Clock cycle: 1 time unit
Pipelined: yes
Pipeline Stages: 6, assume all stages are of equal duration, and that each stage takes 1 Clock cycle
Stage actions: FI, DI, CO, FO, EI, WO (see textbook page 446 for descriptions)
Memory access: **MULTIPLE PORTS**, thus allowing for multiple memory access operations to occur (overlap), per clock cycle.
Instructions: assume ALL instructions go through ALL stages, stalling (causing a pipeline bubble) if necessary
Registers: N/A
Cache: N/A
Bus: N/A

Given the following program segment written in (a certain) Assembly language:

```
        OR  A, B, C          (C=A or B)
        OR  D, E, F
        OR  G, H, I
        OR  J, K, L
        BRNEG  ISNEG         (conditional branch)
        OR  M, N, O
        XOR  P, Q, R
        XOR  V, W, X
        OR  Y, Z, AA
        NAND BB, CC, DD
        BR  CONT             (unconditional branch)
ISNEG: OR  S, T, U
        OR  V, W, X
        OR  Y, Z, AA
        XOR  XX, ZZ, BB
        XOR  WW, ZZ, AA
CONT:  ADD A, B, C
```

1) Assume that the CONDITIONAL BRANCH IS **NOT** TAKEN.
   Complete the provided MS-EXCEL BOOK, LAB2-2, sheet1 by filling out the rows (instructions) with the six stages.

2) Assume that the CONDITIONAL BRANCH **IS** TAKEN.
   Complete the provided MS-EXCEL BOOK, LAB2-2, sheet2 by filling out the rows (instructions) with the six stages.