COMP262-01, LAB2-1 CH12.4
PROCESSOR STRUCTURE/FUNCTION
PIPELINE Execution Performance and Analysis

A certain Processor has the following relevant specs:
Clock cycle: 1 time unit
Pipelined: yes
Pipeline Stages: 6, assume all stages are of equal duration, and that each stage takes 1 Clock cycle
Stage actions: FI, DI, CO, FO, EI, WO (see textbook page 446 for descriptions)
Memory access**: SINGLE PORT, thus only one memory access operation can occur per clock cycle**
Instructions: assume ALL instructions go through ALL stages, stalling (causing a pipeline bubble) if necessary
Registers: N/A
Cache: N/A
Bus: N/A

Given the following program segment written in (a certain) Assembly language:
(operands are 1st and 2nd vars, the result is stored in the 3rd var…C=A and B)

```
AND A, B, C
OR  D, E, F
AND G, H, I
OR  J, K, L
AND M, N, O
OR  P, Q, R
```

Complete the provided MS-EXCEL BOOK-LAB2-1, sheet1 by filling out the rows (instructions) with the six stages.
IF your first reaction is: piece of cake! and proceed to mimic the entry in Fig 12.10, **STOP!** You did not read the above specs carefully! If anything, it will look more like Fig 12.16…Consider/reread the textbook description of the assumptions made in Fig.12.10 and HOW they may differ from those stated here,

considering hazards…

Repeat, this time completing the provided MS-EXCEL BOOK-LAB2-1, sheet2 for the following program segment and again **considering hazards:**

```
NAND A, B, C
OR   D, E, F
NOR  E, F, G
XOR  H, I, G
AND  I, J, K
NAND K, L, K
```