Assume the use of a four-stage pipeline: fetch, decode/issue, execute, write back.
Assume that all pipeline stages take one clock cycle, except for the execute stage, which also takes one cycle for simple integer arithmetic and logical instructions, but takes 5 cycles for a LOAD from memory instruction.

Consider the following sequence of instructions, where the syntax consists of an opcode followed by the destination register, followed by one or two source registers:

```
0 ADD R3, R1, R2        R3=R1 + R2
1 LOAD R6, [R3]
2 AND R7, R5, 3
3 ADD R1, R6, R0
4 SRL R7, R0, 8
5 OR R2, R4, R7
6 SUB R5, R3, R4
7 ADD R0, R1, R10
8 LOAD R6, [R5]
9 SUB R2, R1, R6
10 AND R3, R7, 15
```

---

1) Assume NO out-of-order execution capability.
   Complete the provided MS-EXCEL BOOK, LAB5-1-template, sheet1 by filling out the rows (instructions) with the four stages.

2) Assume out-of-order execution capability.
   Complete the provided MS-EXCEL BOOK, Lab5-1-template, sheet2 by filling out the rows (instructions) with the four stages.

DELIVERABLE:
When completed, upload the (LAB5-1-template).