COMP262-SPRING17 REVIEW for MT1 Thursday March 16

The Mid Term Assessment will consult the student's understanding of the material covered.
There is nothing to MEMORIZE, since this is an open book/material type of assessment, which evaluates the skills that a student has acquired by presenting PROBLEM style Items to be completed.
Remember:
SHORT TERM MEMORY(disposable)=HISTORY EXAMS;
LONG TERM MEMORY(permanent)=SCIENCE EXAMS…..
The student will be asked to ANALYZE a situation and apply both QUALITATIVE and QUANTITATIVE skills in providing answers.
From past semesters, we know that the number of items to be tackled can be handled by a large percentage of the students, within 1:30 to 2:00 hours.

Inevitable, the student will ask: WHAT WILL BE IN THE TEST? HOW DO I PREPARE FOR IT?
WILL YOU PROVIDE A STUDY GUIDE?
We respond by indicating that we will be consulting the degree of skills/understanding that the student has achieved in their study of the material presented and the completed assigned work.
What would be an effective/productive use of the meager time that a student may realistically have?
Review assigned study material guided by the lecture review presentations.
Review/Complete: assigned HW's, LABS, PROJECT1(all Parts)…
Think about what variations on those themes could be thought of and presented to the student…

More specifically, the items in the MT1 will address among other areas:

Lab 1
A properly configured/balanced system. Making changes to one component HOW does it affect the rest.
The relationships between the different components of the system: the CPU, the BUS and Memory.
How do the different components of the CPU(registers) relate to the BUS paths and the Memory unit of transfer. Given the size of certain components, determine the corresponding size of other related components.

Lab 2/3
The Instruction cycles and how they are handled when implementing a pipeline.
The different Hazards present in a pipeline and the effect it has on the pipeline performance.
Calculations/Timings for a given instruction mix involving Hazards in a Pipeline.

Lab 4
The relationship between a CISC vs a RISC machine. The concept of Register Renaming/Reuse and Instruction elimination.

Lab 5
The concept of parallelism, both the Program and the Hardware relationship and how to rearrange an instruction sequence to take advantage of hardware parallelism.
The Superscalar implementation using multiple pipelines and multiple execution units to implement instruction parallelism.
Implementing other PEP8 addressing modes(stack related) in the manner done for the chosen subset in the CO() method of the CPU project. Implementing 'new' PEP9 instructions.
Implementing a sequence of operation for the CU, using RTL as done in LAB6.

In addition, please brush up on your Algebra for the type of questions/problems that may involve, for example, the composition/mix of Instruction type sizes and their Memory access time…

Beyond that, there is no meaningful cramming/catch up possible at this point, since all the material has been progressive and cumulative and stored as patterns to use in order to recognize and solve similar problems; thus the assessment is meant for YOU THE STUDENT to gauge for yourself, YOUR level of comprehension and skills achieved up to this point….RELAX and all will be well……