Assume the use of a superscalar pipeline with decoupled F/D(fetch/decode) and Execute unit(s) .
Assume that the Execution stage takes one clock cycle for ALU instructions, and **3 cycles** for the LOAD/STORE memory operations.
Assume that we have a buffer with a certain number of instructions that have been fetched and decoded.
Assume that the superscalar pipeline allows for **OUT-of-ORDER execution**.

Consider the following sequence of instructions, where the syntax consists of an opcode followed by:
a) for the load/store instructions, the destination register, followed by the variable name and
b) for all other ALU instructions, the destination register, followed by two source registers

```
LOAD Ra, A
LOAD Rc, C
ADD  R1, Ra, Rc
LOAD Rb, B
LOAD Rd, D
SUB  R2, Rb, Rd
MUL  R12, R1, R2
ADD  R3, Ra, Rb
SUB  R4, Rc, Rd
MUL  R34, R3, R4
DIV  RX, R12, R34
STORE RX, X
```

For all three cases that follow, complete the provided MS-EXCEL BOOK, LAB5-2-template, sheet1 by filling out the rows (instructions) with **ONLY THE EXECUTION STAGE TIMING SHOWN**.

1) Assume a simple superscalar implementation with only ONE Execution Unit.
2) Assume a superscalar implementation with TWO Execution Units.
3) Assume a superscalar implementation with FOUR Execution Units.

DELIVERABLE:
When completed, upload the (LAB5-2-template).