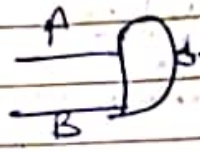
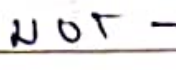
Electronics

A-1

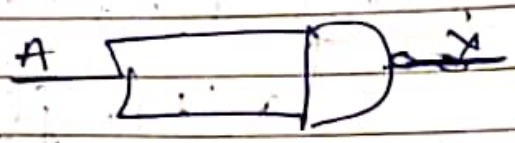
Part-2

Y-1 (a) NAND → 

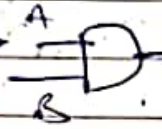
$Y = \overline{A \cdot B} = \bar{A} + \bar{B}$

NOT → 

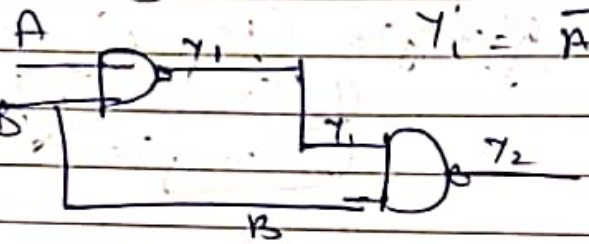
$Y = \bar{A}$



$Y = \overline{A \cdot A} = \overline{A^2} = \bar{A}$.

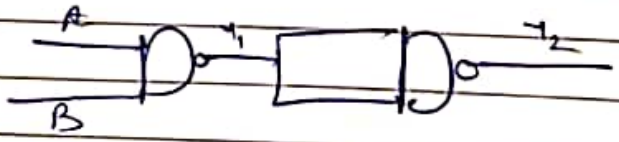
(b) AND → 

$Y = A \cdot B$



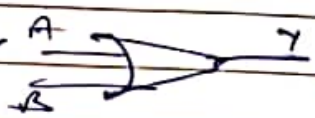
$Y_1 = \overline{A \cdot B}$

$Y_2 = \overline{\overline{AB} \cdot B} = AB + \bar{B}$

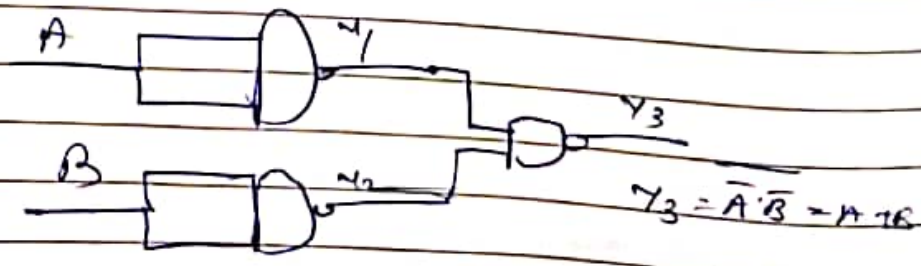


$Y_1 = \overline{AB}$ $Y_2 = \overline{\overline{AB} \cdot \overline{AB}}$

$Y_2 = AB + AB = AB$.

(c) OR → 

$Y = A + B$



$Y_3 = \overline{\bar{A} \cdot \bar{B}} = A + B$

$Y_1 = \bar{A}$ $Y_2 = \bar{B}$

M-2 (a)

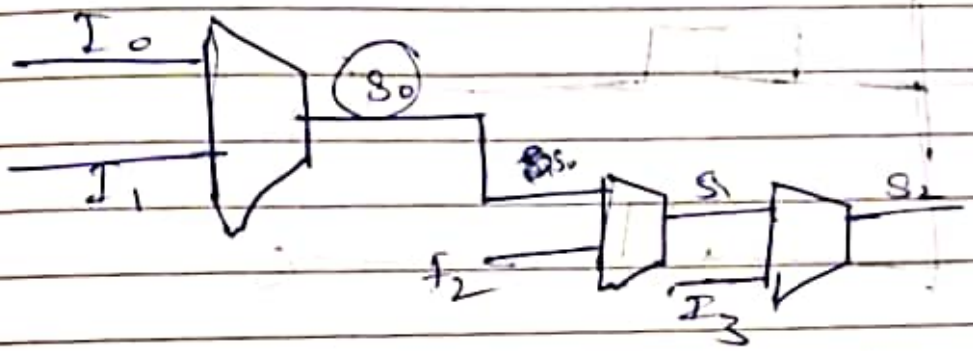
A	B	S	C
0	1	1	0
1	0	1	0
0	0	0	0
1	1	0	1

(b) $C = AB$

$S = \bar{A}B + \bar{B}A$

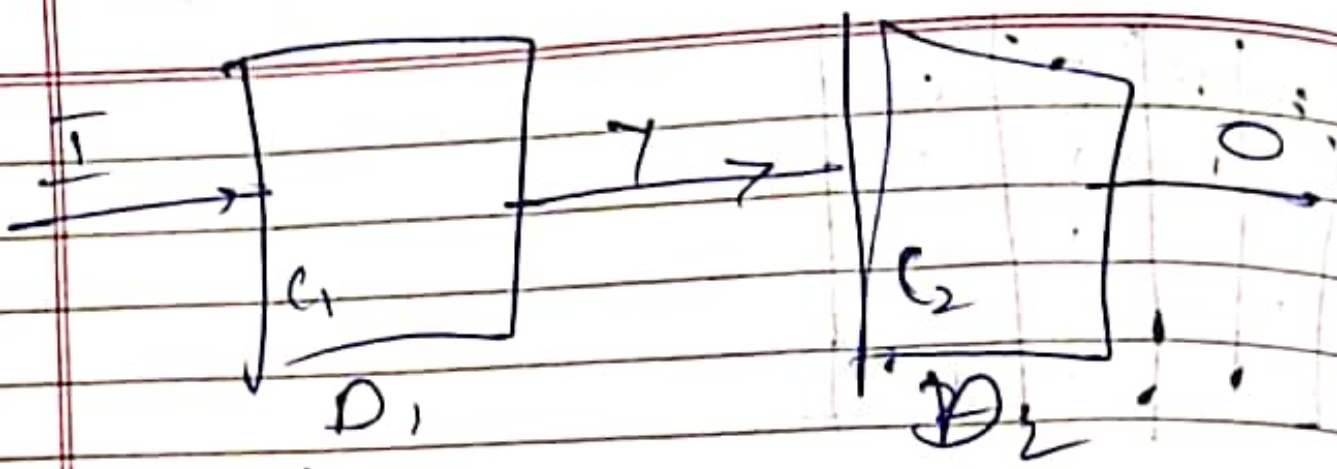
(c) For S - XOR ∴ For C → AND.

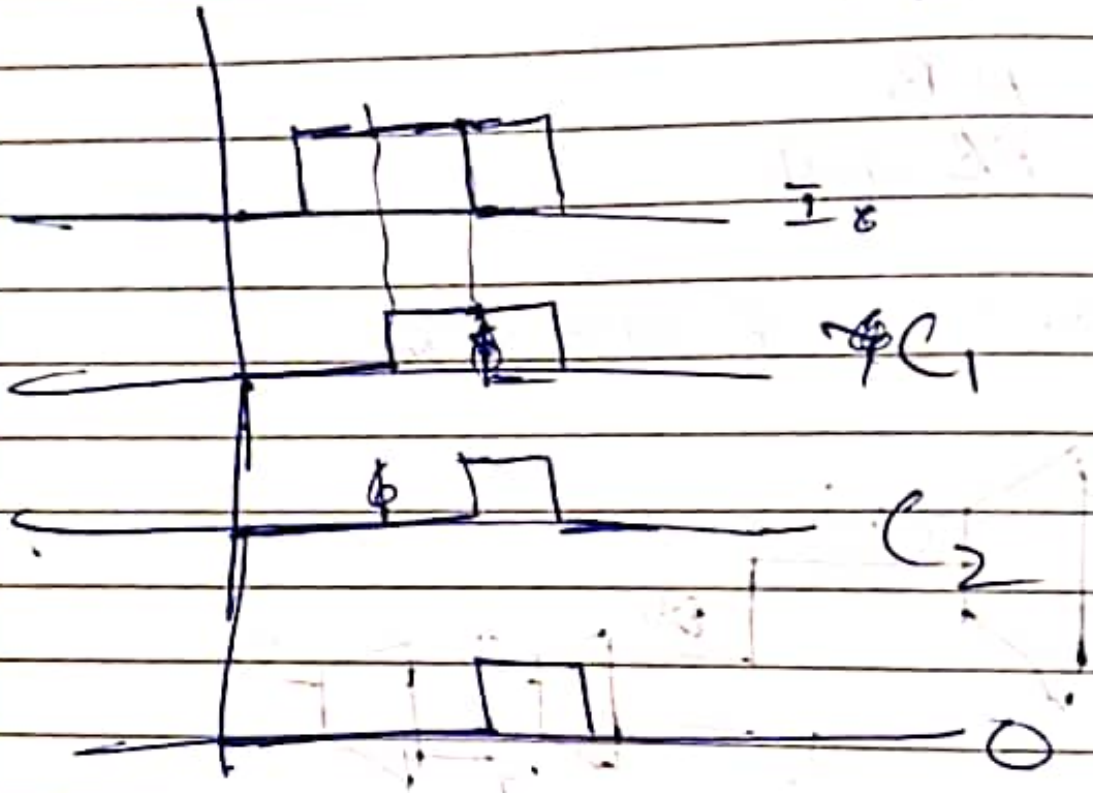
M-3



M-4 M-5

(a) 2 flip flops as when 1 first come it get stored & when 2nd 1 come then we allow the clock timing to release that 1 to another flip flop and then 3rd 1 come then we allow 2nd flip flop to release which gave output 1





M-5