



DynamicFifo Product User Guide

rocksavagetech.chiselWare.DynamicFifo

IPF certified to level: 0 of 5



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September 28, 2024

Contents

1	Errata and Known Issues	3
1.1	Errata	3
1.2	Known Issues	3
2	Port Descriptions	4
2.1	GPIO Interface	4
2.2	APB3 Interface	4
3	Parameter Descriptions	5
4	Theory of Operations	6
4.1	Introduction	6
4.2	Interface Timing	7
5	Simulation	8
5.1	Tests	8
5.2	Code coverage	8
5.3	Running simulation	8
6	Synthesis	9
6.1	Area	9
6.2	SDC File	9
6.3	Timing	9
6.4	Multicycle Paths	9

1 Errata and Known Issues

1.1 Errata

- Care should be taken in creating instances of **DynamicFifo** with internal very large memory (hundreds or thousands of memory cells) as this can generate very large designs. There is currently no checks or constraints on users from doing this.
- Care should be taken regarding dynamically changing the values on the *almostEmptyLevel* and *almostFullLevel* ports when the FIFO is not empty as that may result in unpredictable behaviors on the *almostEmpty* and *almostFull* flags.

1.2 Known Issues

None.

2 Port Descriptions

2.1 GPIO Interface

The ports for **GPIO** are shown below in Table 1. The width of several ports is controlled by the following input parameters:

dataWidth is the width of the gpioInput, gpioOutput, and gpioOutputEnable ports in bits

Port Name	Width	Direction	Description
gpioInput	<i>dataWidth</i>	Input	Data to be sent to the GPIO
gpioOutput	<i>dataWidth</i>	Output	Data to be recieved from the GPIO
gpioOutputEnable	<i>dataWidth</i>	Output	Enable data to be recieved from the GPIO

Table 1: GPIO Ports Descriptions

2.2 APB3 Interface

The **APB3 Interface** is a regular APB3 Slave Interface. All signals supported are shown below in Table 2. See the *AMBA APB Protocol Specifications* for a complete description of the signals. The width of several ports is controlled by the following input parameters:

- *PDATA_WIDTH* is the width of PWDATA and PRDATA in bits
- *PADDR_WIDTH* is the width of PADDR in bits

Port Name	Width	Direction	Description
PCLK	1	Input	Positive edge clock
PRESETN	1	Input	Active low reset
PSEL	1	Input	Indicates slave is selected and a data transfer is required
PENABLE	1	Input	Indicates second cycle of APB transfer
PWRITE	1	Input	Indicates write access when HIGH and read access when LOW
PADDR	<i>PADDR_WIDTH</i>	Input	Address bus
PWDATA	<i>PDATA_WIDTH</i>	Input	Write data bus driven when PWRITE is HIGH
PRDATA	<i>PDATA_WIDTH</i>	Output	Read data bus driven when PWRITE is LOW
PREADY	1	Output	Transfer ready
PSLVERR	1	Output	Transfer error

Table 2: APB Ports Descriptions

3 Parameter Descriptions

The parameters for **GPIO** are shown below in Table 3.

Name	Type	Min	Max	Description
dataWidth	Int	1	≥ 1	The data width of GPIO ports
PADDR_WIDTH	Int	1	≤ 32	The APB address bus width
PDATA_WIDTH	Int	8	≤ 32	The APB PWDATA and PRDATA bus width. Can be 8, 16, or 32 bits wide

Table 3: Parameter Descriptions

The DynamicFifo is instantiated into a design as follows:

```
// Instantiate small FIFO using internal flip-flops
val mySmallFifo = new DynamicFifo(
    externalRAM = false ,
    dataWidth = 8 ,
    fifoDepth = 16)

// Instantiate large FIFO using external SRAM
val myLargeFifo = new DynamicFifo(
    externalRAM = true ,
    dataWidth = 32 ,
    fifoDepth = 512)
```

4 Theory of Operations

4.1 Introduction

The **DynamicFifo** is a highly parameterized FIFO and FIFO controller. It is configurable as a full self-contained FIFO with internal memory being constructed from flip-flops, or a FIFO controller that uses an external SRAM for memory.

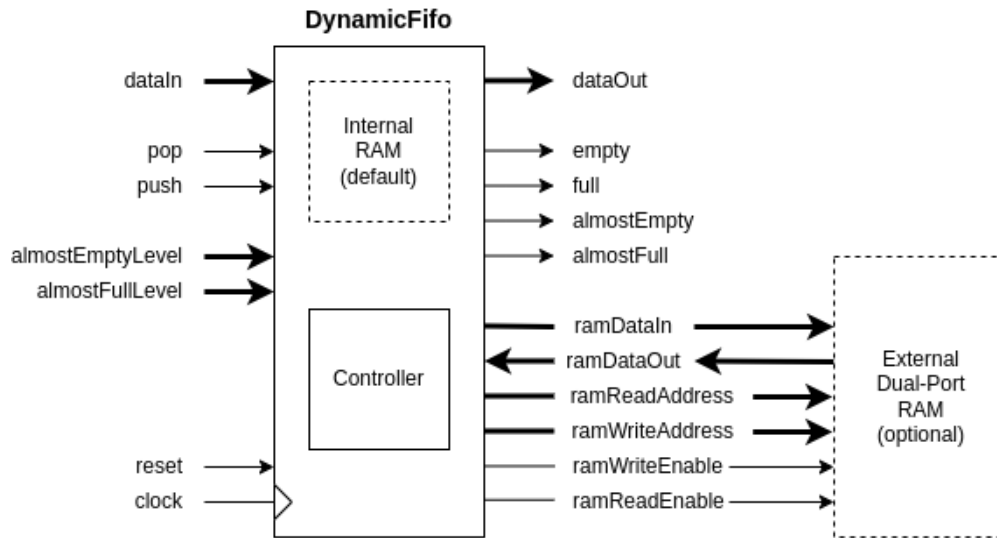


Figure 1: Block Diagram

It features the following status flags which are described in Table 1.

- `empty`
- `full`
- `almostEmpty`
- `almostFull`

When *push* is asserted, the data on the *dataIn* port is enqueued on the next rising edge of *clock*. When *pop* is asserted, the top of the FIFO is dequeued and immediately available on the *dataOut* port. Pop and Push operations can be simultaneous.

There are two error conditions which produce the following effects:

- When *pop* is asserted and the FIFO is empty (*empty* is active), *dataOut* will contain the last valid data held in the FIFO.
- When *push* is asserted and the FIFO is full (*full* is active), *dataIn* will be ignored and not enqueued.

The *almostEmpty* and *almostFull* flags allow for additional feedback to the system that is useful for optimizing data flow control. The levels of these flags can be programmed dynamically through the *almostEmptyLevel* and *almostFullLevel* ports.

4.2 Interface Timing

DynamicFifo has a simple, synchronous interface. The timing diagram shown below in Figure 2 represents an instantiation with the following parameters.

```
val myFifo = new DynamicFifo(
  externalRAM = true,
  dataWidth = 16,
  fifoDepth = 5)
```

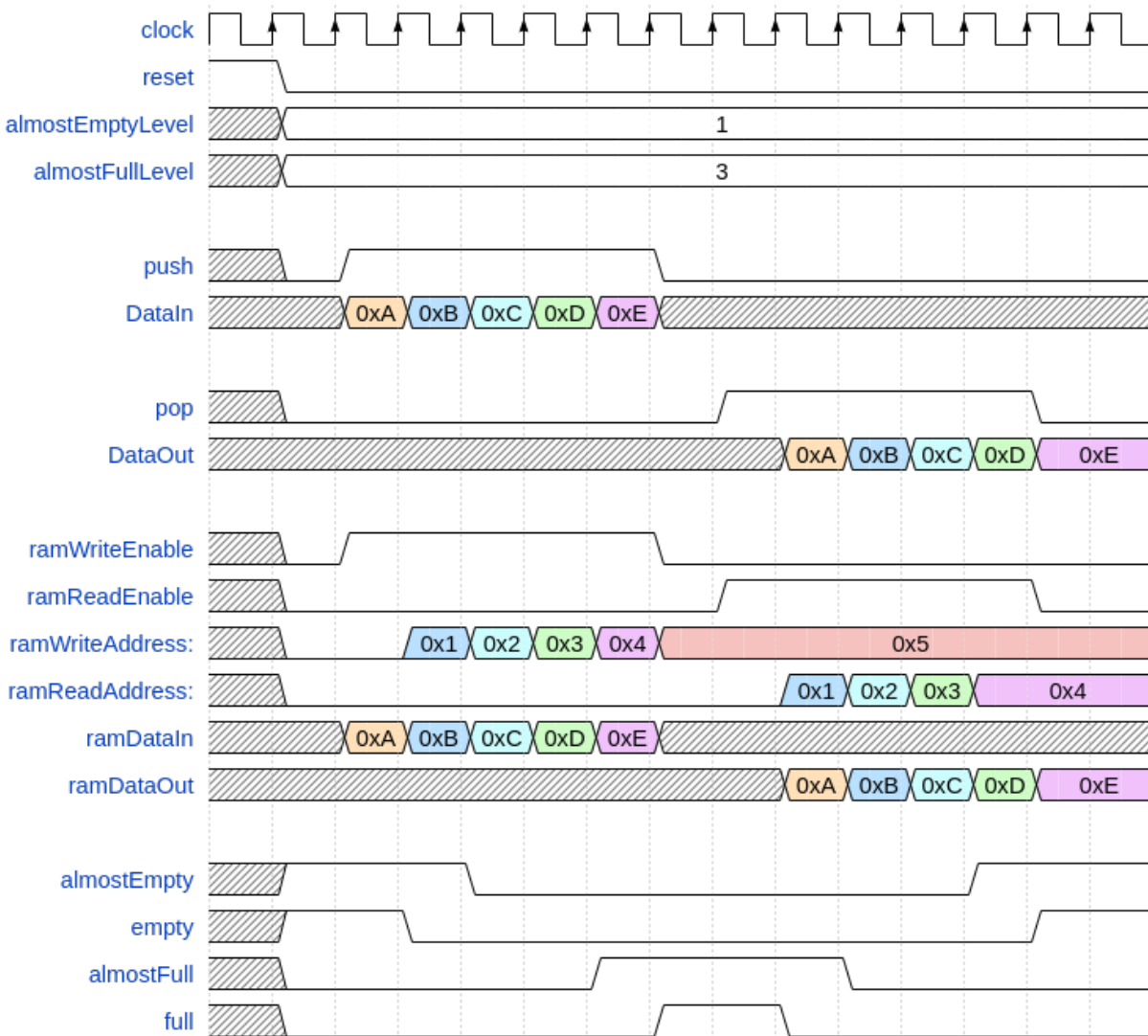


Figure 2: Timing Diagram

The *almostEmptyLevel* port is driven by external logic to a static value of 1 after reset and the *almostFull* port is driven to 3.

Beginning in the third clock cycle, 5 words of data are pushed into the FIFO. The status flags show the FIFO going from empty to full.

The FIFO is then fully emptied when the *pop* port is held high for 5 clock cycles. The status flags show the FIFO going from full to empty again.

5 Simulation

5.1 Tests

The test bench generates a number (default is 50) configurations of the DynamicFifo that are highly randomized. There are two flavors of tests:

- Directed tests that fill the FIFO with random data and then read back the results to verify that the read data matches the writted data.
- Lengthy random tests that are used to check odd combinations of configurations and to compile code coverage data.

5.2 Code coverage

All inputs and outputs are checked to insure each toggle at least once. An error will be thrown in case any port fails to toggle.

The only exception are the *almostEmptyLevel* and *almostFullLevel* which are intended to be static during each simulation. These signals are excluded from coverage checks.

5.3 Running simulation

Simulations can be run directly from the command prompt as follows:

```
$ sbt "test"
```

or from make as follows:

```
$ make test
```


6 Synthesis

6.1 Area

The DynamicFifo has been tested in a number of configurations and the following results should be representative of what a user should see in their own technology.

Config Name	externalRAM	dataWidth	fifoDepth	Gates
small_false_8_8	false	8	8	769
medium_false_32_64	false	32	64	19,283
large_false_64_256	false	64	256	152,808
small_true_64_256	true	64	256	355
medium_true_128_128	true	128	128	477
large_true_256_2048	true	256	2048	502

Table 4: Synthesis results

6.2 SDC File

An `.sdc` file is generated to provide synthesis and static timing analysis tools guidance for synthesis.

The `DynamicFifo.sdc` file is emitted and found in the `./syn` directory.

6.3 Timing

The following timing was extracted using the generated `.sdc` files using the Nangate 45nm free library.

Config Name	Period	Duty Cycle	Input Delay	Output Delay	Slack
small_false_8_8	5ns	50%	20%	20%	2.93 (MET)
medium_false_32_64	5ns	50%	20%	20%	2.69 (MET)
large_false_64_256	5ns	50%	20%	20%	2.80 (MET)
small_true_64_256	5ns	50%	20%	20%	2.80 (MET)
medium_true_128_128	5ns	50%	20%	20%	2.70 (MET)
large_true_256_2048	5ns	50%	20%	20%	2.77 (MET)

Table 5: Static Timing Analysis results

6.4 Multicycle Paths

None.