GPIO
Product User Guide

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IPF certified to level: **0** of 5

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Contents

1 Errata and Known Issues

1.1 Errata

- Care should be taken in creating instances of **DynamicFifo** with internal very large memory (hundreds or thousands of memory cells) as this can generate very large designs. There is currently no checks or constraints on users from doing this.
- Care should be taken regarding dynamically changing the values on the *almostEmptyLevel* and *almostFullLevel* ports when the FIFO is not empty as that may result in unpredictable behaviors on the *almostEmpty* and *almostFull* flags.

1.2 Known Issues

None.

2 Port Descriptions

2.1 GPIO Interface

The ports for **GPIO** are shown below in Table 1. The width of several ports is controlled by the following input parameters:

dataWidth is the width of the gpioInput, gpioOutput, and gpioOutputEnable ports in bits

Port Name	**Width**	**Direction**	**Description**
gpioInput	*dataWidth*	Input	Data to be sent to the GPIO
gpioOutput	*dataWidth*	Output	Data to be recieved from the GPIO
gpioOutputEnable	*dataWidth*	Output	Enable data to be recieved from the GPIO
irqOutput	1	Output	Sent when interrupt is triggered on the GPIO

Table 1: GPIO Ports Descriptions

2.2 APB3 Interface

The **APB3 Interface** is a regular APB3 Slave Interface. All signals supported are shown below in Table 2. See the *AMBA APB Protocol Specifications* for a complete description of the signals. The width of several ports is controlled by the following input parameters:

- *dataWidth* is the width of PWDATA and PRDATA in bits
- *addrWidth* is the width of PADDR in bits

Port Name	**Width**	**Direction**	**Description**
PCLK	1	Input	Positive edge clock
PRESETN	1	Input	Active low reset
PSEL	1	Input	Indicates slave is selected and a data transfer is required
PENABLE	1	Input	Indicates second cycle of APB transfer
PWRITE	1	Input	Indicates write access when HIGH and read access when LOW
PADDR	*addrWidth*	Input	Address bus
PWDATA	*dataWidth*	Input	Write data bus driven when PWRITE is HIGH
PRDATA	*dataWidth*	Output	Read data bus driven when PWRITE is LOW
PREADY	1	Output	Transfer ready
PSLVERR	1	Output	Transfer error

Table 2: APB Ports Descriptions

3 Parameter Descriptions

The parameters for **GPIO** are shown below in Table 3.

Name	**Type**	**Min**	**Max**	**Description**
dataWidth	Int	1	≤ 32	The data width of GPIO ports, PWDATA, and PRDATA. Can be 8, 6, or 32 bits wide
addrWidth	Int	1	≤ 32	The APB address bus width

Table 3: Parameter Descriptions

The GPIO is instantiated into a design as follows:

```
// Valid GPIO Instantiation Example
val myGPIO = new GPIO(
  dataWidth = 32,
  addrWidth = 32 )
```

4 Register Interface

When programming registers, each register starts on a byte address, and the last bits it would take up in its final byte based on its size are unused. To find the size in bytes for any register, divide by the register size, and round up to the nearest whole number. For example, a 32-bit register would take up 4 bytes, and a 1-bit register would take up 1 byte.

Name	**Size (Bits)**	**Description**
DIRECTION	dataWidth	DESC TODO
OUTPUT	dataWidth	DESC TODO
INPUT	dataWidth	DESC TODO
MODE	dataWidth	DESC TODO
ATOMIC_OPERATION	4	DESC TODO
ATOMIC_MASK	p.dataWidth	DESC TODO
ATOMIC_SET	1	DESC TODO
VIRTUAL_PORT_MAP	sizeOfVirtualPorts	DESC TODO
VIRTUAL_PORT_OUTPUT	numVirtualPorts	DESC TODO
VIRTUAL_PORT_ENABLE	1	DESC TODO
TRIGGER_TYPE	dataWidth	DESC TODO
TRIGGER_LO	dataWidth	DESC TODO
TRIGGER_HI	dataWidth	DESC TODO
TRIGGER_STATUS	dataWidth	DESC TODO
IRQ_ENABLE	dataWidth	DESC TODO

4.1 DIRECTION

DIRECTION is a *dataWidth* bits wide active-high read/write register. This register controls the output enable bus *gpioOutputEnable*. Operation can be seen in Table

DIRECTION[n]	**Direction**
0	Input
1	Output

Table 5: DIRECTION Register

4.2 OUTPUT

OUTPUT is a *dataWidth* bits wide read/write register. This register controls the output bus *gpioOutput*. Writing a '0' drives the pad low in both modes of operation. Writing a '1' drives the pad high in push-pull mode, or Hi-Z in open-drain mode.

4.3 INPUT

INPUT is a *dataWidth* bits wide read-only register. This register is written to from the input bus *gpioInput*. On the rising edge of the APB3 Bus Clock (PCLK), input data from *gpioInput* is synchronized using two flops and stored in the INPUT register. From there, it may be read via the APB3 Bus Interface through PRDATA.

4.4 MODE

MODE is a *dataWidth* bits wide read/write register. This register sets the operating mode for each bit of the *gpioOutput* and *gpioOutputEnable* busses as either push-pull or open drain mode. Operation can be seen in Table

MODE[n]	**Operating Mode**
0	Push-Pull
1	Open Drain

Table 6: MODE Register

4.5 TRIGGER_TYPE

TRIGGER_TYPE is a *dataWidth* bits wide read/write register. This register configures whether *gpioInput* is a level or edge sensitive interrupt trigger as seen below:

TRIGGER_TYPE[n]	**Type**
0	Level
1	Edge

Table 7: TRIGGER_TYPE Register

4.6 TRIGGER_LO

TRIGGER_LO is a *dataWidth* bits wide read/write register. This register configures whether the interrupt is triggered on a level low, or a falling edge, of *gpioInput* depending on how TRIGGER_TYPE is set. Operation can be see in Table:

TRIGGER_LO[n]	**Level Trigger**	**Edge Trigger**
0	No Trigger when Low	No Trigger on Falling Edge
1	Trigger when Low	Trigger on Falling Edge

Table 8: TRIGGER_LO Register

4.7 TRIGGER_HI

TRIGGER_HI is a *dataWidth* bits wide read/write register. This register configures whether the interrupt is triggered on a level high, or a rising edge, of *gpioInput* depending on how TRIGGER_TYPE is set. Operation can be see in Table:

TRIGGER_HI[n]	**Level Trigger**	**Edge Trigger**
0	No Trigger when High	No Trigger on Rising Edge
1	Trigger when High	Trigger on Rising Edge

Table 9: TRIGGER_HI Register

4.8 TRIGGER_STATUS

TRIGGER_STATUS is a *dataWidth* bits wide read/write register. This register sets a corresponding bit to '1' if a trigger condition is met on the corresponding *gpioInput[n]* according to the settings of TRIGGER_TYPE, TRIGGER_LO, and TRIGGER_HI.

TRIGGER_STATUS may be read on the PRDATA bus to determine if a trigger condition has occurred. Writing a '1' to TRIGGER_STATUS[n] will clear the status of the corresponding bit. If a new trigger is detected simulatenously during this write, the TRIGGER_STATUS[n] will remain set.

TRIGGER_STATUS[n]	**Status**
0	No Trigger Detected
1	Trigger Detected

Table 10: TRIGGER_STATUS Register

4.9 IRQ_ENABLE

IRQ_ENABLE is a *dataWidth* bits wide read/write register. This register determines if the *irqOutput* pin is asserted when a trigger condition occurs on the corresponding TRIGGER_STATUS[n]. IRQ_ENABLE is responsible for enabling interrupt generation from the GPIO core.

IRQ_ENABLE[n]	**Definition**
0	Disable IRQ Generation
1	Enable IRQ Generation

Table 11: IRQ_ENABLE Register

5 Virtual Ports

When a virtual port is mapped to a physical pin in your GPIO module, the behavior of the virtual port should directly correspond to the mode (input or output) of the physical pin it is mapped to. Here's a breakdown of how the virtual port should behave in each scenario:

1. Physical Pin Configured as Output

- **Data Flow**: When the physical pin is configured as an output, the virtual port should mirror the behavior of the physical pin in the output direction.
  - The virtual port **writes** data to the same physical pin.
  - Any **write** to the virtual port should directly translate into setting the output value of the physical pin.
  - The direction of the virtual port is **implicitly output**, since it is attached to a physical output pin.
- **Enable Behavior**: If virtual ports are supported and enabled, writing to the virtual port should behave as if you are writing directly to the physical pin.
  - The virtual port output should be enabled when the corresponding physical pin's output is enabled.

Example:

- Physical pin p is configured as an output.
- Virtual port v is mapped to pin p.
- Writing 1 to virtual port v should output 1 on physical pin p.

2. Physical Pin Configured as Input

- **Data Flow**: When the physical pin is configured as an input, the virtual port should reflect the data coming **from** the physical pin.
  - The virtual port can **read** the value of the physical pin but cannot write to it.
  - Any **read** from the virtual port should return the current value of the physical pin.
  - The virtual port direction is implicitly **input**, since it is attached to a physical input pin.
- **Enable Behavior**: If virtual ports are supported and enabled, reading from the virtual port should behave as if you are reading directly from the physical pin.
  - The virtual port input should be enabled when the physical pin's input is enabled.

Example:

- Physical pin p is configured as an input.
- Virtual port v is mapped to pin p.
- Reading from virtual port v should return the current state of physical pin p (either 0 or 1).

3. Physical Pin Reconfiguration (Dynamic Behavior)

- If the direction of the physical pin changes dynamically during runtime, the virtual port's behavior should immediately reflect this change.

  - If a physical pin switches from **input to output**, the virtual port should switch from **read-only** to **write-enabled**.
  - If a physical pin switches from **output to input**, the virtual port should switch from **write-enabled** to **read-only**.
- The virtual port should also respect any changes to the physical pin's enable signal (e.g., when a pin is disabled or tri-stated).

Summary of Correspondence

Physical Pin Mode	Virtual Port Behavior	Direction	Enable Be
Output	Writes to virtual port propagate to physical pin	Implicit Output	Enabled if physical pin
Input	Reads from virtual port reflect the physical pin value	Implicit Input	Enabled if physical pi

Additional Considerations

- **Virtual-to-Physical Map**: Ensure that your `virtualToPhysicalMap` correctly identifies which physical pin a virtual port is mapped to, and that this mapping remains consistent throughout the operation.
- **Enable Flag**: The virtual port enable flag should be checked to ensure that virtual ports are supported in the current configuration. If not enabled, virtual ports should not interact with physical pins at all.

By maintaining this mapping behavior, you can ensure that virtual ports act as an abstraction over physical pins, seamlessly extending the functionality of the GPIO without altering the underlying physical behavior.

6 Theory of Operations

6.1 Introduction

The **DynamicFifo** is a highly parameterized FIFO and FIFO controller. It is configurable as a full self-contained FIFO with internal memory being constructed from flip-flops, or a FIFO controller that uses an external SRAM for memory.

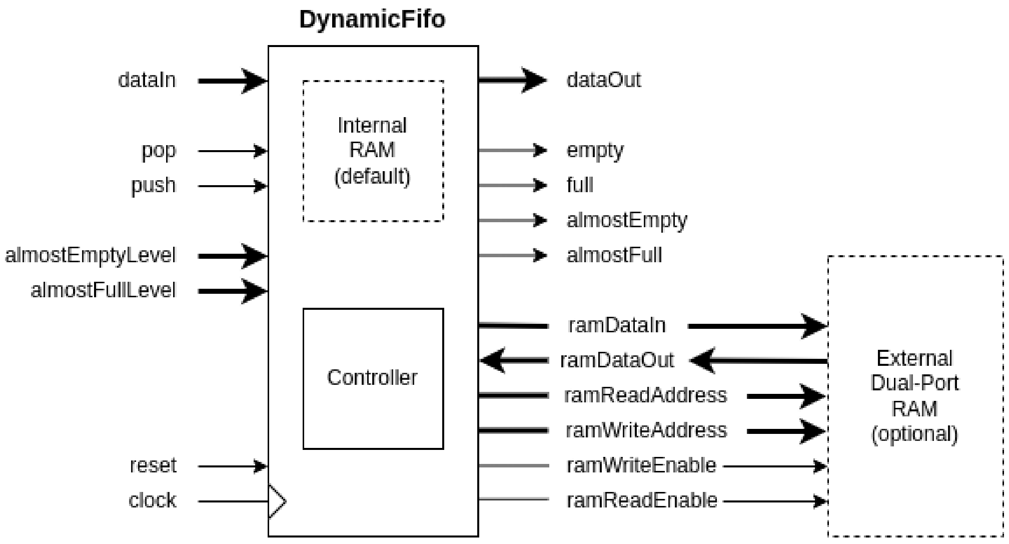

Figure 1: Block Diagram

It features the following status flags which are described in Table 1.

- empty
- full
- almostEmpty
- almostFull

When *push* is asserted, the data on the *dataIn* port is enqued on the next rising edge of *clock*. When *pop* is asserted, the top of the FIFO is dequed and immediately available on the *dataOut* port. Pop and Push operations can be simulataneous.

There are two error conditions which produce the following effects:

- When *pop* is asserted and the FIFO is empty (*empty* is active), *dataOut* will contain the last valid data held in the FIFO.
- When *push* is asserted and the FIFO is full (*full* is active), *dataIn* will be ignored and not enqued.

The *almostEmpty* and *almostFull* flags allow for additional feedback to the system that is useful for optimizing data flow control. The levels of these flags can be programmed dynamically through the *almostEmptyLevel* and *almostFullLevel* ports.

6.2 Interface Timing

DynamicFifo has a simple, synchronous interface. The timing diagram shown below in Figure 2 represents an instantiation with the following parameters.

```
val myFifo = new DynamicFifo(
  externalRAM = true,
  dataWidth = 16,
  fifoDepth = 5)
```

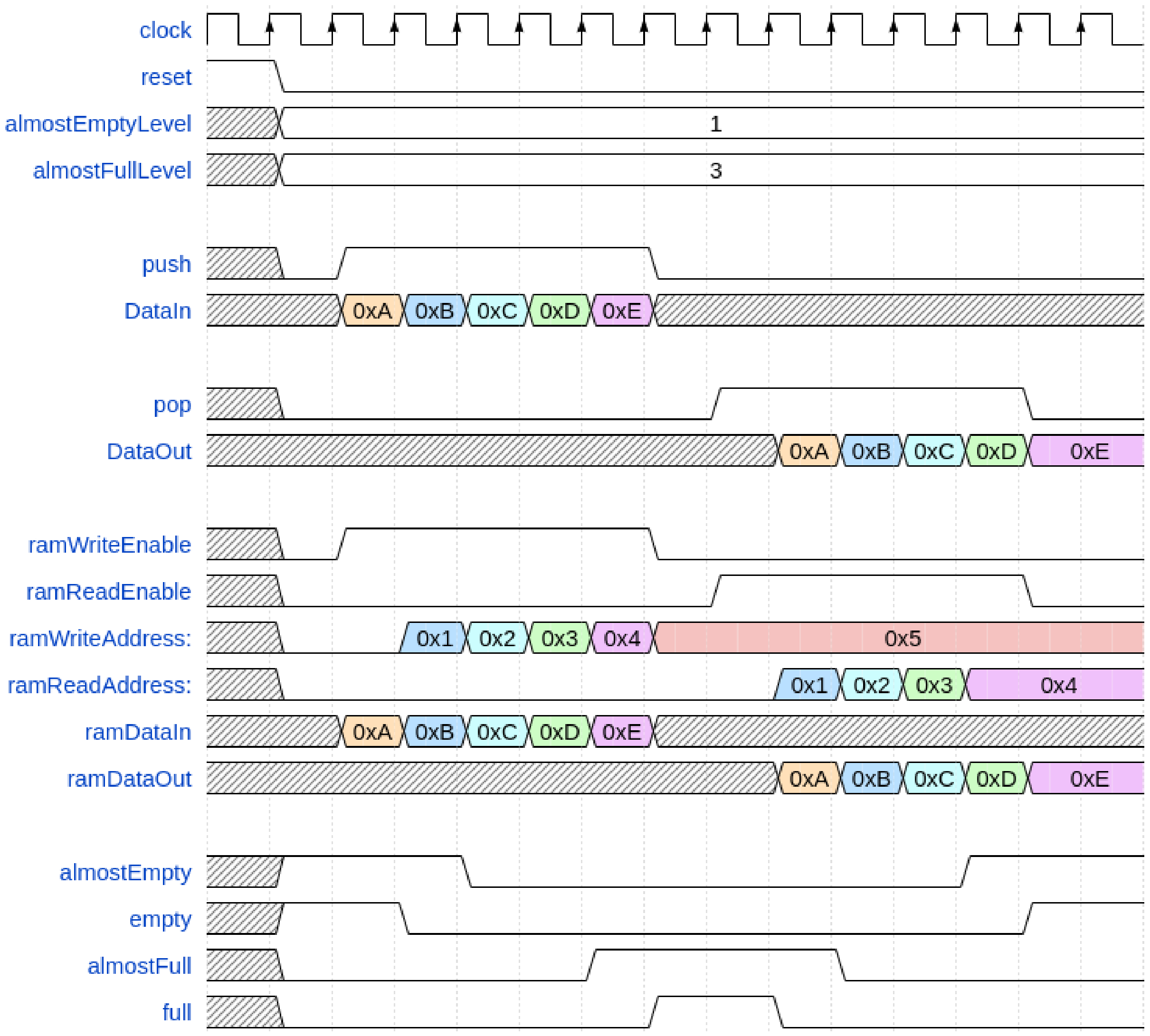

Figure 2: Timing Diagram

The *almostEmptyLevel* port is driven by external logic to a static value of 1 after reset and the *almostFull* port is driven to 3.

Beginning in the third clock cycle, 5 words of data are pushed into the FIFO. The status flags show the FIFO going from empty to full.

The FIFO is then fully emptied when the *pop* port is help high for 5 clock cycles. The status flags show the FIFO going from full to empty again.

7 Simulation

7.1 Tests

The test bench generates a number (default is 50) configurations of the DynamicFifo that are highly randomized. There are two flavors of tests:

- Directed tests that fill the FIFO with random data and then read back the results to verify that the read data matches the writted data.
- Lengthy random tests that are used to check odd combinations of configurations and to compile code coverage data.

7.2 Code coverage

All inputs and outputs are checked to insure each toggle at least once. An error will be thrown in case any port fails to toggle.

The only exception are the *almostEmptyLevel* and *almostFullLevel* which are intended to be static during each simulation. These signals are excluded from coverage checks.

7.3 Running simulation

Simulations can be run directly from the command prompt as follows:

```
  $ sbt "test"
```

or from make as follows:

```
$ make test
```

8 Synthesis

8.1 Area

The DynamicFifo has been tested in a number of configurations and the following results should be representative of what a user should see in their own technology.

Config Name	externalRAM	dataWidth	fifoDepth	Gates
small_false_8_8	false	8	8	769
medium_false_32_64	false	32	64	19,283
large_false_64_256	false	64	256	152,808
small_true_64_256	true	64	256	355
medium_true_128_128	true	128	128	477
large_true_256_2048	true	256	2048	502

Table 12: Synthesis results

8.2 SDC File

An `.sdc` file is generated to provide synthesis and static timing analysis tools guidance for synthesis.

The `DynamicFifo.sdc` file is emitted and found in the `./syn` directory.

8.3 Timing

The following timing was extracted using the generated .sdc files using the Nangate 45nm free library.

Config Name	Period	Duty Cycle	Input Delay	Output Delay	Slack
small_false_8_8	5ns	50%	20%	20%	2.93 (MET)
medium_false_32_64	5ns	50%	20%	20%	2.69 (MET)
large_false_64_256	5ns	50%	20%	20%	2.80 (MET)
small_true_64_256	5ns	50%	20%	20%	2.80 (MET)
medium_true_128_128	5ns	50%	20%	20%	2.70 (MET)
large_true_256_2048	5ns	50%	20%	20%	2.77 (MET)

Table 13: Static Timing Analysis results

8.4 Multicycle Paths

None.