指令	op	PCWre	ALU SrcA	ALU SrcB	DBDataSrc	RegWre	InsMemRW	mRD	mWR	RegDst	ExtSel	PCSRc[1]	PCSRc[0]	ALUOp
addiu	001001	1	0	1	0	!OF	1	X(0)	0	0	1	0	0	0000
addi	001000	1	0	1	0	1	1	X(0)	0	0	0	0	0	0000
andi	001100	1	0	1	0	1	1	X(0)	0	0	0	0	0	0100
ori	001101	1	0	1	0	1	1	X(0)	0	0	0	0	0	0011
xori	001110	1	0	1	0	1	1	X(0)	0	0	0	0	0	0111
lui	001111	1	0	1	0	1	1	X(0)	0	0	0	0	0	1001
slti	001010	1	0	1	0	1	1	X(0)	0	0	1	0	0	0110
sltiu	001011	1	0	1	0	1	1	X(0)	0	0	0	0	0	0101
sw	101011	1	0	1	X(1)	0	1	0	1	X(0)	X(0)	0	0	0000
lw	100011	1	0	1	1	1	1	1	0	0	1	0	0	0000
beq	000100	1	0	0	X(0)	0	1	X(0)	0	X(0)	1	0	zero	0001
bne	000101	1	0	0	X(0)	0	1	X(0)	0	X(0)	1	0	!zero	0001
bltz	000001	1	0	0	X(0)	0	1	X(0)	0	X(0)	1	0	sign	0000
j	000010	1	X(0)	X(1)	X(0)	0	1	X(0)	0	X(0)	X(1)	1	0	X (0000)
halt	111111	0	X(0)	X(1)	X(1)	0	1	X(0)	0	X(0)	X(0)	0	0	X (1000)

指令	func	PCWre	ALU SrcA	ALU SrcB	DBDataSrc	RegWre	InsMemRW	mRD	mWR	RegDst	ExtSel	PCSRc[1]	PCSRc[0]	ALUOp
add	100000	1	0	0	0	!OF	1	X(0)	0	1	X(1)	0	0	0000
sub	100010	1	0	0	0	!OF	1	X(0)	0	1	X(1)	0	0	0001
addu	100001	1	0	0	0	1	1	X(0)	0	1	X(1)	0	0	0000
subu	100011	1	0	0	0	1	1	X(0)	0	1	X(1)	0	0	0001
and	100100	1	0	0	0	1	1	X(0)	0	1	X(1)	0	0	0100
or	100101	1	0	0	0	1	1	X(0)	0	1	X(1)	0	0	0011
xor	100110	1	0	0	0	1	1	X(0)	0	1	X(1)	0	0	0111
nor	100111	1	0	0	0	1	1	X(0)	0	1	X(1)	0	0	1000
sll	000000	1	1	0	0	1	1	X(0)	0	1	X(1)	0	0	0010
srl	000010	1	1	0	0	1	1	X(0)	0	1	X(1)	0	0	1011
sra	000011	1	1	0	0	1	1	X(0)	0	1	X(1)	0	0	1010
sllv	000100	1	0	0	0	1	1	X(0)	0	1	X(1)	0	0	0010
srlv	000110	1	0	0	0	1	1	X(0)	0	1	X(1)	0	0	1011
srav	000111	1	0	0	0	1	1	X(0)	0	1	X(1)	0	0	1010
slt	101010	1	0	0	0	1	1	X(0)	0	1	X(1)	0	0	0110
sltu	101011	1	0	0	0	1	1	X(0)	0	1	X(1)	0	0	0101
jr	001000	1	0	X(0)	X(0)	0	1	X(0)	0	X(1)	X(1)	1	1	X (0110)

PCSrc[1..0]	00：pc<－pc+4，相关指令：add、addiu、sub、or、ori、and、andi、slti、sll、sw、lw、beq(zero=0)、bne(zero=1)、bltz(sign=0)； 01：pc<－pc+4+(sign-extend)immediate，相关指令：beq(zero=1)、bne(zero=0)、bltz(sign=1)； 10：pc<－{(pc+4)[31:28],addr[27:2],2'b00}，相关指令：j； 11：pc<- GPR[rs]，相关指令：jr；