



ASAP5: A predictive PDK for the 5 nm node

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ABSTRACT

We present a predictive process design kit (PDK) for the 5 nm technology node, the ASAP5 PDK. ASAP5 is not related to a particular foundry and the assumptions are derived from literature. It incorporates several innovations that the semiconductor industry has adopted to address scaling challenges, improve reliability and performance. These include contact over active gate (COG), fully self-aligned vias (FSAVs), single diffusion breaks (SDBs), and cobalt interconnects. We discuss implications of these changes in the context of standard cell and static random access (SRAM) bit cells. Interconnect modelling is improved and incorporates the effects of metal fill and barrier geometry on line resistivity. Different metal fill and barrier configurations are compared to determine the PDK interconnect stack. We discuss design rule assumptions for the key layers. The PDK uses horizontal nanowire field-effect transistors (NWFETs) for better ON and OFF-state performance. The transistor compact models are calibrated to the 3-D technology computer-aided design (TCAD) simulation results.

1. Introduction

Moore's law has continued past the 7-nm node by increasing deployment of multiple patterning (MP) and especially, extreme ultraviolet (EUV) photolithography. FinFET follow-on device architectures, e.g., gate all around (GAA) nanowire (NWFET) and nanosheet (NSHFET) transistors are emerging candidates [1–5]. As chips are increasingly power limited, process enhancement has focused on improving logic density via contact over active gate (COG) and single diffusion breaks (SDBs) [6–8]. The mass production success of EUV photolithography (EUVL) has allowed it to replace multiple MP steps.

The deployment of ASAP7 7-nm predictive PDK [9] for educational use [10–12], and its increasing research use [13–16], led us to develop a follow-on ASAP5 5-nm predictive PDK. This 5-nm PDK is described here. It is an update to enable continued educational use, more accurate circuit benchmarks, and allow foundry independent CAD tools and methodology development [17].

1.1. Objective, expected usage, and improvements over ASAP7

ASAP5 provides a foundry-independent, open platform for design exploration and comparison. It is intended primarily for logic design as it contains only thin-gate transistors, which are NWFETs. However, the design rules are compatible with finFETs. Like its predecessor, ASAP5 is based on realistic photolithography and technology assumptions, using

design-technology co-optimization (DTCO) requirements. Advanced EUVL is assumed for some layers, while some rely on the currently deployed EUVL capabilities. As in ASAP7, we assume MP mask decomposition is performed for the designers during mask generation. The design rules do not require designers to "color" the layouts. While many foundries require coloring, we believe this simplification is essential to educational (classroom) use.

The transistors are based on TCAD simulations and other process aspects, such as the choice of interconnect materials is based upon more detailed modeling and analysis. These assumptions, as well as the DTCO driven standard cell architecture and SRAM design are explained in detail.

1.1.1. High-NA EUVL assumption for 2D BEOL layers

The current generation of EUVL scanners with a numerical aperture (NA) of 0.33 are used by foundries for high volume manufacturing [18–20]. EUVL platforms with a high-NA of 0.55 are under development to enable further critical dimension (CD) reduction, since the latter is inversely proportional to NA [21]. Publications suggest high-NA EUVL is approaching readiness [22,23].

ASAP7 assumed the critical BEOL layers are bi-directional (2-D) patterned using 0.33 NA EUVL. This was optimistic since few initial N7 offerings from TSMC [24,25] and the Intel N10 (equivalent to foundry N7) [26] relied on 193i multiple patterning (MP). Subsequent updated N7 processes [20,27–30] employed EUVL for critical BEOL layers,

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Table 1

CDU and LER. Values for 193i and 0.33 NA are from published data, while those 0.55 NA EUVL are based on assumptions.

	193i Published	0.33 NA EUVL Published	0.55 NA EUVL Assumed
3σ CDU (nm)	0.58 ^a [92]	0.46 ^a [93]	0.46
3σ LER (nm)	1.5 [94]	2.5 [95]	1.9

^a Worst-case, isolated lines.

Table 2

Overlay values. XMMO value for 0.55 NA-to-193i is based on assumption.

	3σ Overlay (nm)
193i	2 [96], 2.5 [97]
EUVL (0.33 NA)	1.1 ^a [98]
EUVL (0.33 NA)-to-193i	2.3 ^b [93]
EUVL (0.55 NA)	1.1 ^a [22]
EUVL (0.55 NA)-to-193i	2.3 ^{b,c}

^a Matched machine overlay (MMO).

^b Cross MMO (XMMO).

^c Assumption.

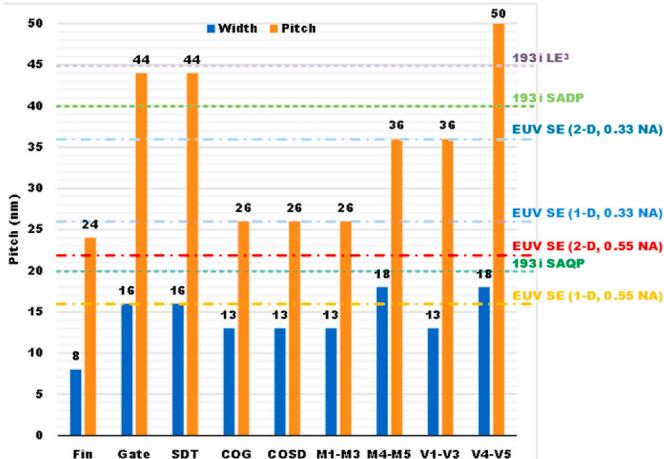


Fig. 1. Photolithography patterning cliffs by pitch and width for salient ASAP5 layers.

including 2-D EUVL patterned layers.

The approach to offer updated versions of a given process node with density, power, and other improvements, is standard practice that extends the longevity of a technology node. Bearing this in mind, we have made an optimistic assumption for ASAP5 as well, viz. the use of high-NA EUVL for 2-D patterning of critical BEOL layer patterning.

1.2. Paper organization

Section 1 presented a brief rationale for this work. Section 2 discusses the relevant photolithography related considerations and assumptions. Section 3 describes the NWFET transistor structure and parameters, as well as our choice of it over finFET and NSHFET. This is a summary of a more complete analysis and further details can be found in our previous work [31]. The front-end-of-line (FEOL) rules are also described. Section 4 describes the metal stack, including addition of COG features in the MOL layers. Design rule derivations are included. The resistivity modeling and choices of materials in the back-end-of-line (BEOL) comprises Section 5. DTCO aspects and the standard cell architecture, as well as the SRAM cells are discussed in Section 6. Section 7 describes the transistor electrical behavior and the process corners. Section 8

concludes the paper. When necessary, we explain our DTCO-based choice of the photolithographic assumptions for a layer in the context of either standard cells or SRAM cells rather than solely a scaling perspective.

2. Photolithography considerations and design rule calculation approach

This section describes some of the photolithography-related assumptions for determining the design rule checks (DRCs). We focus on EUVL, as it has become standard on many sub-10 nm processes and appears essential for sub-7 nm processes. We also discuss some of its advantages compared to 193i multiple patterning.

Critical dimension uniformity (CDU) is the dimensional consistency of a feature printed. CD variations arise due to a number of factors including wafer temperature, photoresist thickness, dose, focus, and mask variations [32]. The 3σ CDU values for 193i and 0.33 NA EUVL scanners are summarized in Table 1. We assume the same CDU value as the latter for 0.55 NA EUVL. Overlay is the positional inaccuracy resulting from misalignment between two mask steps [33]. The 3σ matched machine overlay (MMO) and cross matched machine overlay (XMMO) values for 193i, 0.33 NA EUVL, and 0.55 NA EUVL scanners comprise Table 2. We assume the XMMO value between 193i and 0.55 NA EUVL and 193i and 0.33 NA EUVL scanners is the same.

2.1. Stochastic effects in EUVL

Besides CDU and overlay variability, photolithography suffers from stochastic effects. These refer to random variability between features over small, “local” regions and arise due to photon shot noise, resist inhomogeneity, and local mask errors [34,35]. They differ from global CDU components that result from dose and focus variations [34] and manifest as local CD uniformity (LCDU). LCDU components include contributions from resist, dose, and contrast. LCDU is directly proportional to the square root of the light energy, inversely proportional to the square root of the dose, and inversely proportional to the normalized aerial image log slope (NILS) [36,37]. NILS refers to the steepness of the aerial image intensity and denotes the contrast of a printed feature [38].

Line edge roughness (LER) constitutes the majority of LCDU [39]. For EUVL, the local LER is large enough to dominate the total variability in a printed feature and even exceeds the printed feature global variability [40]. It is larger for EUVL due to fewer photons per unit dose compared to 193i, i.e., larger photon energy [41]. Other factors include limited EUV power transmission to the wafer, low EUV resist photon absorption, and smaller photon collection area [41]. Increased dose lowers LER but adversely affects throughput and thus cost. Increasing NILS reduces stochastics, lowering both LER and LCDU [42]. 0.55 NA EUVL scanners are expected to have a larger NILS than 0.33 NA EUVL [21]. This drives our lower LER assumption of 1.9 nm for high-NA EUVL (Table 1).

2.2. Design rule calculation approach

Design rules require determining patterning variation between different features, often typified as edge placement error (EPE). Gabor et al. argue against using the term EPE to represent space variations [43]. Mulkens et al. determine three different variation types: systematic, global, and local independently [44]. Gabor et al. suggest the variation be calculated accounting for CDU, overlay, and LER standard deviation as a root sum square (RSS) [43]. The latter represents the traditional approach for design rule calculations, and we use it for ASAP5. Stochastics can be accounted for by including the LER term in the RSS method. Strictly speaking, combining terms via RSS requires independent variability terms with ideal Normal distributions. In reality, this is not always the case—frequently the distributions exhibit kurtosis and skew. Moreover, by retargeting the photolithographic

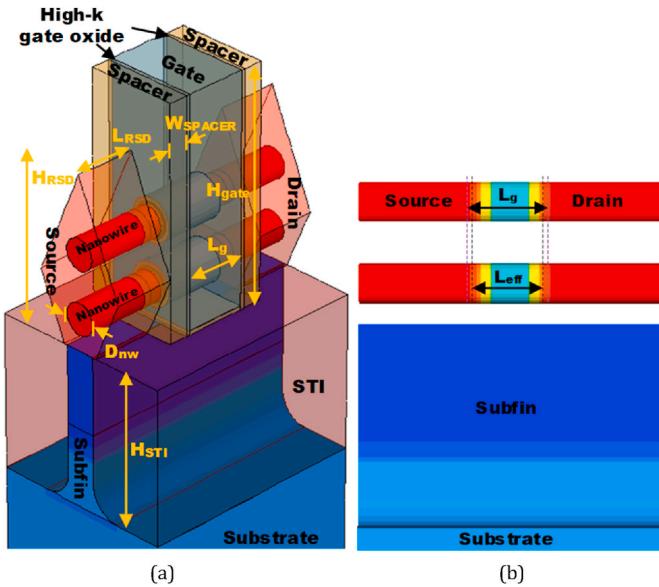


Fig. 2. Simulated n-NWFET (NW = 2) (a) 3-D view with 16 nm L_g and 16 nm L_{RD} (corresponding to 44 nm CGP) (b) cross section depicting doping concentration along the NW length. STI contacts to the raised source/drain are not shown in (a) for clarity.

Table 3
ASAP5 NWFET nominal design parameters.

Parameter	Value
L_g (nm)	16
L_{RD} (nm)	16
W_{SPACER} (nm)	5
CGP (nm)	44
W_{RSD} or P_{nw} (nm)	24
D_{nw} (nm)	8
W_{eff} (nm)	50.26
H_{RSD} (nm)	44
H_{STI}/H_{subfin} (nm)	40
H_{gate} (nm)	60
EOT (nm)	0.78
φ_{NMOS} (eV)	4.497
φ_{PMOS} (eV)	4.734
ρ_{c-NMOS} ($\Omega \cdot \text{cm}^2$)	2.2×10^{-9}
ρ_{c-PMOS} ($\Omega \cdot \text{cm}^2$)	2.0×10^{-9}
N_{sub} (cm^{-3})	1×10^{17}
N_{subfin} (cm^{-3})	5×10^{18}
N_{nw} (cm^{-3})	1×10^{15}
$N_{S/D}$ (cm^{-3})	2×10^{20}
S/D Doping Gradient (nm/dec)	1

targets and via rework, the distribution tails can be truncated. Gabor et al. suggest the use of 4σ values of the variability components for high volume manufacturing DRCs and even argued in the favor of using values as large as 7σ since failure opportunities increase with scaling [43]. We restrict ourselves to the use of 4σ values for calculating rules related to 0.55 NA EUVL. DRCs for layers patterned using 0.33 NA EUVL and 193i are unchanged from ASAP7.

Rules for enclosure and extension of one layer by another can be given by calculating the space variation alone. However, feature spacing may also require adding a reliability component to prevent time-dependent dielectric breakdown (TDDB). Which is used as elucidated for key layers below.

2.3. Single exposure (SE) EUVL necessity

193i MP use to pattern increasingly small pitches has resulted in both cost and throughput issues. Fig. 1 shows key ASAP5 layers and metal

patterning cliffs for various photolithography pitch values [45,46]. Often, factors other than the required minimum resolution and pitch must be considered. These include the required tip-to-tip same layer spacing and space variations between the same or different layers to enable dense standard cell pin placement and accessibility. In addition to cost, MP is challenging due to CDU variability and overlay considerations. A 2-D shape using multiple litho-etch steps, i.e., LELE (LE^2) or LE^x , may necessitate stitching, which complicates overlay requirements to ensure sufficient overlap. SADP is less amenable to 2-D shapes, and suggests a 1-D patterning approach [47]. This trades wire density against manufacturability [48]. Mallik et al. estimate a 16% and 5–15% lower area for 2-D vs. 1-D metal layers for SRAM cell and standard cells, respectively [49]. Our ASAP7 experiments have shown a pure 1-D approach makes simple logic gate layout difficult. 1-D on all but M1 has no discernible impact on area [50]. Consequently, in ASAP5 we opt for aggressive high-NA EUV that allows 2-D patterning for critical BEOL layers, particularly on M1.

2.4. EUVL advantages

EUV mask cost is approximately $1.5 \times$ that of 193i [49]. Other operational expenses bring up the EUVL cost to nearly $3 \times$ of 193i single exposure [51]. The mask count in each technology node has increased almost linearly up until N10. Liebmann et al. estimate the normalized LE^2 , LE^3 , SADP, and SAQP cost to be $2.5 \times$, $3.5 \times$, $3 \times$, and $4.5 \times$ that of 193i SE, respectively. Substitution of EUV over MP is a departure from this trend at N7 [52]. A 50% cost reduction for EUV over SAQP has been estimated [52]. Faster time to yield and time-to-market with EUVL as large as 30% contribute to EUVL cost-effectiveness. Yeap et al. reported EUVL replaced four 193i layers with a commensurate mask count reduction for a foundry N7 to N5 transition [53]. A recent foundry N5 publication even revised the traditional power, performance, and area (PPA) matrix terminology to power, performance, area, cost, time-to-market, and reliability-plus (PPACT™R+) [54].

Single exposure EUVL reduces overlay requirements. The small EUV wavelength allows a relatively large processing factor k_1 of 0.4–0.5. The resulting high contrast (NILS) allows printing higher fidelity features [18,28]. High feature fidelity, better corner rounding, and a single exposure reduce line and space CD variations, resulting in metals and vias with more uniform sheet resistance and lower capacitance [28]. Dummy fills and metals cuts are also obviated, improving scalability and performance [30].

Mallik et al. estimated the normalized wafer cost to increase by 32% at N10 and by a further 14% at N7 without EUV insertion [55]. They also estimated a 27% cost reduction with EUVL use at N7 for critical BEOL layer patterning with a 150 wafers per hour throughput. Ha et al. estimated 25% mask reduction at N7 with EUVL [28]. Dicker et al. estimate over 40% cost per function reduction in moving from N10 to N7, and further to N5 as a consequence of EUV insertion for critical BEOL layers [52].

3. ASAP5 NWFET design and FEOL layers

For the ASAP5 PDK, we conducted 3-D TCAD device simulations of NWFETs, finFETs, and NSHFETs [31] in contrast with the ASAP7 PDK, wherein the compact models were based on scaling trends. The analysis began with 3-D TCAD device simulations with finFET parameters, congruous with the ASAP7 compact models and geometries as the calibration reference. Synopsys Sentaurus Structure Editor was used to design the transistor structures and simulations used Sentaurus Device [56]. Fig. 2 (a) shows the 3-D view for the NWFET transistor structure—a similar finFET architecture is obvious. Essentially, the vertically stacked nanowires are etched from a fin comprised of a stack of silicon and silicon-germanium (SiGe), where NWs are formed by etching the SiGe [1]. Consequently, finFET layouts are identical.

The results indicated that finFETs are adequate at the 5 nm node,

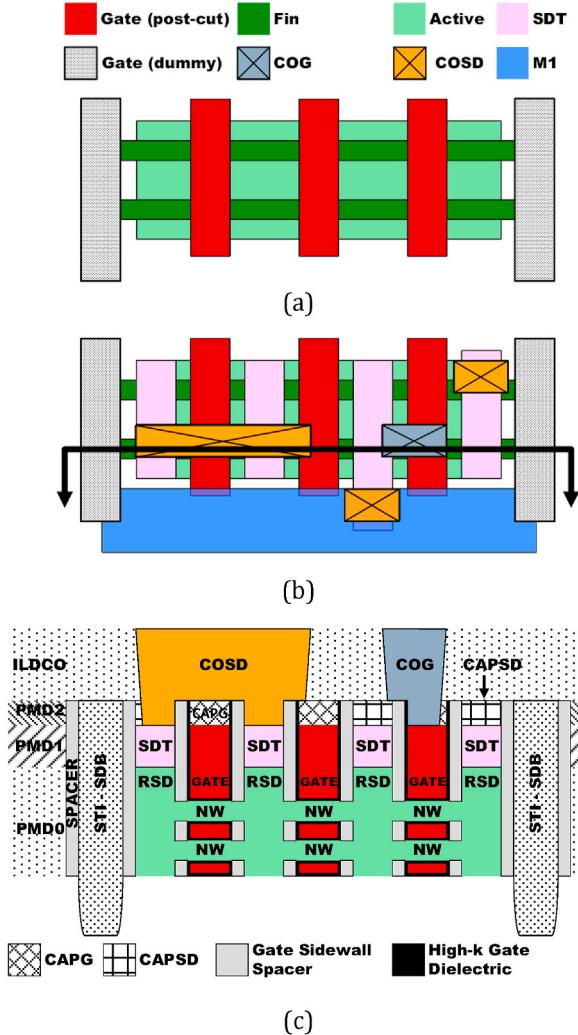


Fig. 3. Layout and cross section showing ASAP5 MOL and FEOL stack for a standard cell portion. (a) Gate, SDB, fin, and active constitute the FEOL. (b) FEOL shown together with SDT, COG, and COSD constituting the MOL. COG and COSD are drastically misaligned here to show shorting tolerance. (c) Cross section with both FEOL and MOL layers. COSD-to-SDT and COG-to-gate connections are evident. Both COSD and COG can cross-over the Gate and SDT, respectively. A single diffusion break is required at the cell boundaries.

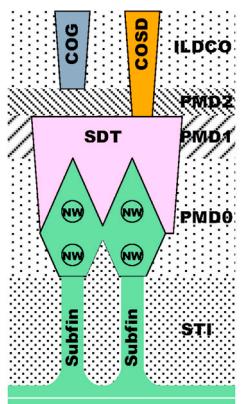


Fig. 4. NW and raised S/D cross section showing SDT and COSD connection. Ensuring a vertical spacing between SDT and COG eases the SDT-to-COG spacing.

Table 4

Technology node key layer dimensions and pitches by foundry.

Node	Foundry	Lg (nm)	CGP (nm)	Mx Pitch (nm)	Reference
N16	TSMC	30–34	90	64	[99]
N14	Intel	20	70	52	[63]
N10	Alliance	20	64	48	[100]
N10	Intel	–	54	36	[26]
N7	TSMC	15	–	40	[24]
N7	Alliance	15	48	36	[59]
N7	Samsung	–	–	–	[28]

should GAA devices, viz. NWFETs or NSHFETs, prove unmanufacturable. As expected, better GAA electrostatics provide I_{off} improvements and increased drive currents at the same I_{off} . The finFET sufficiency is consistent with foundry N5 finFET use [53,54]. The simulated NWFETs have better ON-state, but slightly worse OFF-state characteristics compared to NSHFETs for similar effective channel width. The latter afford greater latitude in circuit design due to non-discrete channel widths, but their drive strength and electrostatic characteristics degrade at larger widths. Although NSHFET fabrication has been demonstrated [57], we opted for the NWFETs since they are interchangeable with finFET layouts, enabling easier comparative studies and modeling. Moreover, variable width NSHFETs complicates the otherwise regular fin layout grid.

3.1. Gate length (L_g) and nanowire diameter (D_{nw})

Table 3 summarizes nominal parameters and doping concentrations used to design the NWFET. We assume a 16 nm metal gate length L_g , which is in line with another L_g estimate for N5 [1]. The NWFETs contain two vertically stacked horizontal nanowires (NWs), as shown in Fig. 2. The stack is analogous to a fin in a standard cell context, so units quantifying transistor characteristics for a single stack are “per fin”. The sub-fin, NW, and the raised source/drain (S/D) are all silicon (see the cross sections in Fig. 3 and Fig. 4).

A variety of gate lengths have been published for 16 nm, 10 nm and 7 nm foundry processes, although these values are frequently not disclosed or are treated as exemplary (see Table 4). Gate length in a certain node from one foundry does not match that from another foundry. It is reasonable to assume that foundries “put their best foot forward” by publishing aggressive data. Additionally multiple gate lengths are often offered. Moreover, the need to offer multiple V_t ’s, achieved via multiple work function layer combinations, requires sufficient gate length to include these layers, as well as a high conductivity shunt metal [58]. The gate layers are deposited over the fins or NWs within the spacers and thus consume volume in the gate length as well as the between fin directions. Yoshida shows that there is no room for conductive tungsten gate fill at 18 nm L_g for the lowest V_t option, and for any V_t option at 12 nm. The gate resistance increases for L_g under 20 nm without cobalt (Co) fill metal that may allow L_g scaling to 12 nm “WF chamfering” recesses the WF material, using the entire top of gate for barrier and conductive metal to ensure low resistance as demonstrated “for $L_g < 17$ nm” [59].

Some estimates show a 7 nm nanowire diameter (D_{nw}) at N5 [60,61]. We chose D_{nw} of 8 nm for the NWFET, since it provides a larger I_{dsat} than the former at a comparable target I_{off} for the nominal (16 nm L_g) device with only two NWs [31].

3.2. Contacted gate pitch (CGP) and NW pitch (P_{nw})

Foundry publications have demonstrated 48 nm contacted gate pitch (CGP) at N7 [59] and 54 nm CGP from Intel’s N7 equivalent [26]. The ASAP7 used 54 nm. CGP scaling is likely to slow down at N5, with some projecting a 42 nm value [1]. At early stages we assumed an aggressive 40 nm CGP, with a 12 nm raised source/drain (RSD) length (L_{RSD}). The RSD height is 44 nm and NWs are equidistant from RSD top and bottom. At this CGP and L_{RSD} , ring oscillator (RO) simulations showed significant

Table 5
Width, pitch, and photolithography assumptions for ASAP5 layers.

Layer	Width/drawn (nm)	Pitch (nm)	Lithography
Fin	8	24	193i SAQP
Active	24	40	–
Gate	16	44	193i SADP
SDT	16	44	EUV SE (1-D, 0.55 NA)
COG, COSD	13	26	EUV SE (1-D, 0.55 NA)
M1-M3	13	26	EUV SE (2-D, 0.55 NA)
V1-V3	21/13	18 ^a	EUV SE (0.55 NA)
M4-M5	18	36	EUV SE (2-D, 0.33 NA)
V4-V5	18	25 ^a	EUV SE (0.33 NA)
M6-M9	24	48	193i SADP
V6-V9	24	34 ^a	193i LELE
M10-M12	40	80	193i SE
V10-V12	40	57 ^a	193i SE

^a Corner-to-corner spacing as drawn.

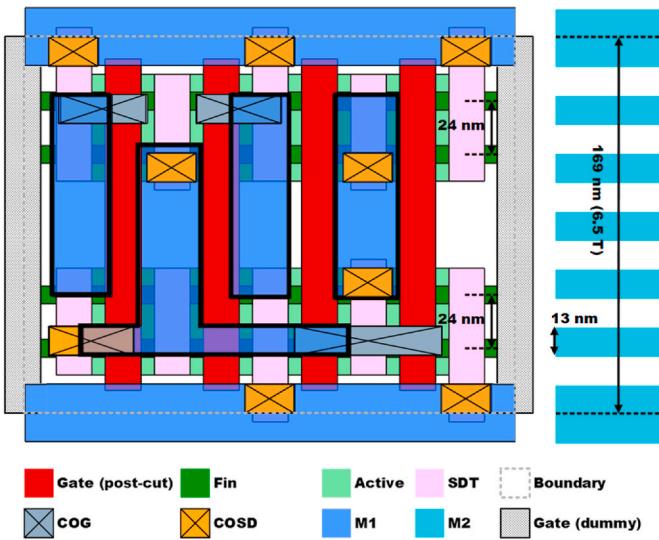


Fig. 5. A 6.5 M2 track ASAP5 standard cell, with two “fins” (NW stacks) per device type. The cell layout shows the FEOL, MOL, and M1 layers in an AND2 cell. The M1 power rails are connected to the source/drain by using the layer COSD.

speed-up when compared ASAP7. Unsurprisingly, relaxing the CGP and L_{RSD} to 44 nm and 16 nm, respectively, increased I_{dsat} . A larger CGP also improves pin access driving a final 44 nm CGP assumed to be patterned using SADP at a uniform 28 nm spacing.

Fin pitch scaled by $0.7 \times$ from N22 to N14 [62,63] and by $0.8 \times$ from N14 to N10 [26]. Assuming a $0.88 \times$ pitch scaling factor with respect to ASAP7 in order to conform with the slowing scaling trend, NWs are considered to be patterned at a 24 nm pitch and an 8 nm diameter using SAQP. In a finFET version of the process, fin width would scale, but the same pitch makes our design assumptions compatible. Table 5 summarizes the salient width/pitch and photolithography assumptions for ASAP5.

As in ASAP7, the drawn and actual active layers in ASAP5 differ from each other. The drawn active layer vertical edges (horizontal extent) denote the gate sidewall spacer edge and makes it visually apparent to the designer (see Fig. 3(a)). Unlike ASAP7, the actual active layer in ASAP5 does not extend half-way underneath the gate but is rather assumed to terminate at the gate edge. In standard cells, the single diffusion break (SDB) is created by a separate diffusion/fin cut layer which is self-aligned to the spacer [26]. The nanowires are cut at the gate edge inside the spacer by this shallow trench etch and deposition (Fig. 3 (c)). The ASAP5 PDK makes this cut mask implicit, with the intent of making the layout appear more conventional. SDBs result in a

horizontal spacing requirement of 26 nm between two active layer polygons. The implicit mask is 21 nm wide, assuming its edges are centered on the spacer.

3.3. Oxides, spacer width, and doping

Since we assume no V_{DD} scaling from N7, EOT is not scaled. The high- k gate oxide is a 1-nm thick HfO_2 layer. A 0.6 nm thick native SiO_2 layer separates it from the Si channel. This results in a 0.78 nm equivalent oxide thickness (EOT), which is approximately the EOT estimate for N7 at 0.8 nm [64]. The gate trench sides are coated with a 1 nm thick HfO_2 layer during its deposition at the trench bottom.

The sidewall high- k gate oxide layer abuts the 5 nm wide Si_3N_4 /low- k gate sidewall spacers that are used for raised S/D (RSD) self-alignment. While I_{dsat} improves due to lower S/D extension resistance with W_{SPACER} reduction, the rapid capacitance increase eventually dominates. The W_{SPACER} and high- k gate thickness combination of 6 nm was chosen to optimize the drive vs. capacitance by optimizing $\tau = CV/I$ and not just I_{dsat} [31].

Fig. 2 (b) shows the doping concentrations for various regions within the n-type NWFET. To avoid sub-surface punch-through in the finFET, the subfin close to the S/D is highly doped at $5 \times 10^{18} \text{ cm}^{-3}$. The NWs have a low, essentially intrinsic doping concentration of less than $1 \times 10^{15} \text{ cm}^{-3}$. We used a super steep sub-fin to fin retrograde doping profile for the finFETs [65]. The same sub-fin doping is used on the ASAP5 NWFETs for consistency, but it is unimportant since NWs are physically distinct from the sub-fin. The peak S/D region doping concentration is $2 \times 10^{20} \text{ cm}^{-3}$, which diminishes with a 1 nm/dec gradient from the extensions inside the spacers to the channel. The effective channel length (L_{eff}) is demarcated by a $2 \times 10^{19} \text{ cm}^{-3}$ peak doping concentration in the channel [65]. Thus, the L_{eff} is 14 nm for a 16 nm L_g and the 1 nm fin regions that underlay the metal gate edges on either side comprise the gate and S/D overlap dimension.

Uniaxial 1.6 GPa tensile and 2 GPa compressive stress are applied to the NMOS and PMOS, respectively, to increase drive currents. $2.2 \times 10^{-9} \Omega \text{ cm}^2$ and $2.0 \times 10^{-9} \Omega \text{ cm}^2$ contact resistivity (ρ_c), which have been proven in production, are used for the n-FETs and p-FETs, respectively [66]. Lower values have been reported [67].

4. ASAP5 MOL and BEOL layers

Fig. 3 comprises part of an ASAP5 standard cell layout and cross section. Fig. 4 shows the cross section in the perpendicular plane. In ASAP5 the source/drain trench (SDT) the RSD regions and does not cut through the gate sidewall spacers. It is self-aligned to the gate sidewall spacers. SDT is patterned at a wider width than the trench gap between the two gates/gate spacers then recessed below the spacers and capped (see Section 6.1). The vertical SDT edge is thus defined by the GATE whereas its horizontal edge is defined by 0.55 NA EUVL. This distinction results in different design rules depending on the edge in question.

RSD connects the nanowires upwards to the SDT. The local interconnect layers are contact over source/drain (COSD) and contact over active gate (COG), that connect M1 to the respective layers below. There is no V0 layer—M1 connects to the COG or COSD wherever they are coincident. The ability to contact gate over active device area is a key density improvement [26] greatly easing standard cell layout where gate contacts limit density [68]. The local interconnect COG and COSD are used as shown in Fig. 5.

The layer spacing, cap thickness, and spacer dimensions are driven by TDDB reliability. We assume a 5 nm minimum spacing requirement based on projection by Gao et al. for a process with 13 nm layer line and space CD, which is similar to ASAP5 assumptions [69]. This TDDB spacing is added to a design rule value where necessary. Despite an unscaled supply voltage from ASAP7, this more aggressive TDDB spacing is aided by the choice of interconnect material, as discussed in Section 5.1, and less conservatism.

4.1. COG and COSD process assumptions

The COG and COSD patterning and deposition is assumed to follow that demonstrated by Pethe et al. [6]. First, the COSD pattern is transferred atop the dielectric layer ILDCO (see Fig. 3 (c)), followed by ILDCO and trench cap (CAPSD) layer selective etching to create openings for contacts to SDT wherever COSD is coincident with SDT. The gate spacers, and more importantly, the gate cap (CAPG) are not affected since the CAPG material is different than the CAPSD material, which allows selective etching. This also enables COSD routing over gates (not shown) as well as COG routing over SDT. The 10 nm tall CAPG and a 5 nm wide gate sidewall spacer, which is assumed to be un-eroded due by the selective etch, despite potential COSD mask misalignment, alleviates TDDB removing a spacing requirement between COSD and GATE. At this point, the COSD metal is not yet deposited.

Subsequently, the process is repeated with COG patterns to etch CAPG to create openings for contacts to the gate, with the spacer and CAPSD (also 10 nm tall) remaining un-etched due to selective etching. In this manner, gates are contacted wherever COG in coincident with

$$4\sigma \text{SPACE}_{\text{COG-GATE-H}} = \left[\left(\frac{4\sigma \text{CDU}_{\text{GATE-MANDREL}}}{2} \right)^2 + (4\sigma \text{CDU}_{\text{SPACER}})^2 + (4\sigma \text{LER}_{\text{MANDREL}})^2 + (4\sigma \text{OVL}_{\text{EUVL-193i}})^2 + \left(\frac{4\sigma \text{CDU}_{\text{COG}}}{2} \right)^2 + (4\sigma \text{LER}_{\text{COG}})^2 \right]^{1/2}, \quad (1)$$

GATE. After this step the metal for COG and COSD is deposited. SDT-to-gate lateral distance meets the TDDB spacing specification as the SDT is self-aligned with respect to the 5 nm wide gate sidewall spacer and spacer is assumed to be un-eroded during SDT patterning.

Both COSD and COG layers are drawn to horizontally overlap and extend past the SDT and GATE layers. The extension amounts are given by the 4σ space variations between the respective layers and are computed in Section 4.1.1. The extension rule values ensure maximization of the COSD/COG fill contact area over SDT/GATE, even with misalignment. Fig. 3 (b) and (c) show an exaggerated misalignment case where the COSD left edge and COG right edge are not drawn with extension past SDT and GATE, respectively. The other COSD and COG edges overlap CAPG and CAPSD, respectively, but do not contact to the underlying layers due to selective etching assumption. This demonstrates that severe misalignment on the MOL does not result in shorting to the underlying GATE and SDT layers. A reduced overlap area between COSD-SDT and COG-GATE does however, increase resistance.

Because they comprise a single metal, COG and COSD short where touching. This is used to advantage in the SRAM cell and is common in many standard cells. In ASAP7, a V0 de-couples the LIG and LISD layers from M1 to permit LISD routing crossing M1 tracks and M1 routing crossing LIG that connect multiple gates in the middle of the cell. In ASAP5, minimizing the COSD use for routing and moving the COG over the active regions obviates a V0 layer, thereby simplifying both the

$$4\sigma \text{SPACE}_{\text{COSD-SDT-H}} = \left[\left(\frac{4\sigma \text{CDU}_{\text{GATE-MANDREL}}}{2} \right)^2 + (4\sigma \text{CDU}_{\text{SPACER}})^2 + (4\sigma \text{CDU}_{\text{GATE-low-k}})^2 + (4\sigma \text{LER}_{\text{MANDREL}})^2 + (4\sigma \text{OVL}_{\text{EUVL MMO}})^2 + \left(\frac{4\sigma \text{CDU}_{\text{COSD}}}{2} \right)^2 + (4\sigma \text{LER}_{\text{COSD}})^2 \right]^{1/2}, \quad (2)$$

assumed process and consequently, the design rules. Fig. 4 shows the CAPSD ensures a vertical separation, easing the SDT-to-COG spacing requirement. The 13 nm COG/COSD CD allows for connectivity to the M1 layer that is patterned at the same CD.

4.1.1. Salient COG and COSD design rule computation

In this section we compute the design rules for COG and COSD that affect standard cell density, reliability, and contact resistance. These rules are: horizontal COG extension past GATE, horizontal COSD extension past SDT, and COG/COSD spacing to M1.

Van Setten et al. demonstrated that NILS reaches the minimum useable value of two near a 18 nm half-pitch for contact hole arrays with 0.33 NA EUVL [21]. At the same resolution limit, the 0.55 NA EUVL system has a NILS of five. Furthermore, even though LE³ can reach the 11 nm half-pitches with a 0.33 NA source, the throughput, i.e. wafers per hour, is greatly reduced compared to a single EUVL exposure with a 0.55 NA source [70]. By comparison, 0.55 NA EUVL can print dense contact/via hole patterns at an 11 nm half pitch with a NILS value greater than two and with higher throughput [21,70]. Consequently, we assume the use of 0.55 NA EUVL to pattern the 13 nm wide COG and COSD layers for improved throughput, NILS, LER, and spacing variations.

We use the traditional RSS approach for design rule calculations. Thus, the horizontal COG extension past GATE is given by

where the $\text{CDU}_{\text{GATE-MANDREL}}$ term corresponds to the 193i CDU for the SADP GATE layer mandrel. $\text{CDU}_{\text{SPACER}}$ gives the variability in the spacer deposited around the mandrel and its 3σ value is assumed to be 1 nm. Spacers are formed using atomic layer deposition (ALD) and exhibit negligible LER [71]. The 193i patterned $\text{LER}_{\text{MANDREL}}$ is non-negligible. The COG layer patterning uses 0.55 NA EUVL. COG layer is aligned with respect to the GATE layer, which requires including the XMMO between the 193i and 0.55 NA EUVL toolsets, given by the term $\text{OVL}_{\text{EUVL-193i}}$. CDU_{COG} and LER_{COG} have the respective values assumed for the 0.55 NA EUVL.

Tables 1 and 2 enumerate the 3σ values for CDU, overlay, and LER. As discussed in Section 2.2, we considered 4σ values of all variability components for the 0.55 NA EUVL patterned layers. Thus, the values for the individual variability terms in the equations described within this section, and those used for computing other design rules for these layers, are scaled accordingly. The $4\sigma \text{SPACE}_{\text{COG-GATE-H}}$ value thus computed is found to be equal to 4.67 nm and is rounded to 5 nm.

As mentioned, the GATE layer defines the vertical SDT edges, so all GATE layer related terms from eq. (1) must be included when computing the spacing variation between COSD and SDT. The CDU for the gate sidewall spacers must also be considered. The COSD layer is aligned with respect to SDT, not GATE. Therefore, for the overlay requirement we use the 0.55 NA EUVL MMO. Consequently, the COSD extension past SDT in the horizontal direction is given by

which results in an aggressive $4\sigma \text{SPACE}_{\text{COSD-SDT-H}}$ value of 4.05 nm that we round to 4 nm. In addition to the M1-to-M1 spacing, the M1 routing in standard cells is also limited by its spacing requirement to

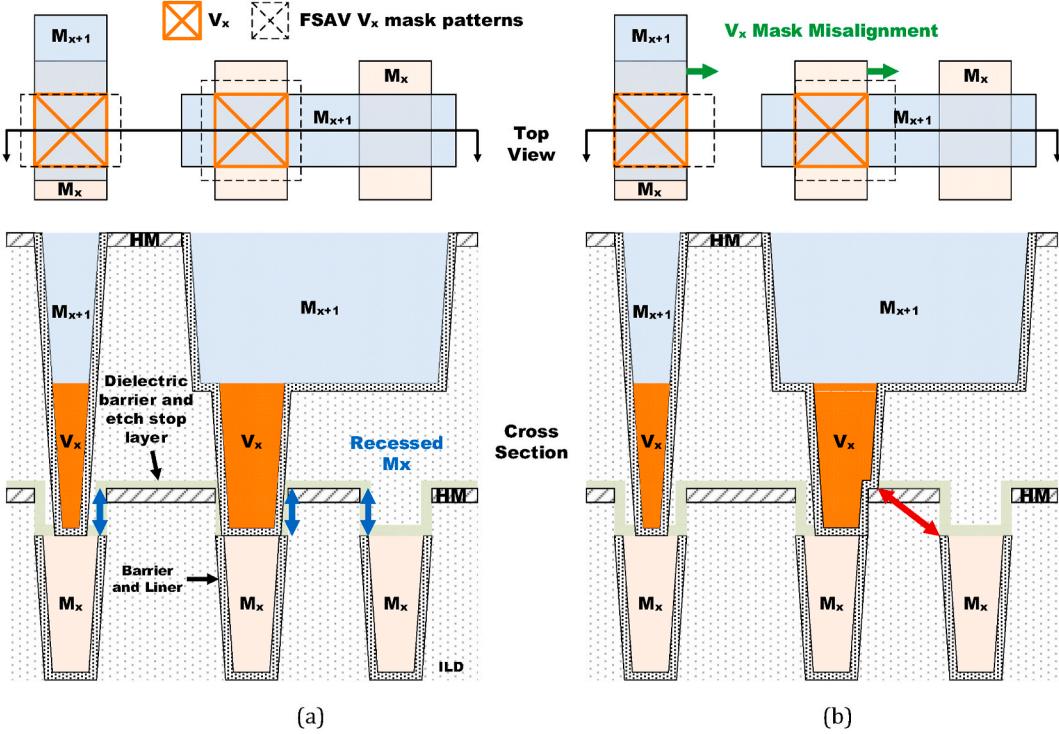


Fig. 6. (a) Fully self-aligned via (FSAV) scheme showing M_x , V_x , and M_{x+1} connectivity. (b) Worst-case M_x to V_x spacing scenario wherein V_x mask is misaligned to the greatest extent (green) in one direction. M_x recess below hard mask (HM) alleviates M_x to V_x shorting by ensuring sufficient spacing (red). M_{x+1} recess below the HM is not shown but is assumed.

COG and COSD layers that are not connected. The COSD/COG-to-M1 spacing includes the spacing required for allaying TDDB is

$$\text{Target_Space}_{\text{COSD-M1}} = \text{SPACE}_{\text{TDDB}} + 4\sigma \text{SPACE}_{\text{COSD-M1}}, \quad (3)$$

Where the COSD to M1 space variation is calculated as

D) patterned using 0.33 NA EUVL.

The M6-M9 target CD and pitch are 24 nm and 48 nm, respectively. This pitch target can be attained using either SADP or LE³. We assume SADP for cost and its lower LER that limits RC variability [51,71,74]. Spacer-is-dielectric (SID) is selected over spacer-is-metal as it permits

$$4\sigma \text{SPACE}_{\text{COSD-M1}} = \left[\left(\frac{4\sigma \text{CDU}_{\text{COSD}}}{2} \right)^2 + (4\sigma \text{LER}_{\text{COSD}})^2 + (4\sigma \text{OVL}_{\text{EUVL MMO}})^2 + \left(\frac{4\sigma \text{CDU}_{\text{M1}}}{2} \right)^2 + (4\sigma \text{LER}_{\text{M1}})^2 \right]^{1/2}, \quad (4)$$

The $4\sigma \text{SPACE}_{\text{COSD-M1}}$ value, as computed above, is 3.9 nm, rounded to 4 nm. This results in a 9 nm COSD/COG-to-M1 spacing requirement (Target_Space_{COSD-M1}) including the 5 nm TDDB spacing specification.

4.2. BEOL layers

The ASAP5 PDK provides 12 interconnect metal layers (M1-M12) and corresponding vias (V1-V12) for routing. ASAP7 supported M1-M3 layers were assumed to be patterned EUVL with a 0.33 NA source, which enabled 2-D shapes on these layers to simplify educational use. We follow the same approach for ASAP5 and to enable lower metal pitch scaling as well as 2-D shapes, we assume the M1-M3 layers to be patterned using EUVL with a 0.55 high-NA source [21,36,72] at a 13 nm half-pitch [45,46]. Tip-to-tip values as small as 20 nm has been shown for 0.33 NA EUVL [73] and as we assume the same for 0.55 NA EUVL. V1-V3 are assumed to be patterned at a 13 nm width using 0.55 NA EUVL following the same reasoning as that for COG and COSD.

For the layers above M1-M3 and V1-V3, we use some of the same width/pitch values and consequently, the same assumptions, as in ASAP7. M4-M5, as well as V4-V5 have an 18 nm CD and 36 nm pitch (2-

multiple metal widths and spaces, which is beneficial for clock and power routing. Patterning 2-D shapes is possible in SADP but presents challenges [74]. Consequently, we restrict these layers to 1-D routing. For SADP, design rules must ensure that shapes patterned using the block mask and the mandrels can be resolved. Fixing DRCs by looking at these masks, and the spacer, is non-intuitive. The ASAP5 SADP design rules are based on ASAP7 equivalent metals [75]. We formulated restrictive design rules (RDRs) that ensure correct-by-construction metal topologies and guarantee resolvable shapes referring only to the metals as drawn. The rules are color agnostic. Nonetheless, to validate the DRCs, the mandrel, block mask, and spacer shapes are completely derived in our separate validation rule decks (not released) which used coloring decks [75].

The primary SADP decomposition criterion uses a single CD routing grid based color assignment. This is supplemented with decomposition criteria and design rules to account for wide metals of specific legal widths for preventing odd-cycle conflicts. A fixed metal side-to-side spacing RDR reduces the occurrences of block mask defined line edges that suffer from worse CDU compared to spacer-defined edges. Other RDRs include adjacent metal tip-to-tip and parallel run length for block mask correctness.

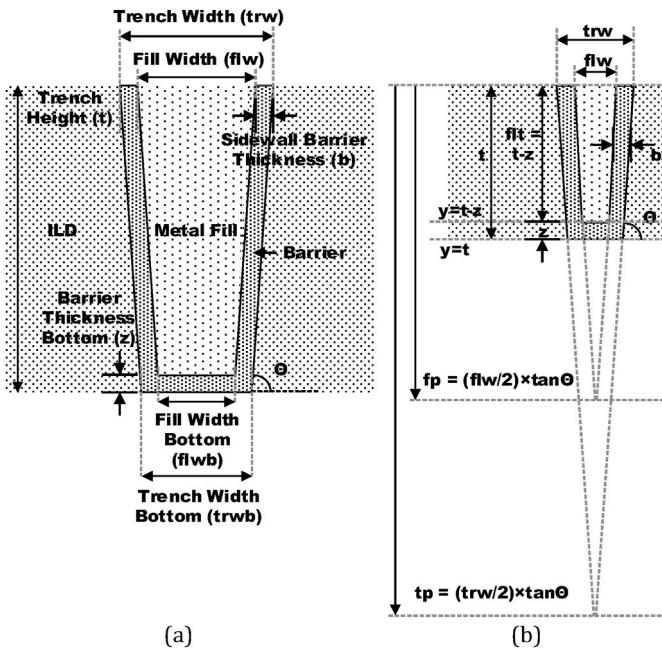


Fig. 7. (a) Metal and barrier geometric parameters. (b) Fill (f_p) and trench peak (t_p) locations determine various line configurations, including pinch-off scenarios.

Table 6

Parameters for eq. (5) [84].

Parameter	Definition	Value		Units
		Cu	Co	
ρ_0	Sum of resistivity from bulk, impurity, and defect	1.8	6.1 ^a	$\mu\Omega\text{-cm}$
A	Fill cross sectional area	—	—	nm^2
B	Parameter for resistivity increased by size effect	92	152	$10\Omega\text{-nm}^2$

^a For Ti/TiN barrier.

Table 7

Parameters for W used eq. (6) [85].

Parameter	Definition	Equation	Value	Units
ρ_0	Bulk resistivity	—	8.7	$\mu\Omega\text{-cm}$
C	Geometry based constant	—	1.2	—
P	Electron specular reflection parameter at interface	—	0.3	—
h	Trench height	—		nm
A	Fill cross sectional area	—		nm^2
λ	Electron mean free path	—	33	nm
α	—	$\frac{\lambda}{G} \frac{R}{(1-R)}$	—	—
R	Electron reflection coefficient at grain boundaries	—	0.25	—
G	Grain size diameter	$g\sqrt{A}$	—	nm
g	Grain size relative to wire size	—	1.32 ^a	—

^a Value computed assuming a grain size of 26 nm and a wire size of 18 nm.

V6–V9 are patterned using 193i LELE at a 24 nm CD. Lastly, M10–M12 and V10–V12 are assumed to be patterned using 193i SE at a 40 nm CD for the metals.

4.2.1. Fully self-aligned vias (FSAV)

ASAP5 layers assume fully self-aligned via (FSAV). The layout and cross sections are shown in Fig. 6. A fully self-aligned V_x is not merely aligned with respect to M_{x+1} , which was the case in SAV, but also to M_x .

The FSAV process follows the steps described in Refs. [76–78]. A SAV process suffers from via spreading along the M_{x+1} length [9]. Depending upon the extent of misalignment, this can either lead to via-metal encroachment that exacerbates the TDDB or create shorts between a V_x and neighboring M_x , which is adjacent to the M_x to which V_x must connect. Furthermore, when the V_x connects perpendicular M_x and M_{x+1} , the SAV V_x (non-FSAV) mask, which has a larger CD perpendicular to M_{x+1} , can only tolerate the misalignment in the same direction and not perpendicular to the M_x . This results in V_x not landing completely on M_x when misalignment occurs, thereby increasing the via resistance due to a smaller contact area.

A FSAV alleviates the TDDB and shorting to neighboring M_x by ensuring sufficient spacing [78] and also maximizes the contact area by ensuring full V_x landing on M_x , as shown in Fig. 6. Alignment of FSAV V_x to M_x is enabled by recessing M_x with respect to the dielectric layer surrounding M_x . This recess below the inter-layer dielectric (ILD) works similarly to the previously described gate/SDT. In the case of a V_x misalignment perpendicular to the M_x length, the height difference between the raised ILD and M_x ensures sufficient TDDB V_x to neighboring M_x separation. A FSAV scheme also allows for a wider V_x mask CD perpendicular to the M_x length. This ensures full V_x landing on M_x in case of a misalignment perpendicular to M_x length, thereby maximizing V_x -to- M_x connection landing area. As the V_x CD being printed is larger, it also mitigates photolithographic variability (Fig. 6(b)). In our assumed FSAV process, the V_x mask shape is derived by extending the V_x visible layer edges corresponding to the M_x and M_{x+1} layers. Moreover, when the V_x connects perpendicular M_x and M_{x+1} , the V_x mask shape can be a square, with the extension amount equal. This is evident in the rightmost via in Fig. 6(a).

5. Interconnect parasitic resistance considerations and material

The exponential increase in resistivity due to surface and grain boundary electron scattering with metal CD reduction, i.e., the resistivity size effect, has become a particular concern for copper (Cu) interconnects [79]. A highly resistive barrier layer, typically tantalum nitride (Ta_N) is required at the Cu inter-layer dielectric (ILD) interface to out-diffusion. The barrier layer thickness does not reduce commensurately with interconnect scaling, as a minimum width of this layer is required to prevent fill metal diffusion. Thus, compared to the amount of the less resistive metal fill, the fraction of the barrier material increases in the interconnect cross section with scaling that exacerbates the resistivity increase. Thus, the combined choice of barrier layer and fill metal are crucial. Consequently, alternatives to Cu and Ta_N, both of which have been used in the CMOS metallization flow for nearly two decades, have been sought [80].

We analyzed different metal fill and barrier configurations to determine the ASAP5 interconnect stack assumptions. Herein, the term “fill” denotes the conducting metal deposited in an interconnect trench, sans the barrier layer, whereas the term “line” denotes both the fill and barrier layers (see Fig. 7 (a)). In early versions of ASAP7, we included the barrier resistivity contribution, but not its effects on line resistivity due to changes in the fill and barrier area as functions of barrier sidewall (b) and bottom (z) thicknesses, trench slope angle (θ), trench aspect ratio (AR), and trench CD. Moreover, while we computed the resistivity change with CD for Cu, we did not do so for the tungsten (W) MOL layers. For the most recent ASAP7 release and ASAP5, we used a more detailed interconnect parasitic resistance analysis that incorporates the effects of fill and barrier on the line resistivity due to changes in the aforementioned parameters. The fill and trench pinch-off scenarios when critical CDs are reached are also comprehended.

Cu was replaced with Co in a foundry N10 (really N7) interconnect stack to achieve a 2 × reduction in via resistance and a concomitant 5–10 × electromigration improvement [26]. W has been used for MOL layers in recent technology nodes despite its higher resistance than Cu due to the former causing less device contamination and its resilience to

electromigration, high temperature, and other processing steps [81]. Additionally, W allows for good step coverage and gap-fill even with large aspect ratios [82]. Titanium nitride (TiN) can be used as a barrier for both Co and W. Although Co can be deposited directly on a dielectric without a barrier, its adhesion is weak, risking delamination [83]. A 1 nm thin layer of TiN has been found to prevent delamination and decreases diffusion into the dielectric [83]. Thus, we included Cu, W, and Co, as fill metal candidates, and TiN and TaN as barrier layer candidates in our analysis. We compute the Cu and Co resistivity by using an extension of the Fuchs-Sondheimer, Mayadas-Shatzkes (FS-MS) model after Hu et al. by using eq. (5) [84]. Parameter definitions and values for eq. (5) are given in Table 6.

$$\rho = \rho_0 + \frac{B}{\sqrt{A}} \quad (5)$$

We determine the W resistivity after Steinhögl et al. who used the classic FS-MS, given by eq. (6) [85]. Parameter definitions and values for eq. (6) are given in Table 7.

$$\rho = \rho_0 \frac{3}{8} C(1-P) \left(\frac{1}{h} + \frac{h}{A} \right) \lambda + \rho_0 \left[1 - \frac{3}{2} \alpha + 3\alpha^2 - 3\alpha^3 \ln \left(1 + \frac{1}{\alpha} \right) \right]^{-1} \quad (6)$$

The line resistivity includes contributions from both the metal fill and barrier layers. The areal term A in eq. (5) and eq. (6) corresponds to the fill metal and varies as the function of b , z , θ , and trench height (t), as evident in Fig. 7 (a). All possible trench and fill shape combinations can be derived by changing the locations of the apexes of the equilateral triangles formed by extending the lines corresponding to the trench and fill sidewalls, as shown in Fig. 7 (b). These apexes are termed as trench peak (t_p) and fill peak (f_p). As they are functions of b , z , θ , and t , they can be used to analytically estimate the area A and ascertain when fill and trench pinch-off occur. Relating the barrier and trench geometric parameters to the fill area in this manner allows us to determine the effects of changes in the former parameters on fill resistivity and subsequently, line resistivity. We assume θ to be 86°. For a given combination of fill and barrier, we consider b to be equal to z .

For ASAP7, we had assumed Cu fill with a ruthenium (Ru) barrier by comparing it to Cu fill with TaN barrier after Pyzyna et al. [86]. For the most recent ASAP7 version we re-computed line resistivity and via resistivity for the same material choices after the same author and while employing our revised approach. Since we chose Co as a potential fill candidate for ASAP5, we refer to the work by Hu et al. that considers both Cu and Co fill. However, the resistivity values that we computed for Cu fill with a TaN barrier after Pyzyna et al. do not correspond well with those computed for the same fill and barrier materials by Hu et al. Thus, only the latter work was used when comparing Cu and Co for ASAP5 as it provides a common frame of reference.

5.1. Comparison of metal resistivity change with CD and interconnect material choices

The BEOL metals and vias have a 2:1 AR in ASAP5 and the MOL layers have a 3:1 AR, which corresponds to 26 nm and 39 nm trench heights relative to the 13 nm CD BEOL and MOL layers, respectively. A taller MOL trench is useful as it allows for 9 nm (including an additional 5 nm guard-banding) gate/SDT cap for TDDB prevention.

Fig. 8 shows the line resistivity as a function of the line/trench CD at 26 nm trench height corresponding to the critical BEOL layers, comparing the traditionally used Cu and a viable alternative, viz. Co. We computed line resistivity for Cu fill with 2 and 3 nm TaN barrier, and Co fill with 1 and 2 nm TiN barrier. For Co, the 1 nm barrier thickness represents a realistic option as discussed earlier and given that it suffices

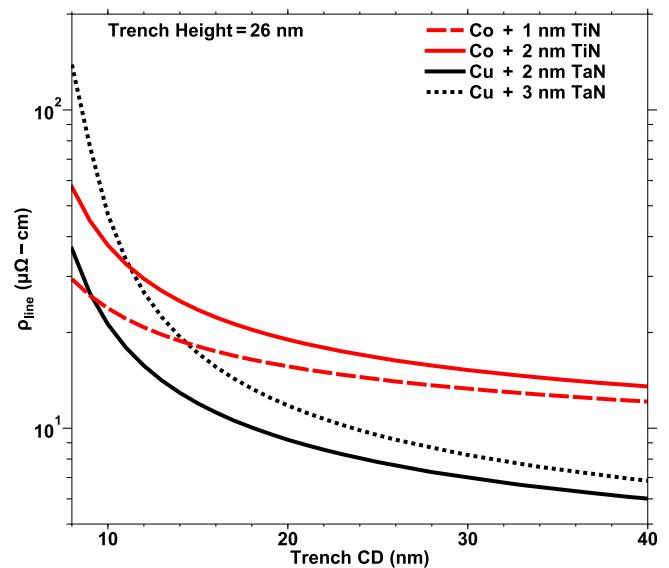


Fig. 8. Co and Cu line resistivity vs. interconnect trench CD for 26 nm trench height and 86° trench slope. The trench height corresponds to a 2:1 AR with respect to 13 nm trench CD and is used for M1–M3 and V1–V3 layers.

in a real CMOS process flow [83], we consider 2 nm thick barrier as the only other alternative and exclude a 3 nm thick barrier from the analysis. These line resistivities correlate well with those given by Edelstein [80].

While Cu has a smaller bulk resistivity than Co [84], its line resistivity increases faster with trench CD reduction than Co, as apparent from Fig. 8 due to the need for a thicker and highly resistive TaN barrier. At small trench CDs, the Cu line resistivity crosses over and is larger than the Co alternatives. Although Ru is a good candidate for TaN replacement as a Cu barrier layer, its adaption for this purpose in foundry processes is as yet unclear.

The Cu vs. Co cross-over points favor Co fill with a 1 nm TiN barrier below a 15 nm trench CD when comparing it to Cu fill with a 3 nm TaN barrier (see Fig. 8). Thus, we chose Co fill with a 1 nm TiN barrier for the M1–M3 and V1–V3 layers since the routing on these layers will frequently be at the minimum metal/via width of 13 nm. Cu remains competitive against Co with a 1 nm TiN barrier until an approximately 9 nm trench CD for a more optimistic process where a 2 nm thick TaN barrier is considered for Cu. Nonetheless, we decided on Co fill for its 5–10 × lower electromigration [26]. Co interconnects have also been shown to have better TDDB reliability than Cu [83].

As mentioned, For M4–M12 and corresponding V4–V12 in ASAP5, Cu fill with a 1 nm Ru barrier is used for line resistivity calculations, i.e., ASAP7 assumptions, as those layers are copied, despite the lack of foundry adoption.

As mentioned, W MOL layers have advantages despite higher W resistivity. However, Auth et al. demonstrated W replacement with Co in a foundry N7 equivalent contact metal layer [26]. This makes it relevant to compare the two metals for MOL usage. To this end, we also compute line resistivities for W (with 2 and 3 nm TiN barrier) and Co (with 1 and 2 nm TiN barrier) as function of the line/trench CD at a 39 nm trench height corresponding to the MOL layers, as shown in Fig. 9. W resistivity is exceedingly high and is greater than that of Co for all trench CD and barrier combinations. This drives our assumption of Co fill and 1 nm TiN barrier for the ASAP5 SDT, COSD, and COG layers.

The fill pinch-off for 26 nm and 39 nm tall trenches with an 86° slope

and 3 nm thick barrier occurs at 9 nm and 11 nm trench CD, respectively. When the barrier thickness is changed to 1 nm, the fill pinch-off occurs at 5 and 7 nm, respectively. With a 4 nm thick barrier, the 39 nm tall wire pinches-off at a 12 nm trench CD. For a trench slope of 83°, fill pinch-off in a 39 nm tall trench occurs at 13 nm (target MOL CD) given a 2 nm thick barrier. Thus, an N5 metallization scheme requires barriers thinner than or equal to 3 nm and preferably a steeper trench angle ($\geq 86^\circ$) at a 13 nm CD to prevent fill-pinch off for 3:1 AR MOL layers. Beyond N5, where CD may be ~ 8 nm, still thinner barrier layers will be required for low AR BEOL layers.

6. Standard cell and SRAM bitcell architectures

6.1. Standard cell

For the ASAP5 cell library, we assumed a 6.5-track cell (see Fig. 5) library that allows for double CD, i.e. twice the minimum metal width, M2 power rails that ensure robust power delivery. This follows the foundry trend of fin depopulation for greater density. A 5.5 or 5 track architecture reduces the number of cell internal routing tracks, potentially affecting the library richness [68]. The 6.5-track architecture allows for two fin wide transistors for both device types and has five M2 routing tracks. The COG and COSD contact layers fall on the same M2 routing track grid, which simplifies design by permitting a template approach. The cells end on a SDB to further maximize density.

The connectivity between the M1 power rail and RSD in the ASAP5 standard cells uses the SDT-COSD stack (Fig. 5). This (we believe common) scheme avoids the spacing requirements between gate and power rail LIG in ASAP7. The gate cap ensures sufficient gate-to-COSD vertical separation for TDDB. Because the COSD connecting to the M1 power rail is drawn at half the M1 power rail width, it is always separated from the non-equipotential SDT in the vertically adjoined cell by 13 nm.

Selecting adequate thickness for the CAPSD/CAPG/gate spacer layers and metal recess depth in the FSAV scheme preclude the TDDB spacing requirements for MOL-to-FEOL and M_x -to- V_x inter-layer design rules, respectively. Consequently, the only inter-layer design rules incorporating TDDB spacing are those for COG/COSD-to-M1 and COG-to-COSD (9 nm).

The SDT rules used DTCO, e.g., in the vertical spacing requirement between the power and non-power SDT at the standard cell power rails. SDT must extend past the COSD for misalignment tolerance. The space variation for SDT extension past COSD in the vertical direction (i.e., horizontal edges) must be given by an equation like eq. (4) but for single exposure. The rounded SDT 4σ space extensions needed are 5 nm and 4 nm, for 0.33 NA and 0.55 NA EUVL, respectively. This implies a vertical SDT-to-SDT spacing of 12 nm or 13 nm, respectively, at the power rails.

The 12 nm spacing forces 0.55 NA EUVL, but even then, it cannot be reached as a tip-to-tip dimension. Thus, the SDT printing must be wide enough to invoke the side-to-side rule (W_{SDT_WIDE}) at 26 nm w. Drawn and actual post-recess SDT has a width of 16 nm between the gate sidewall spacers and W_{SDT_WIDE} (see the cross-section in Fig. 3 (c)).

Fig. 10 (a) shows a 6.5-track ASAP5 cell with an ASAP7-like (V0 equipped) MOL stack lacking contact over active gate. Fig. 10 (b) shows the same cell with the ASAP5 MOL stack, i.e., no V0 and with COG/COSD. COG considerably simplifies routing on the (bold outlined) internal node. Not apparent here, its greatest benefit is on high fan-in gates and latch layouts, including pass-gate cross-overs. The route is shorter with COG (Fig. 10 (b)), thus lowering RC. However, the removal of V0 can reduce pin access (height). The SAQP fin patterning scheme for the 6.5-track cells is shown in Fig. 10 (c) and is also driven by fin patterning requirements in the SRAM cells. As we will discuss in Section 6.2, an 8

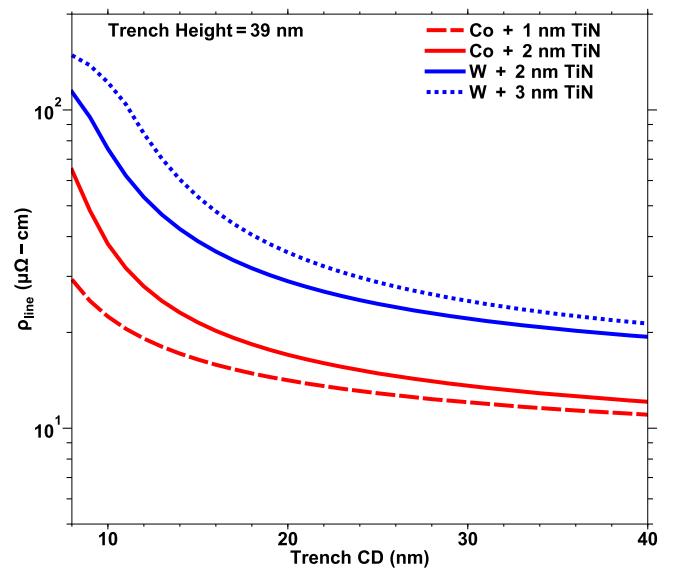


Fig. 9. Co and W line resistivity vs. interconnect trench CD for 39 nm trench height and 86° trench slope. The trench height corresponds to a 3:1 AR with respect to 13 nm trench CD and is used for COG and COSD.

nm resist trim (4 nm on each edge) is required for the fin mandrels in SRAMs. The same amount of resist trim must be used on the standard cell mandrels too since it must be uniform across the wafer. This is not an issue for ASAP5 6.5-T standard cells, due to the large values of mandrel pitch (169 nm) and target mandrel width (71 nm). This provides latitude for the application of 8 nm etch bias and still maintain the 98 nm mandrel-to-mandrel target spacing.

Fig. 11 demonstrates the interplay between some of the density limiting rules and pin access in a standard cell. Reiterating, these rules are: horizontal COG extension past GATE, horizontal COSD extension past SDT and COG/COSD-to-M1 spacing. These values are given by those for the terms $4\sigma_{SPACE_{COG-GATE-H}}$, $4\sigma_{SPACE_{COSD-SDT-H}}$, and Target_Space_{COSD-M1}, respectively, as calculated in Section 4.1.1. The 13 nm M1 side-to-side spacing is another limiting rule. These rules are annotated atop the cell layout portion in Fig. 11. The internal M1 routes (R1 through R3; R1 and R2 are connected) and M2 tracks (T1 through T5) denoting pin access are also labeled. Both the power rails and the internal M1 routes invoke a tip-to-side spacing requirement on the M1 pins. This large spacing can limit the available tracks for pins. A wide M1 pin requires the smaller side-to-side value, often improving pin access.

The B1 pin (horizontal) width is limited by the COSD.M1.S.8 and M1 S2S rules depicted (Fig. 11). The COSD vertical edge that interacts with B1 pin's right edge cannot be pulled-back to the right due to the COSD. SDT.EX.3 required overlap. By jogging the B1 pin M1 and placing the COG connecting to pin A1 over the active region, B1 can be sufficiently widened so as to only require M1 S2S rules between itself and R3. This enables B1 access via track T4.

6.2. SRAM

Fig. 12 shows the 122 (1 pull-up, 2 pull-down, and 2-access NW stacks) SRAM cell designed for ASAP5 with a 208 nm height. The same 44 nm gate pitch as the standard cells is for simplicity. SRAM nearly always uses a longer gate—SRAM L_g could be increased by up to 4 nm at the expense of S/D resistance, using the SRAM ID layer. The non-uniform pitch fins are patterned using SAQP (Fig. 12 (a)). The 80 nm

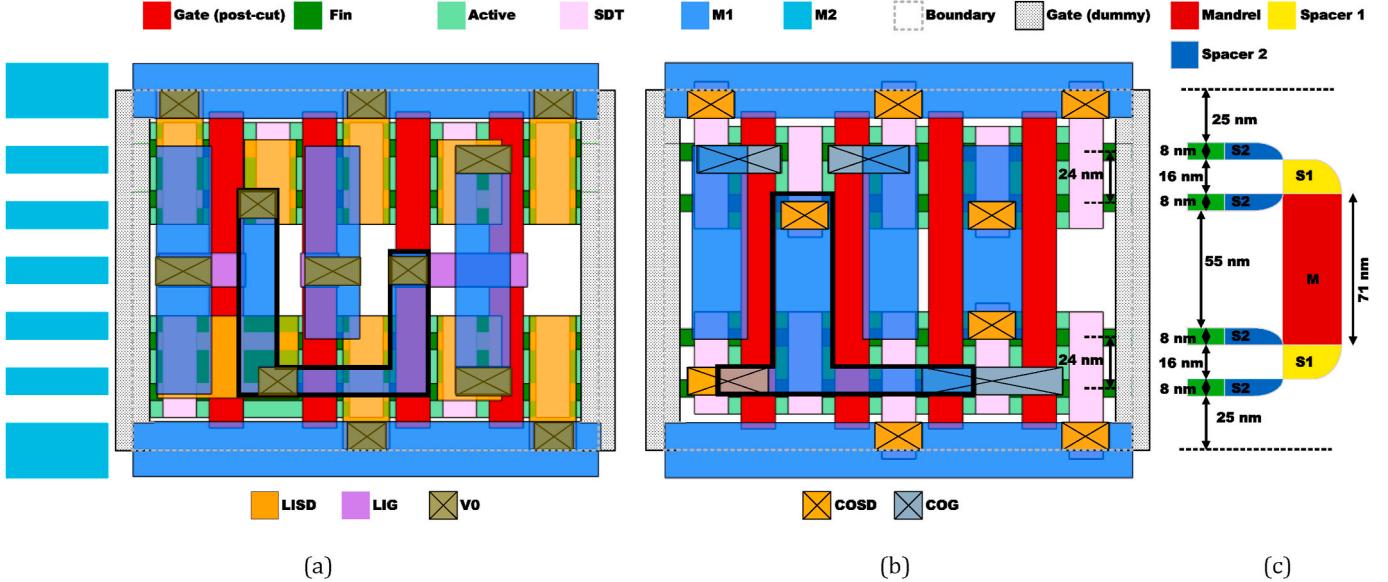


Fig. 10. (a) A 6.5-track AND2 cell, designed with an older ASAP5 version with an MOL stack with LIG, LISD, and V0 similar to ASAP7. (b) AND2 cell with the ASAP5 COG and COSD stack. Emboldened M1 routes in both cells illustrate the routing simplification in the latter cell when contact over active gate layer (COG) is used. Top legend shows common layers and bottom legend shows layers unique to each layout. (c) Nanowire (NW) patterning scheme for ASAP5 standard cells.

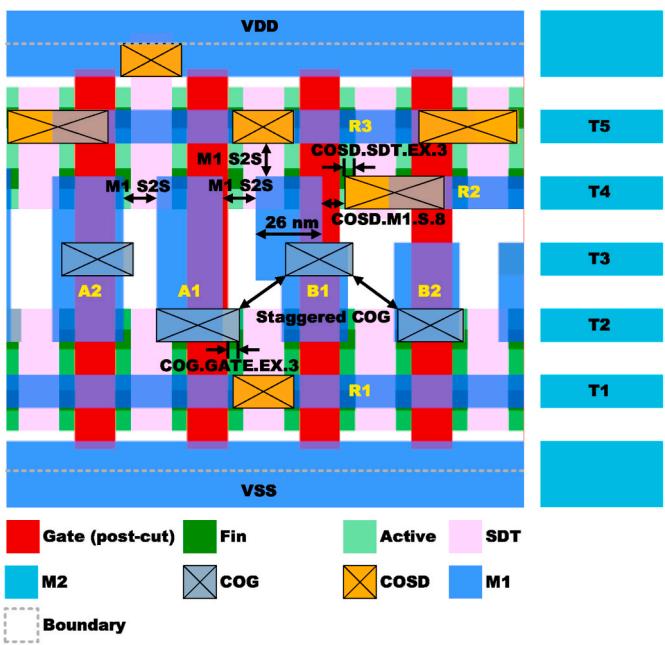


Fig. 11. Standard cell layout portion showing rules that limit density, viz. the COSD-SDT, COG-Gate extension rules, COSD/COG-to-M1 spacing (includes TDDB requirement). Wide M1 pins lower the resistivity and allows minimum M1-to-M1 spacing to the vertical M1 internal routes for improved pin access. Ability to place COG over the active enables staggering it, easing COG-to-COG and COG-to-M1 spacing requirements.

mandrel-to-mandrel pitch allows a 193i single exposure. The 32 nm mandrel spacing is obtained by a post-exposure resist trim (4 nm on each edge). The NMOS transistors are on a 24 nm pitch and the PMOS transistors are separated by 40 nm, which is also their pitch to the NMOS transistors. Fin patterning at the center of the SRAM is suppressed by abutting the two first-level spacers labeled S1 in Fig. 12 (a). Abutting spacer merging has been demonstrated [87,88].

The M1 bit lines (M2 word lines) may not be desirable as these metal directions do not match the standard cells. An M2 bit line cell can be

trivially obtained by promoting the metals up one layer. The FEOL and MOL layers for the cell comprise Fig. 12 (b). The inverter PMOS and NMOS RSD and the other inverter gate are connected using SDT as is typical. Fig. 12 (c) and (d) show BEOL layers. The 122 SRAM cell is eight tracks tall and aggressively scaled at $0.57 \times$ the area of a 122 SRAM cell in ASAP7, which was pessimistic compared to N7 foundry data. The LIG to SDT spacing, critical in ASAP7 SRAM cells, is alleviated by the SDT cap. V_{ss} is gridded on M2 to ensure a good reference level. However, the V_{dd} is not gridded, allowing the use of a separate V_{dd} by column for write assist [50,89].

The SDB scheme outlined above in Section 3.2 and Fig. 3 (c) creates a complication for the SRAM cells. Since the diffusion/fin cut mask terminates a fin at the gate and fills the region between the spacers with oxide, contacting the gates at the ends of the PMOS transistors would not be possible. Moving the fin cut and STI fill past the gate, to the location between the cells, as shown in Fig. 12 (b) and (e), removes the fin between the cells where needed. The gate is retained and can be contacted as before. The NW transistor is retained but the channel and gate are equipotential. The cross section corresponding to the cutting plane line shown in Fig. 12 (b) is given in Fig. 12 (e). The dashed arrow represents the cell boundary and the STI fin cut between the PMOS fins of the two abutting cells is apparent.

Fig. 13 (a) shows fins patterned using SAQP at a uniform pitch for the 111 SRAM cell and it is 160 nm in height. As in the standard cells, the spacers are merged. The MOL layers for the 111 cell (Fig. 13 (b)) do not drive the SRAM design rules any more than the 122 cell. However, apparent in Fig. 13 (c) and (d), the V_{ss} is not gridded on M1. Instead, V_{ss} is gridded on M2 and shared with adjoining cells. The V_{ss} and WL M1 connections are on the same track, which creates a tip-to-tip M1 spacing. This connection thus cannot be placed along the y-axis centerline, resulting in a 2-D M2 word-line.

DRCs often differ between SRAM and standard cell to either promote reliability or to enable higher density. The minimum COSD/COG to M1 design rule value, which includes the TDDB spacing specification, has been relaxed to 7 nm in SRAM cell as compared to 9 nm in standard cells by accounting for the M1 sidewall tapering angle of 86°, which results in its bottom edge to be pulled-in by 1.8 nm. Referring to Fig. 13 (c), this allows an 8 nm spacing between the M1 V_{dd} and the two neighboring COSD contacts that are wider than a single CD by 4 nm on each side. This decreased DRC value in turn enables full contact where COSD connects

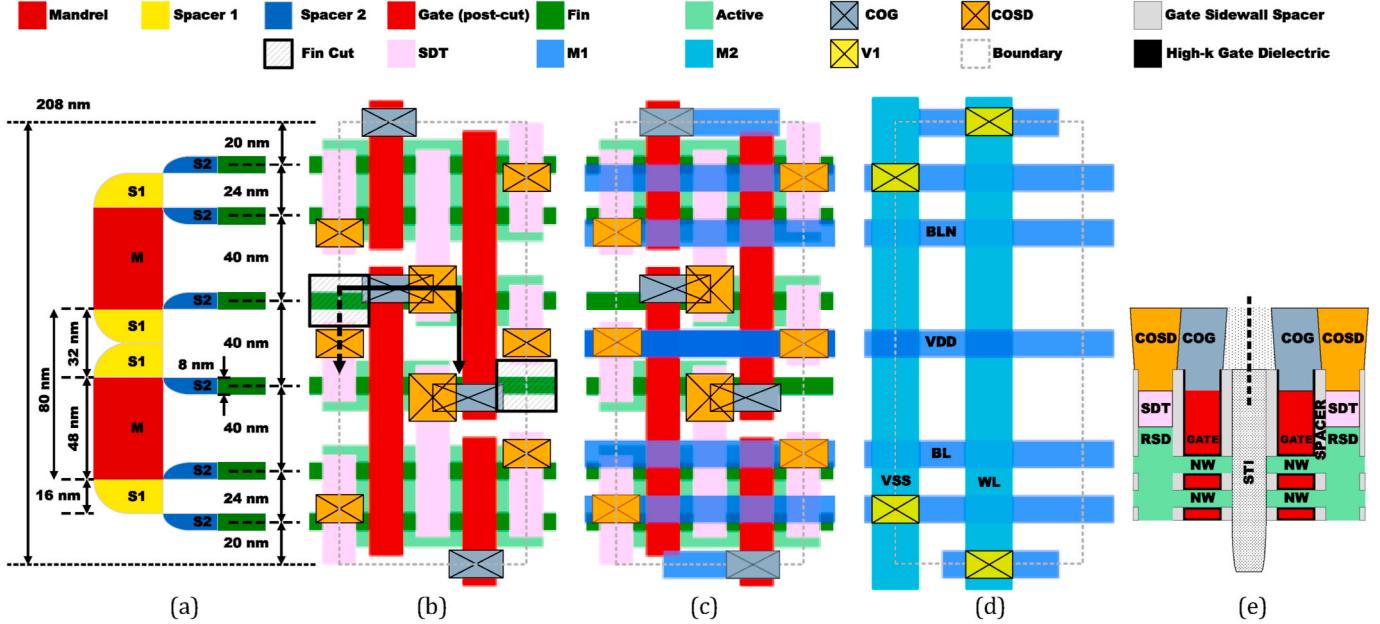


Fig. 12. (a) Nanowire (NW) patterning scheme for ASAP5 122 SRAM cell. The first level spacers (S1) are merged to preclude NW formation. 122 SRAM cell layout (b) without M1 and M2 for clarity, (c) with M1 and without M2, (d) and with only M1, V1, and M2. (e) Cross section showing STI fin cut use between two SRAM cells. It is symmetrical around the dashed line centered at the boundary between the two cells to separate their PMOS.

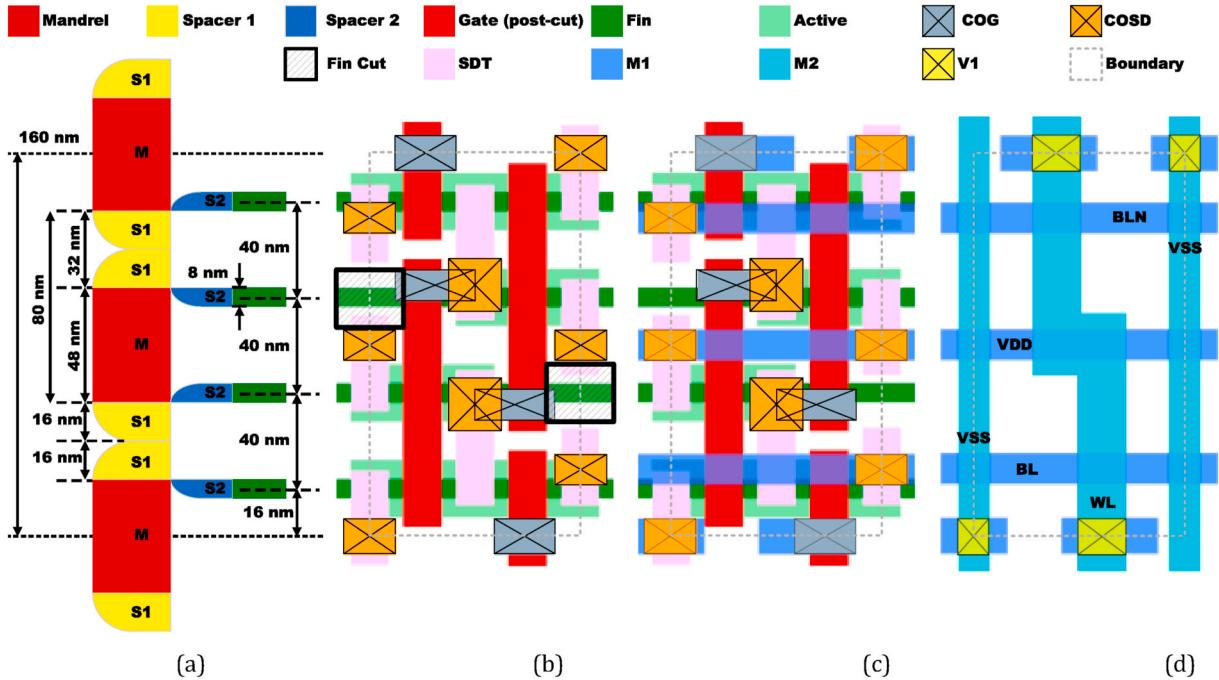


Fig. 13. (a) Nanowire (NW) patterning scheme for ASAP5 111 SRAM cell. 111 SRAM cell layout (b) without M1 and M2 for clarity, (c) with M1 and without M2, (d) with only M1, V1, and M2.

to COG (the NMOS drain to inverter gate) despite a 4 nm space variation between the high-NA EUVL patterned COG and COSD along the vertical axis. This prevents a high resistance contact, or in the worst-case the possibility of contact failure, i.e. open-circuit, due to an even larger space variation.

The relaxation of the minimum vertical extension of WELL layer past GATE from 5 nm (in logic) to 4 nm to enable a denser cell is yet another SRAM specific DRC. Several DRCs used for standard cells/logic are restrictive in nature and are intended to promote patterning regularity. However, these rules are forfeited in SRAMs for various reasons. For

instance, COSD vertical width is stipulated as exactly 13 nm in standard cells, but a larger vertical width is allowed in SRAMs to improve COG-COSD contact as discussed above.

7. Transistor electrical behavior

The 3-D TCAD (Section 3) used 12 nm L_{RSD} , corresponding to a 40 nm CGP, whereas we settled on a 16 nm L_{RSD} for ASAP5, i.e., a 44 nm CGP. The compact models reflect this change and are expanded to include the low V_t (LVT), super low (SLVT) and SRAM (which acts as

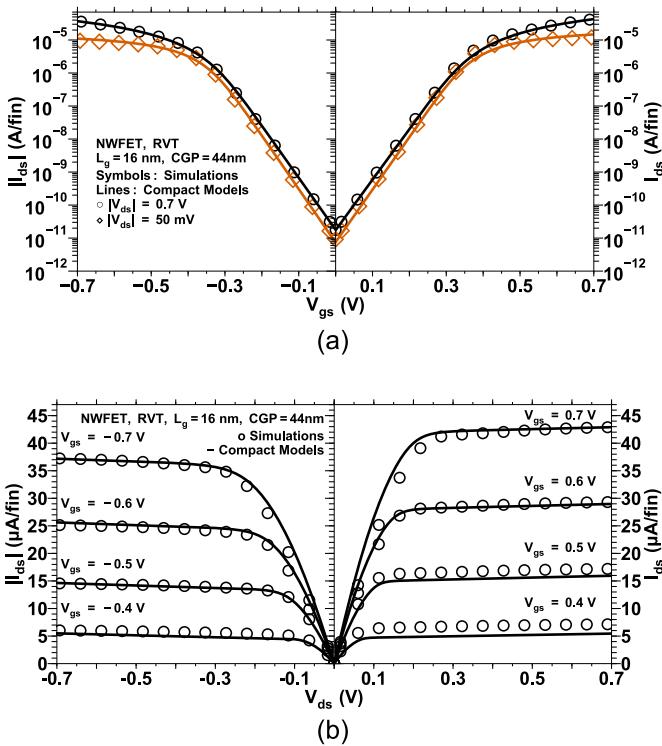


Fig. 14. (a) I_{ds} - V_{gs} and (b) I_{ds} - V_{ds} characteristics for the ASAP5 n-NWFET and p-NWFET RVT TT compact models and the 3-D TCAD simulations to which they were calibrated. The 44 nm CGP corresponds to 16 nm L_{RSD} . The simulated NWFETs comprise two nanowires per fin. All simulations are at nominal 0.7 V V_{DD} .

high V_t).

We did not scale the ASAP7 0.7 V supply voltage (V_{DD}) in our TCAD simulations [9]. Surprisingly, published foundry data have indicated the use of 0.7 V V_{DD} for an N7 process [24] and 0.75 V V_{DD} for same foundry's N5 process [53]. We chose a 17.7 pA/fin OFF-state ($V_{ds} = V_{DD}$, $V_{gs} = 0$ V) leakage current (I_{off}) target for the nominal RVT transistor by adjusting the metal gate work function [31].

7.1. Models

ASAP5 SPICE models use BSIM-CMG [90] calibrated to 3-D TCAD simulations at a 14 nm L_{eff} that corresponds to 16 nm drawn L_g (Section 3.3). Fig. 14 shows good compact model fits to the TCAD simulations for the RVT typical corner. NMOS I_{dsat} is $3.58 \times$ the I_{dlin} and $3.94 \times$ for the PMOS. The NMOS-to-PMOS I_{dsat} ratio for these transistors is approximately 1.15. All transistor characteristics are “per fin”, i.e., the drawn increment, comprised of a two nanowire vertical stack.

7.1.1. Transistor threshold voltages

The ASAP5 compact models support four threshold voltage devices, viz. super-low V_t (SLVT), low V_t (LVT), RVT, and SRAM (see Fig. 15). The former two enable high performance designs whereas the SRAM V_t devices allow low-leakage in SRAMs, retention latches, and other low-power designs. For the SRAM transistors the nominal RVT design parameters were preserved, with ϕ_{MG} modified to tune the transistor V_t in order to obtain characteristics that represented an optimal trade-off between I_{off} (<5 pA/fin), a large I_{on} to I_{off} ratio, and a low GIDL contribution to the total I_{off} (GIDL $<40\%$ I_{off}) [31]. We did not conduct new 3D-TCAD simulations for the SRAM transistors when we revised our CGP and L_{RSD} assumption to 44 nm and 16 nm, respectively. Instead, we used the calibrated compact models corresponding to aforementioned 40 nm CGP SRAM transistors and increased the I_{dsat} to obtain the compact

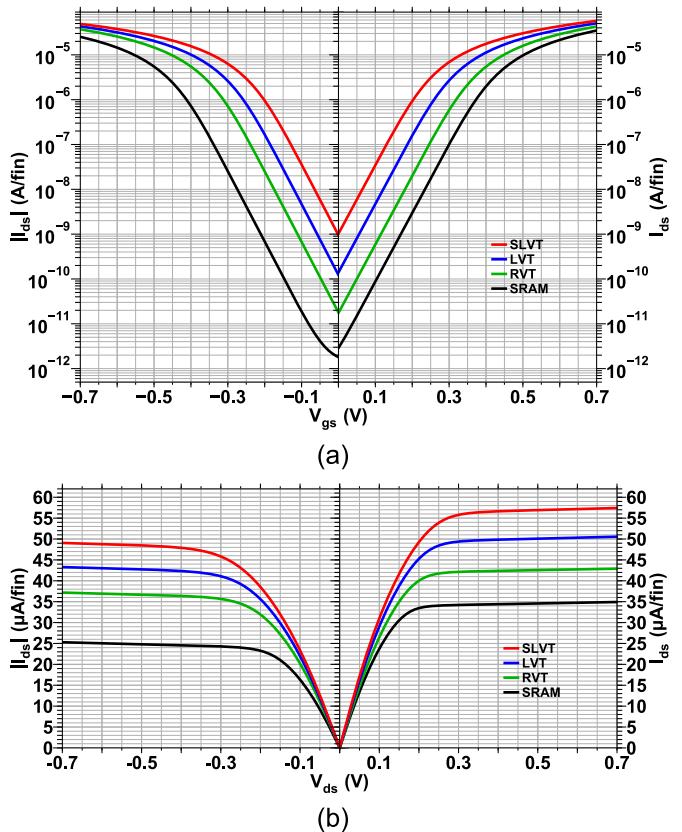


Fig. 15. ASAP5 n-NWFET and p-NWFET BSIM compact model (a) I_{ds} - V_{gs} and (b) I_{ds} - V_{ds} characteristics for different threshold voltage devices for the TT case. The simulated NWFETs comprise two nanowires per fin. All simulations are at nominal 0.7 V V_{DD} and 25 °C.

models for the 44 nm CGP SRAM transistors in order to account for the larger RSD of the former.

7.2. Corners

Transistor corners for the ASAP5 include TT, slow-slow (SS), fast-fast (FF), slow-fast (SF), and fast-slow (FS). The latter two corners were absent in ASAP7 and have been included with ASAP5 to enable users designing SRAMs, ratioed and other domino circuits without having to split the models themselves. In ASAP7 we had made SF and FS corners for our use by simply separating the P and N in the FF and SS corners. Given the absence of literature on creating split corner models, we suspect that the WF metal deposition may be the primary cause for the FS and SF corners, since all the other steps appear to affect both NMOS and PMOS. In the end, we produced all corners by modifying the same parameters as those modified for ASAP7 models for consistency.

Fig. 16 (a) shows the NMOS and PMOS I_{dsat} vs. I_{off} characteristics for different transistor V_t flavors at the TT, FF, and SS corners. As evident, I_{off} increases by approximately one order of magnitude from one V_t to another at a particular corner for most transistors. V_{tsat} , I_{off} , and I_{dsat} corner plots are shown in Fig. 16 (b), (c), and (d), respectively, for different transistor V_t flavors. V_t is computed using constant current at 50 nA I_{ds} .

Key transistor parameters for the NMOS and PMOS at the TT corner are shown in Table 8 and Table 9, respectively. ASAP5 transistors have larger I_{dsat} and lower I_{off} compared to ASAP7 transistors owing to the transistor architecture. They also exhibit good SS and DIBL values, similar to those reported by Kim et al. for the same D_{nw} [91].

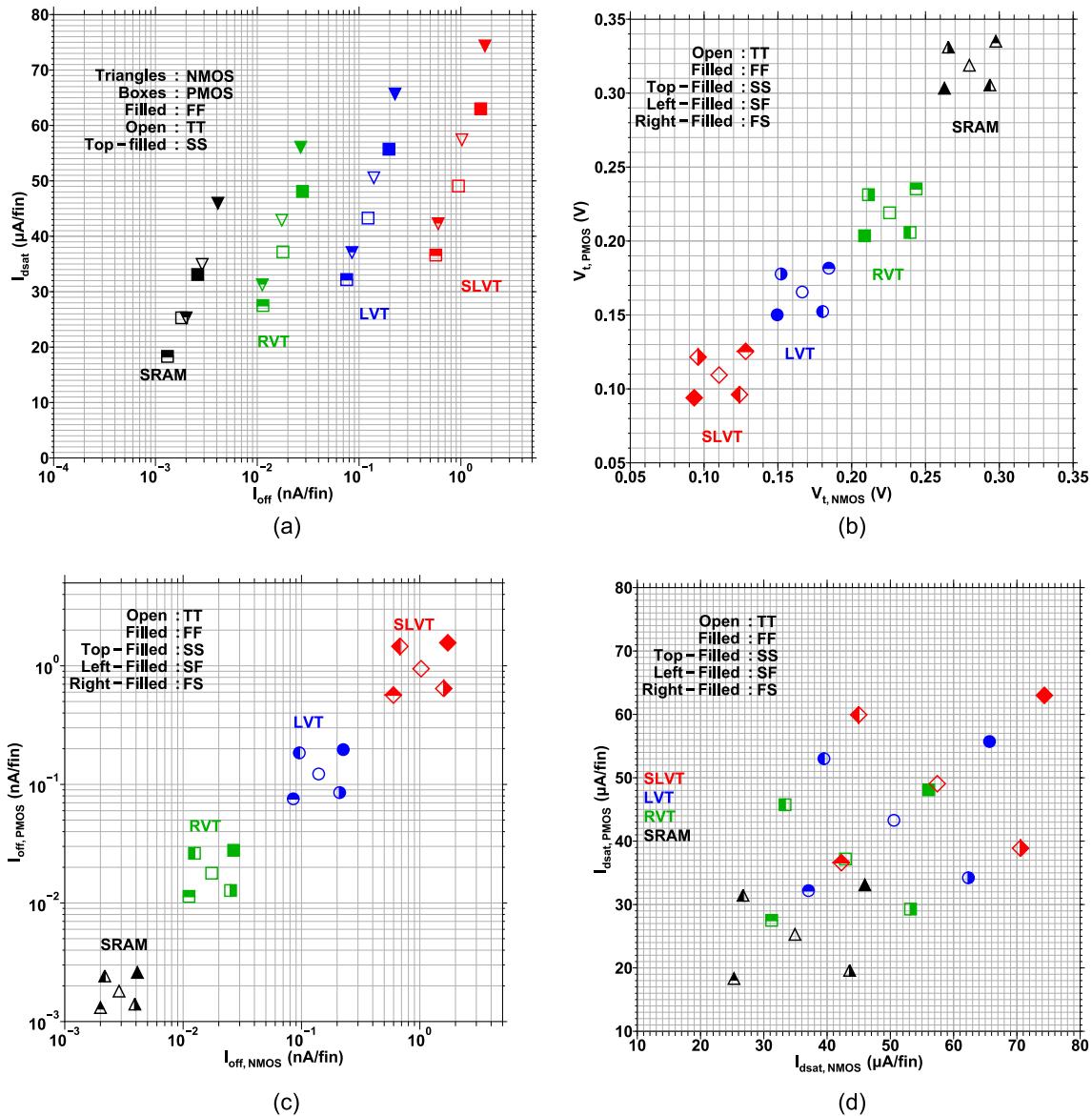


Fig. 16. (a) Transistor I_{dsat} vs. I_{off} characteristics at the TT, FF, and SS process corners. NMOS vs. PMOS (b) V_t (as computed with VTC), (c) I_{off} , and (d) I_{dsat} at the TT, FF, SS, SF, and FS corners from HSPICE simulations at nominal 0.7 V V_{DD} and 25 °C. The simulated NWFETs comprise two nanowires per fin.

Table 8

ASAP5 NMOS NWFET ($L_g = 16 \text{ nm}$, $L_{eff} = 14 \text{ nm}$) TT corner parameter (per fin) at 25 °C.

	SRAM	RVT	LVT	SLVT
I_{dsat} ($\mu\text{A}/\text{fin}$)	34.92	42.90	50.55	57.42
I_{off} (pA/fin)	2.87	17.43	139.67	1023.93
V_{tsat} (V)	0.280	0.226	0.166	0.110
DIBL (mV/V)	20.06	22.11	26.35	27.69
SS (mV/dec)	66.07	66.07	66.02	65.99
GIDL (pA/fin)	0.35	0.31	0.31	0.31

8. Summary and future work

This paper has presented an overview of the ASAP5 5-nm PDK including the key assumptions. We justified the design rules and electrical performance based on the literature. Besides basing the PDK on NWFETs, ASAP5 incorporates significant improvements compared to ASAP7, which are commensurate with those employed by foundries at the N5 node, e.g., single diffusion breaks, contact over active gate, fully

Table 9

ASAP5 p-NWFET ($L_g = 16 \text{ nm}$, $L_{eff} = 14 \text{ nm}$) TT corner parameter (per fin) at 25 °C.

	SRAM	RVT	LVT	SLVT
I_{dsat} ($\mu\text{A}/\text{fin}$)	25.29	37.18	43.29	49.06
I_{off} (pA/fin)	1.80	17.85	122.45	945.84
V_{tsat} (V)	-0.319	-0.219	-0.165	-0.109
DIBL (mV/V)	27.93	27.98	29.16	29.53
SS (mV/dec)	64.56	64.60	64.51	64.49
GIDL (pA/fin)	1.35	0.54	0.52	0.50

self-aligned vias, as well as improved interconnect materials and modeling. The compact model fits are TCAD based. Standard cell and SRAM layouts have been demonstrated using the PDK. Moreover, the fin/NW mandrel schemes have been shown as compatible between the SRAM and standard cell patterning.

At this time, the interconnect models in the PDK do not account for self-heating and electromigration. As the PDK will be in the public domain, we hope that its users will contribute to further development

that may involve the incorporation of these effects in the PDK.

Standard cell libraries for ASAP5 are under development and will be released with other collaterals for synthesis and automated place-and-route enablement in near future.

Author statement

Vinay Vashishtha: Conceptualization; Data curation; Formal analysis; Investigation; Methodology; Project administration; Resources; Software; Validation; Visualization; Roles/Writing - original draft; Writing – review & editing. Lawrence T. Clark: Conceptualization; Data curation; Formal analysis; Funding acquisition; Investigation; Methodology; Project administration; Resources; Software; Supervision; Validation; Visualization; Roles/Writing - original draft; Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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