**Verilog Project**

**Project Overview:**

During the course of this project you will be required to design a limited version MIPS processor. The processor will support a limited number of instructions and functionalities. The processor needs to be tested for the supported functionalities. All design and test aspects should be well documented.

**Deadline & Submission Process:**

* The project along with its report are due by: **Noon 19th Dec 2019**.
* All submissions are via email to: [a.almousa@psut.edu.jo](mailto:a.almousa@psut.edu.jo)
* The subject of the email should include your team #.
* Delivery past the deadline will result in **ZERO** credit.
* The Project Report should be in docx format (~10 Pages. Not more than 15, single spaced, Font: Times New Roman size11)
* Submission should be a **ONE** zipped file names (Group\_#.zip) that include the following:

1. Honor Statement, signed by ALL members of the team. “We, signing below, swear that the work submitted in this report is done entirely by our team. And that we have not copied anything from any other resource”
2. Project Report that included the following:
   * **Design Block Diagram:** with detailed description of each module and its functionality.
   * Design Analysis
   * Test Cases discussion
   * Test Cases results discussion
   * Conclusion
3. Design & Test Verilog files; Top file names (top.v) and test cases names tb\_1.v, tb\_2.v …etc.
4. Run logs: the run result for each test case: tb\_1.txt ..etc.

**Tools:**

Use the following Verilog simulator (or any one of your choice)

* Download Verilog from: <http://bleyer.org/icarus/>

**Requirements:**

You are required to develop the following:

* A limited version of a 32 bit-MIPS processor. Instruction set is based on the attached excel sheet.
* The processor should have the support for the following instructions – at least:
  1. All the core instruction set.
  2. The highlighted Floating Point.
* The Design should include ALU-ALU and MEM to ALU-Forwarding.
* No Handling for Control Hazards is required.
* Two separate Instruction and Data Memories (each of size 1024x1bytes).
* At minimum there should be 10 test benches that cover:
  1. Add
  2. Addi
  3. Multiply
  4. Beq
  5. J
  6. LW
  7. SW
  8. SLL
  9. SLT
  10. JR