DATA SHEET

GPR27P512A

512M-BIT NAND INTERFACE OTP

Nov. 21, 2011

Version 1.5

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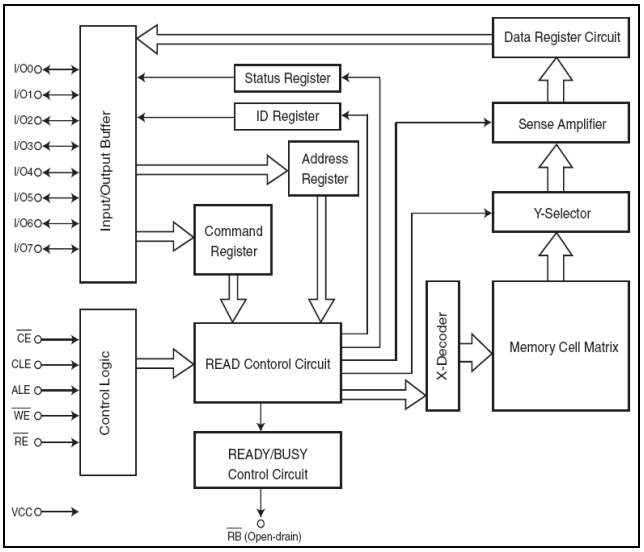
512M-BIT NAND INTERFACE OTP

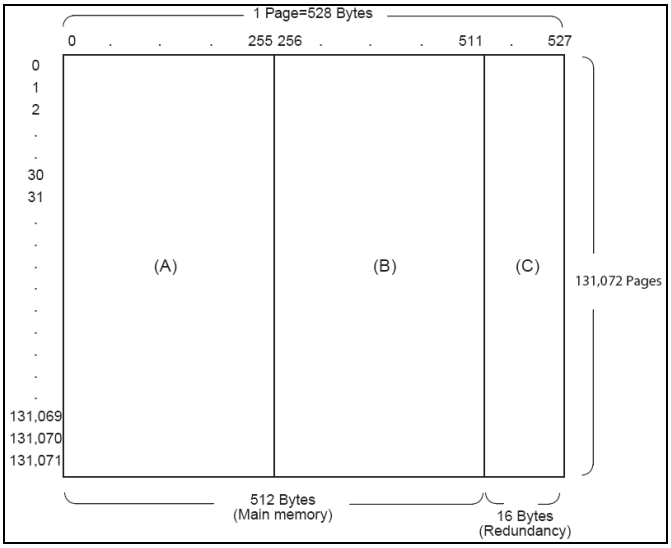
1. FEATURES

- Word organization
  - (67,108,864 + 2,097,152[Note]) words by 8 bits
- Page size
  - (512 + 16[Note]) by 8 bits

  Note: Underlined parts are redundancy and fixed to all FFH.
- Operation mode
  - READ mode (1), READ mode (2), READ mode (3), RESET, STATUS READ, ID READ
- Operating supply voltage : VCC = 2.7~3.6V
- Access Time
  - Memory cell array to starting address: 25us (MAX.)
  - Read cycle time: 25ns (MIN.)
  - $\overline{RE}$ access time: 20ns (MAX.)
- Operating supply current
  - During read: 30mA (MAX.) (25ns cycle operation)
  - During standby (CMOS): 10uA(Typ.), 50uA(Max.)
- Package Type
  - 48-pin TSOP(I) (12mmx20mm)

2. BLOCK DIAGRAM





The start address (SA) during read operation is specified divided into three areas using three types of read commands.

- In read mode (1), start address (SA) is set in area (A).
- In read mode (2), start address (SA) is set in area (B).
- In read mode (3), start address (SA) is set in area (C).

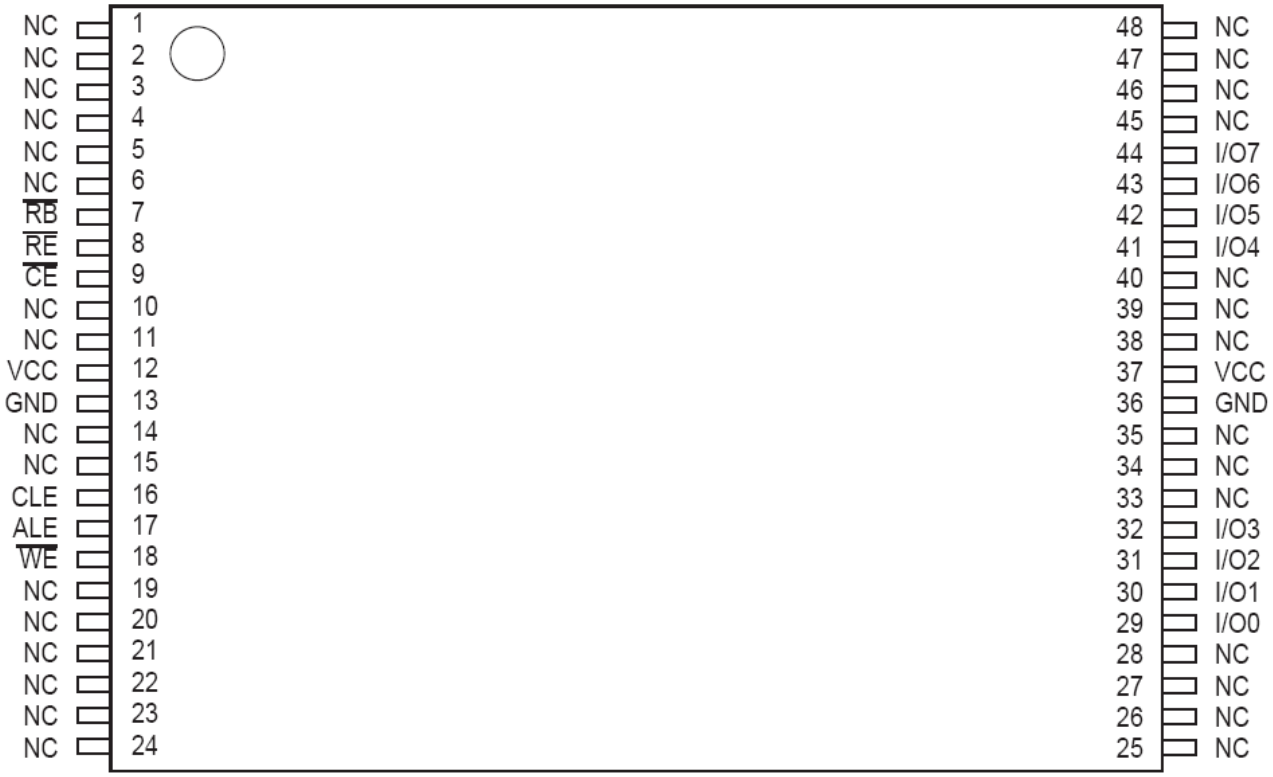
One page consists of a total of 528 bytes broken down into 512 bytes (main memory) and 16 bytes (redundancy).

Caution The data of area (C) is redundancy, which is not programmable and is fixed to all FFH.

3. 48 TSOP PIN DESCRIPTIONS

PIN No	Name	Normal Function Description
29-32, 41-44	I/O0~I/O7	Address Input/Command Inputs/Data Outputs
16	CLE	Command Latch Enable
17	ALE	Address Latch Enable
18	$\overline{WE}$	Write Enable
8	$\overline{RE}$	Read Enable
9	$\overline{CE}$	Chip Enable
7	$\overline{RB}$	READY/BUSY pin
12, 37	VCC	Supply Voltage
1-6, 10-11, 14-15, 19-28, 33-35, 38-40, 45-48	NC	No Connection
13, 36	GND	Ground

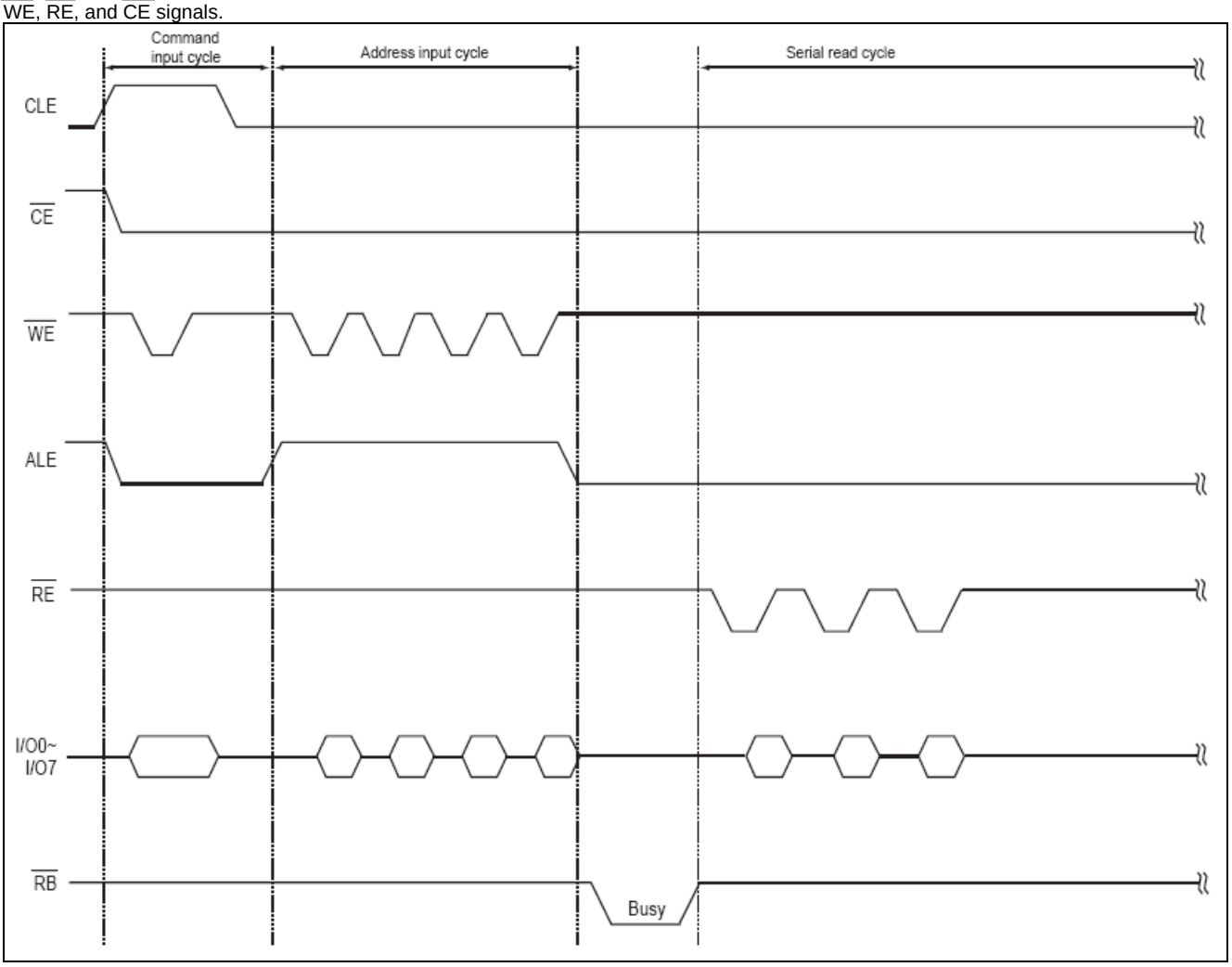
3.1. PIN Assignment



4. FUNCTIONAL DESCRIPTIONS

4.1. Operation Modes

Command input, address input, and serial read are all performed from I/O pins, and the respective statuses are controlled by the CLE, ALE, $\overline{WE}$, $\overline{RE}$, and $\overline{CE}$ signals.



4.2. Operation Mode

Mode	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$
Command input cycle	H	L	L	⎍	H
Address input cycle	L	H	L	⎍	H
Serial read cycle	L	L	L	H	⎎

4.3. Operation Mode during Serial Read

Mode	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O0 - I/O7
Data output	L	L	L	H	L	Data output
Output Hi-Z	L	L	L	H	H	Hi-Z

Remark : VIH or VIL

4.4. Operation Commands

The following six operation settings are possible by inputting commands from I/O pins.

Command	Hex	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Command receivable during Busy
Read mode(1)	00	L	L	L	L	L	L	L	L	
Read mode(2)	01	L	L	L	L	L	L	L	H	
Read mode(3) Note1	50	L	H	L	H	L	L	L	L	
Reset Note2	FF	H	H	H	H	H	H	H	H	○
Status read	70	L	H	H	H	L	L	L	L	○
ID read Note3	90	H	L	L	H	L	L	L	L	

Note1: The data output in read mode (3) is all FFH.

Note2: The only commands that can be executed when the device is Busy are the reset command and status read command. Do not set any of the other commands while the device is Busy.

Note3: For ID read, input "00" during the first address cycle after setting a command.

4.5. I/O Pin Correspondence Table during Address Input Cycle (Address Setting)

4.5.1. When 00H or 01H command is set [Read Mode (1), Read Mode (2)]

Command	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st address cycle	L	L	L	L	L	L	L	L
2nd address cycle	A16	A15	A14	A13	A12	A11	A10	A9
3rd address cycle	A24	A23	A22	A21	A20	A19	A18	A17
4th address cycle	L	L	L	L	L	L	A26	A25

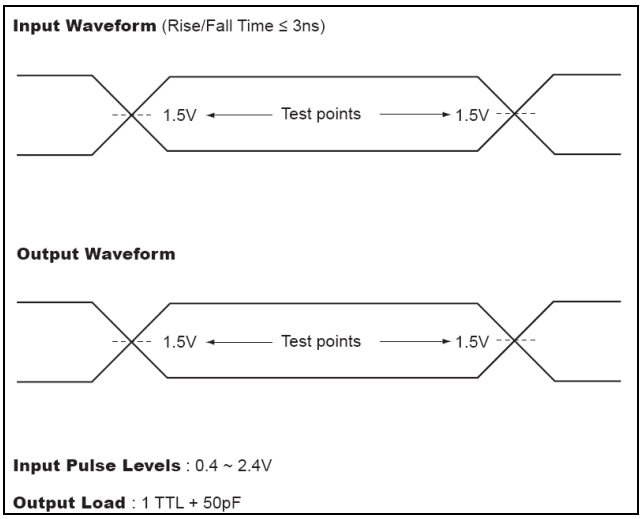
4.5.2. When 50H command is set [Read Mode (3)]

Command	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st address cycle	X	X	X	X	L	L	L	L
2nd address cycle	A16	A15	A14	A13	A12	A11	A10	A9
3rd address cycle	A24	A23	A22	A21	A20	A19	A18	A17
4th address cycle	L	L	L	L	L	L	L	A25

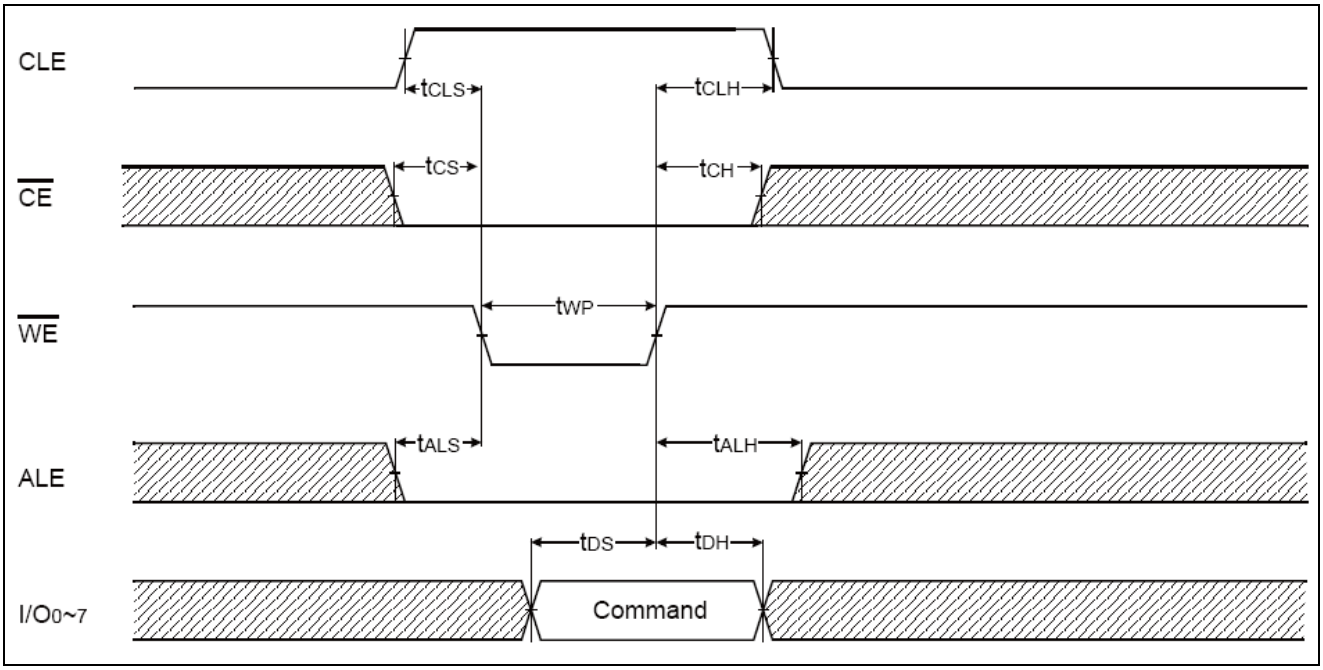
Remarks:

1. A0 to A25 are internal addresses.
2. Internal address A8 is set internally with command 00H or 01H.
3. When 00H command is set [read mode (1), (2)], the I/O0~ I/O7 inputs of the 1st address cycle are VIL.
4. When 50H command is set [read mode (3)], the I/O4, I/O5, I/O6, and I/O7 inputs of the 1st address cycle are VIH or VIL.

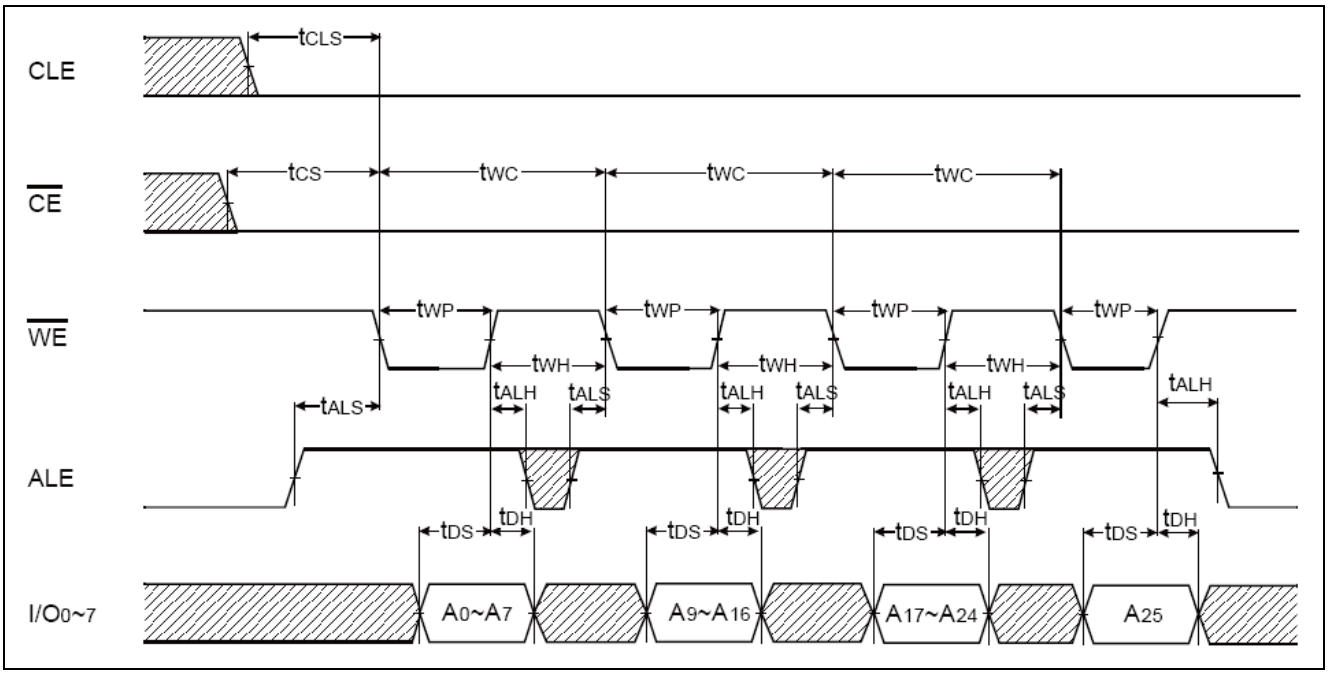
4.6. AC Test Conditions



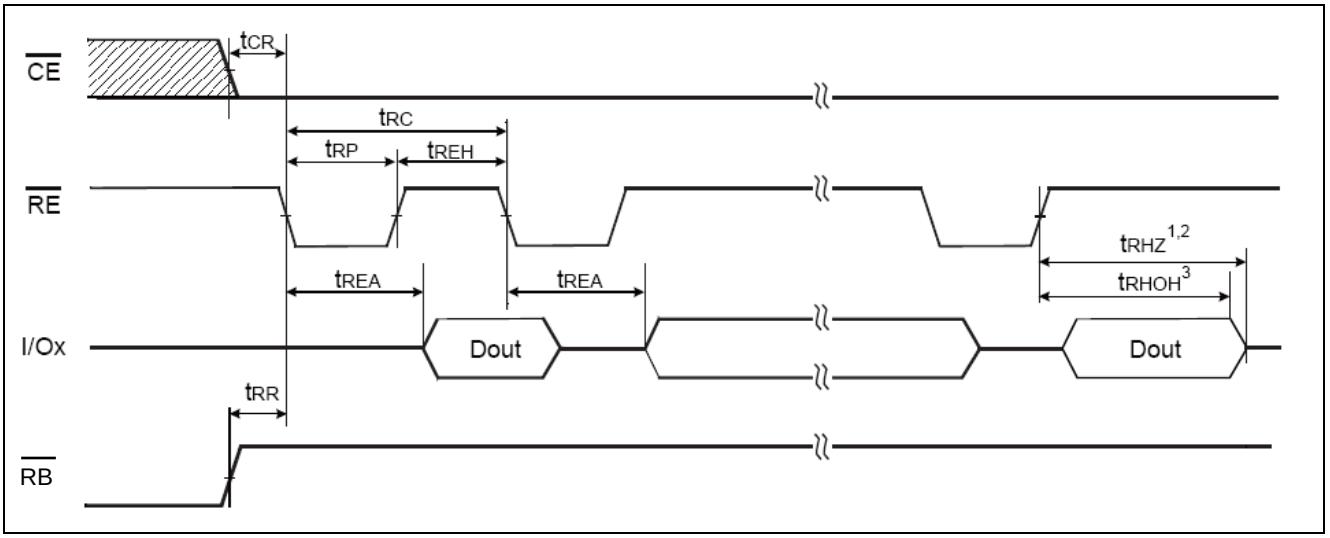
4.7. Command Latch Cycle



4.8. Address Latch Cycle



4.9. Serial Access Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)

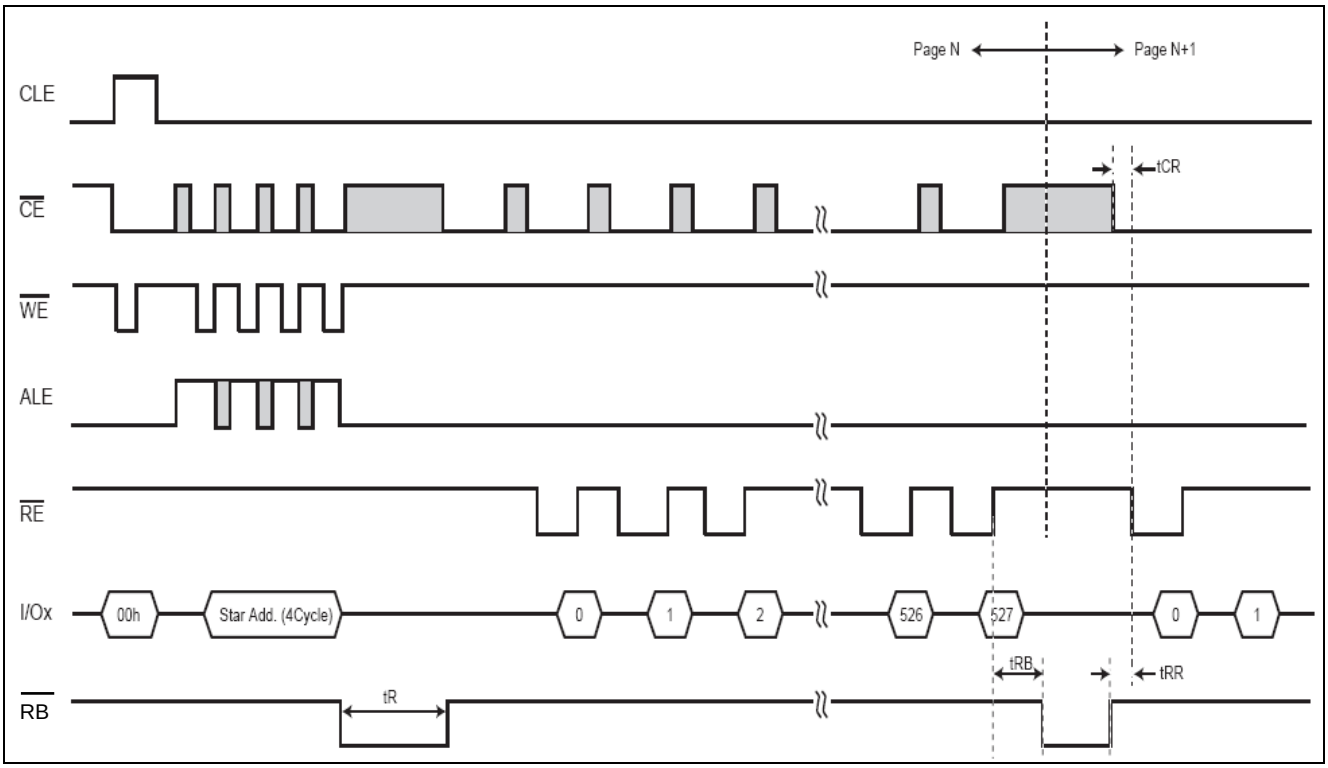


Note1: Transition is measured at ±200mV from steady state voltage with load.

Note2: This parameter is sampled and not 100% tested.

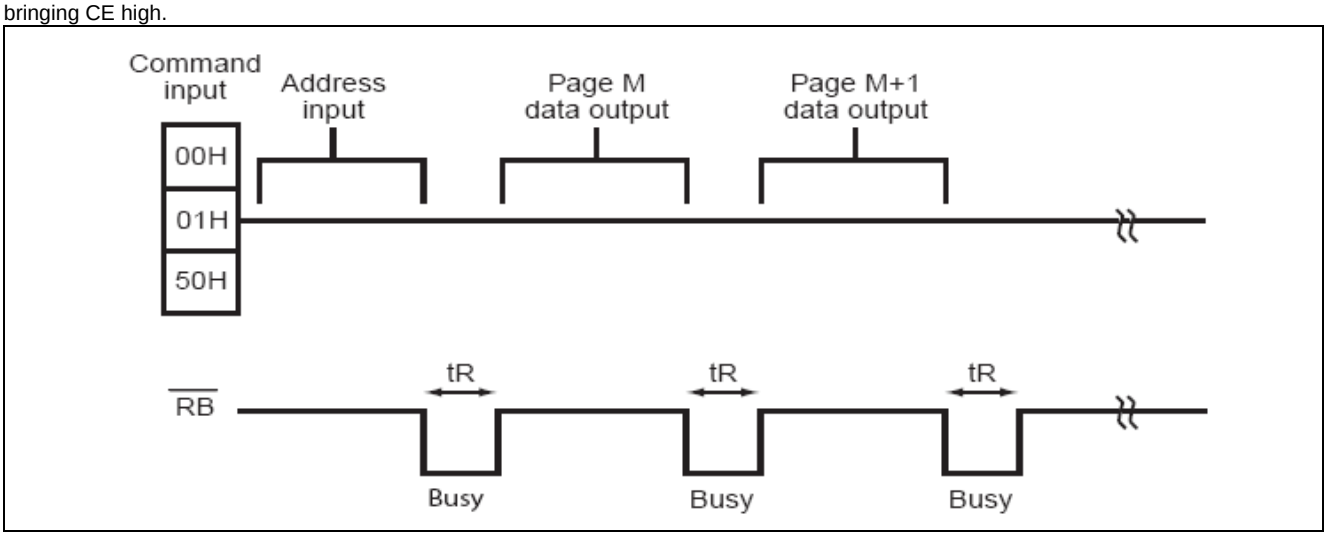
Note3: tRHOH starts to be valid when frequency is lower than 33MHz.

4.10. Read Operation with $\overline{CE}$ Don't Care

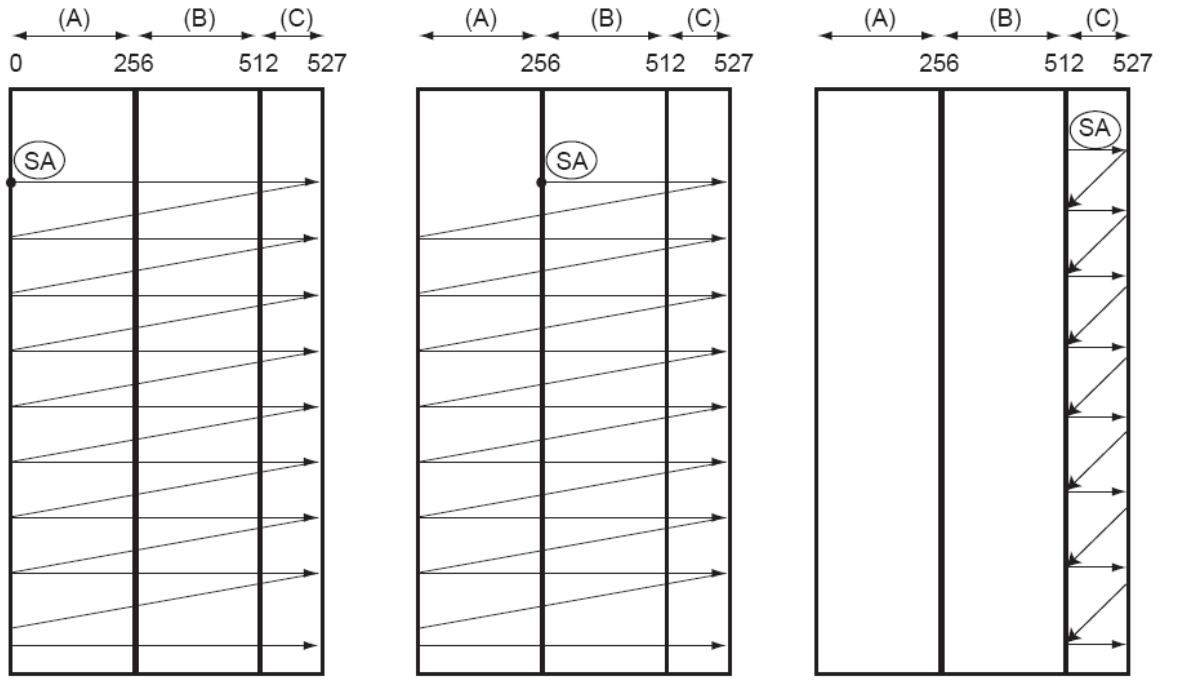


4.11. Sequential Read

In read modes (1), (2), and (3), when a command (00H, 01H, 50H) is input and an address specified, the address is automatically incremented and the read operation is continuously performed, by inputting the $\overline{RE}$ clock. At this time, a Busy period (tR) occurs after the last address is accessed in a page. After the last address of the page is read out, the sequential read operation can be terminated by bringing $\overline{CE}$ high.



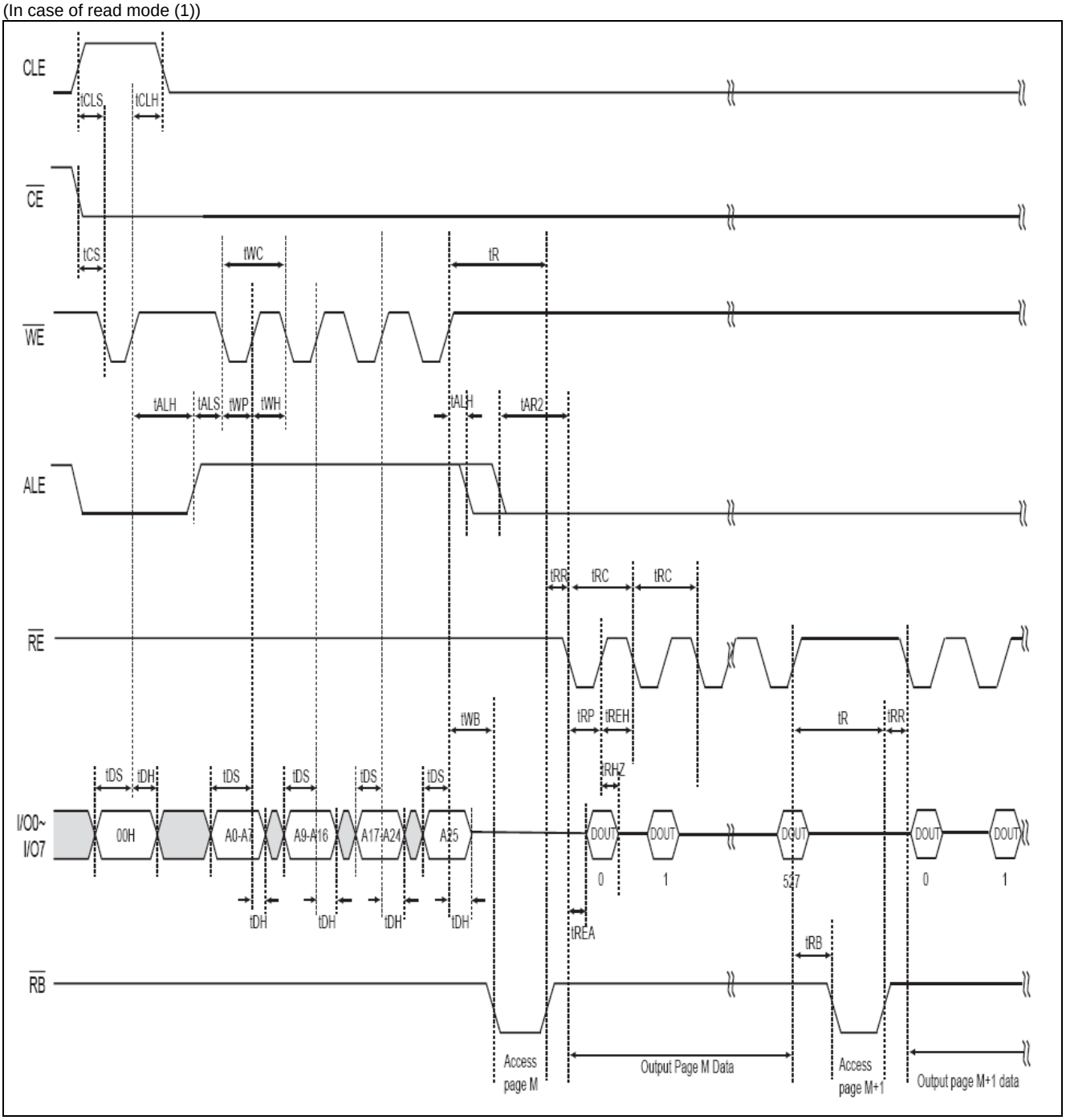
4.12. Relationship between Command and Start Address (SA) during Sequential Read



- When the "00H" command is set, (SA) is set to area (A) and start from 0th address.
- When the "01H" command is set, (SA) is set to area (B) and start from 256th address.
- When the "50H" command is set, (SA) is set to area (C) and start from 512th address.

4.13. Sequential Read Cycle Timing Chart(1)

(In case of read mode (1))

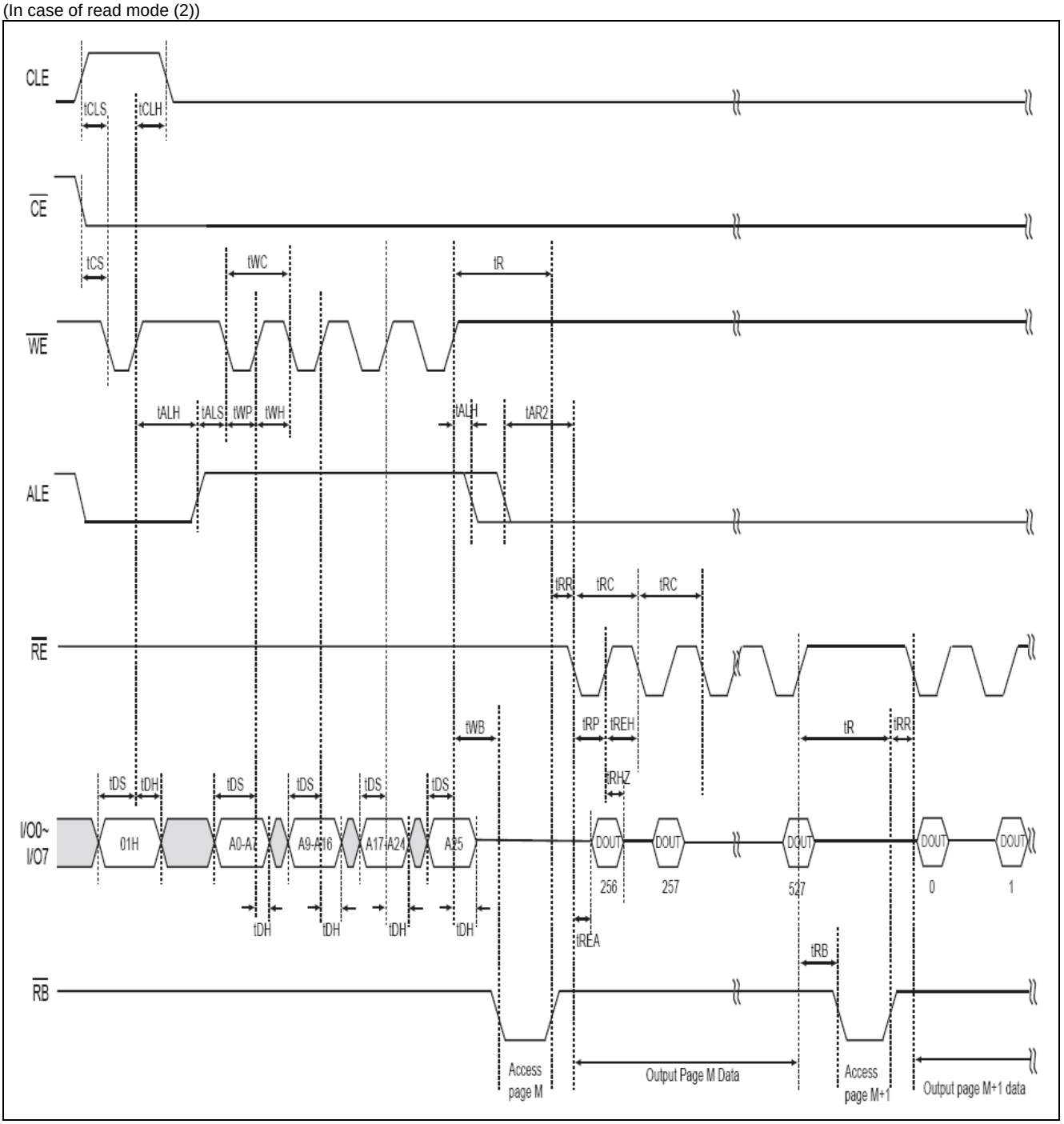


Remark:

1.Start address (SA) specification when read is performed with command 00H.

4.14. Sequential Read Cycle Timing Chart(2)

(In case of read mode (2))

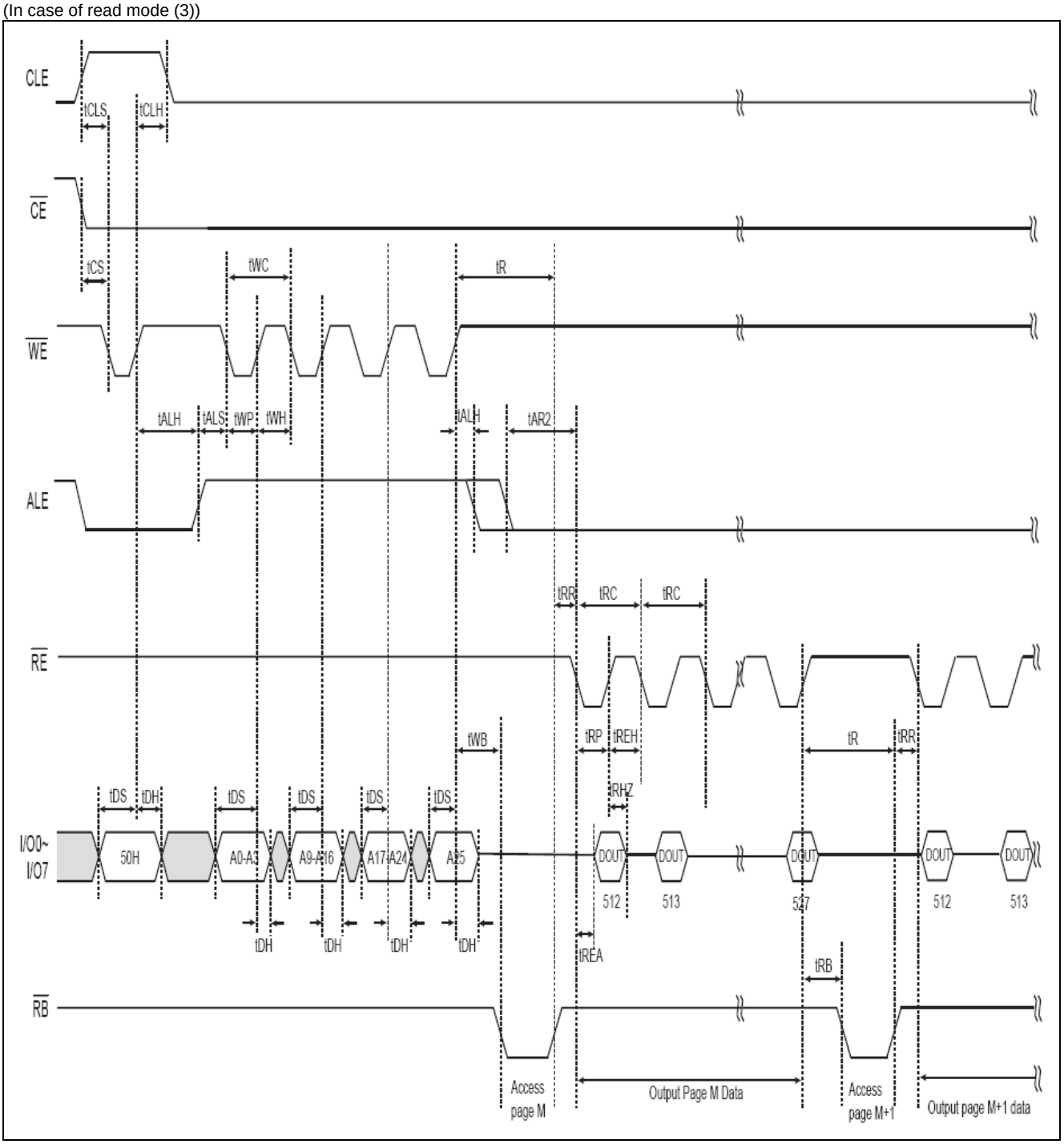


Remark:

1.Start address (SA) specification when read is performed with command 01H.

4.15. Sequential Read Cycle Timing Chart(3)

(In case of read mode (3))

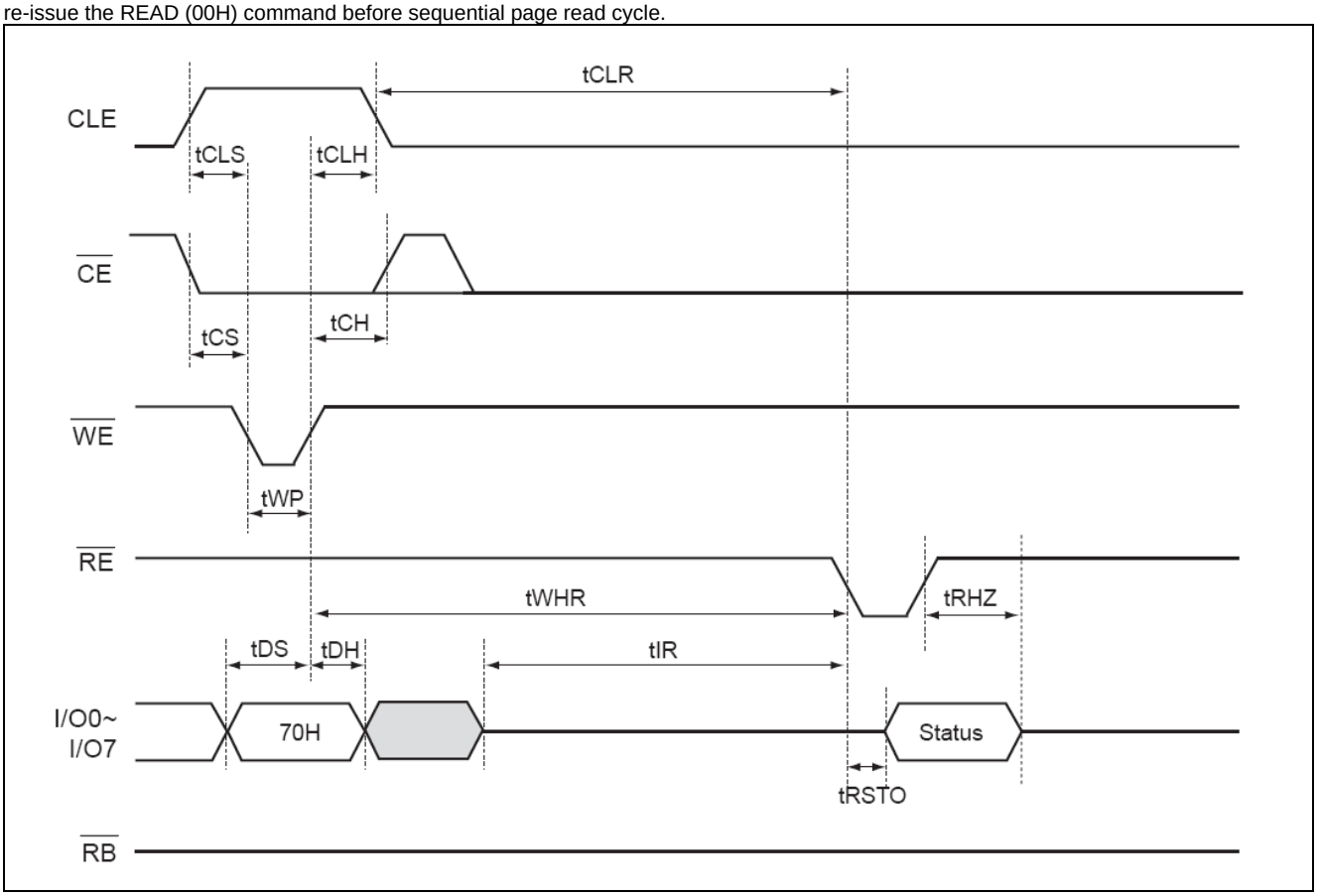


Remark:

1.Start address (SA) specification when read is performed with command 50H.

4.16. Status Read

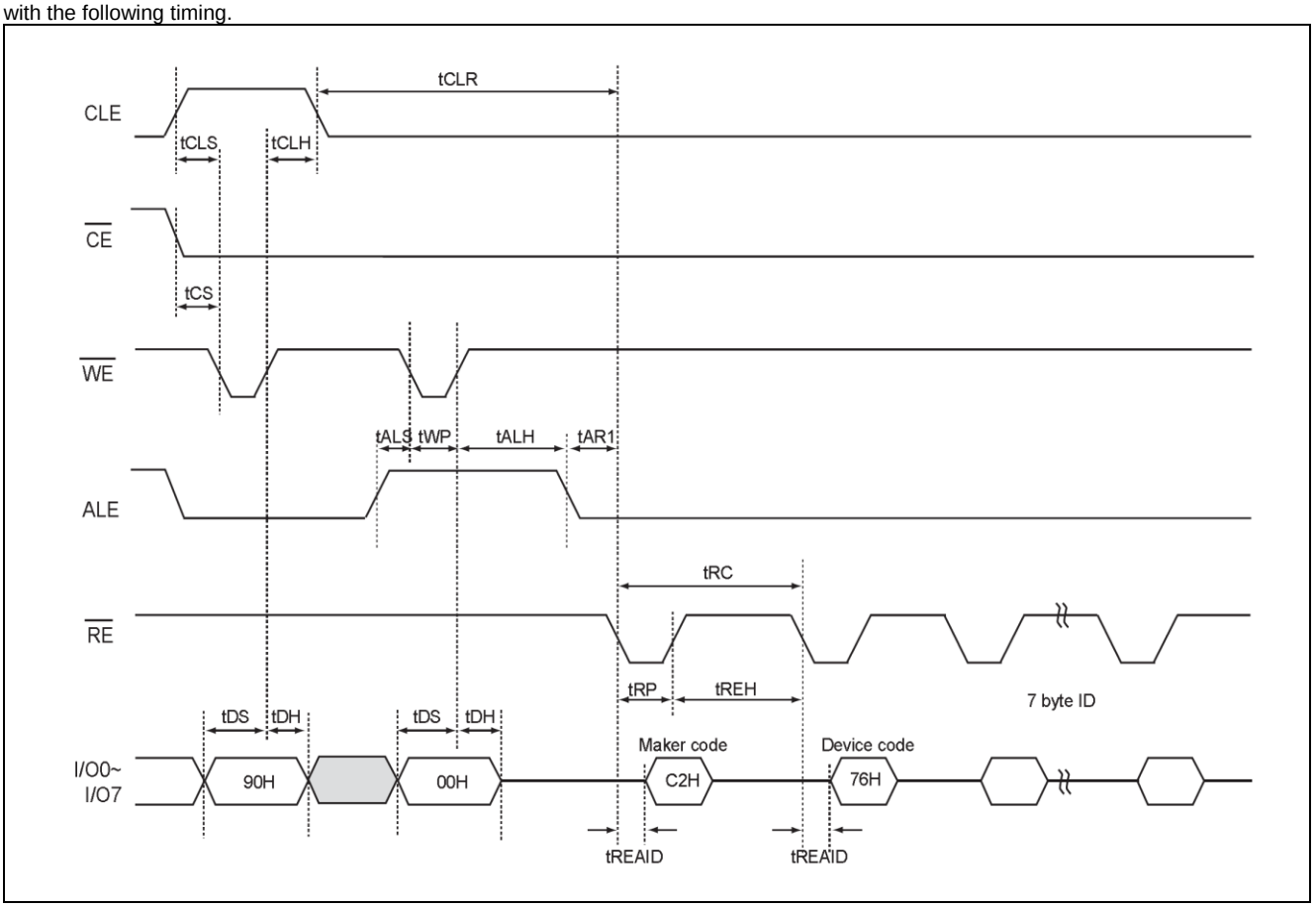
Status information can be output from the I/O pins with the $\overline{RE}$ clock following input of the 70H command. Status read is a function to recognize the status of the device from external. If the READ STATUS command is used to monitor the status of the device, user must re-issue the READ (00H) command before sequential page read cycle.



	Status	Status Output Data[NOTE]
I/O0	Ready / Busy	0 / 1
I/O1	Not used	0
I/O2	Not used	0
I/O3	Not used	0
I/O4	Not used	0
I/O5	Not used	0
I/O6	Ready / Busy	1 / 0
I/O7	Write protect	0

4.17. ID Read

To recognize the ID code (maker code / device code) of this device in a system, execute the ID read command. The ID code can be read with the following timing.

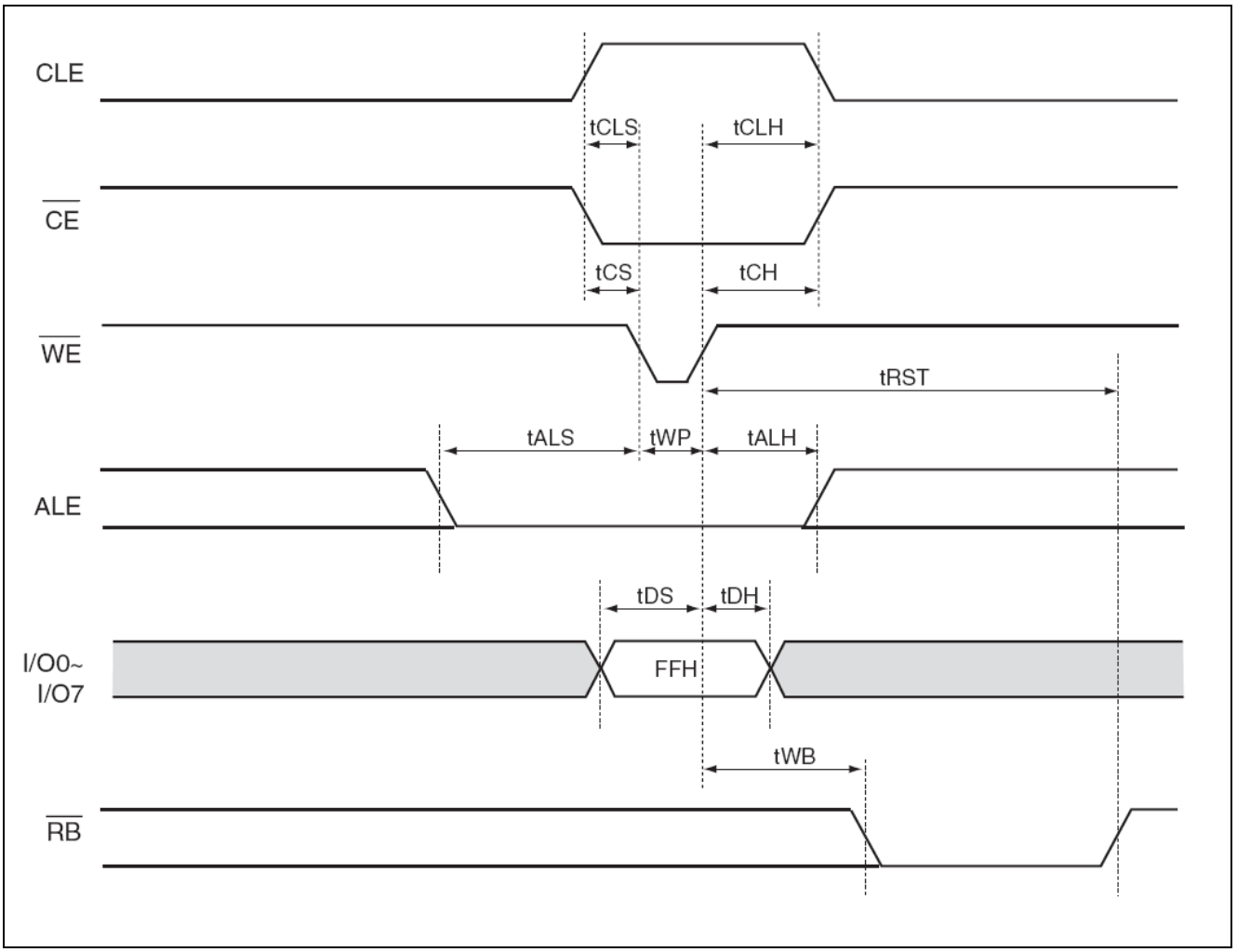


	Value	Description
1st Byte	C2H	Maker Code
2nd Byte	76H	Device Code
3th Byte	reserved	Unique ID
4th Byte	reserved	
5th Byte	reserved	
6th Byte	reserved	
7th Byte	reserved	
8th Byte	reserved	Title ID
9th Byte	reserved	

Notes:

1. GPR27P512A reserves 2 bytes for Title ID and 5 bytes for Unique ID. The 2-byte Title ID can be assigned by customers to represent each of their content. The 5-byte Unique ID has different value on each piece of chip, Generalplus has a method to produce each silicon die with different ID.
2. Do not input an address other than 00H after setting the ID read command (90H). If an address other than 00H is input, the data following $\overline{RE}$ clock input is not guaranteed.

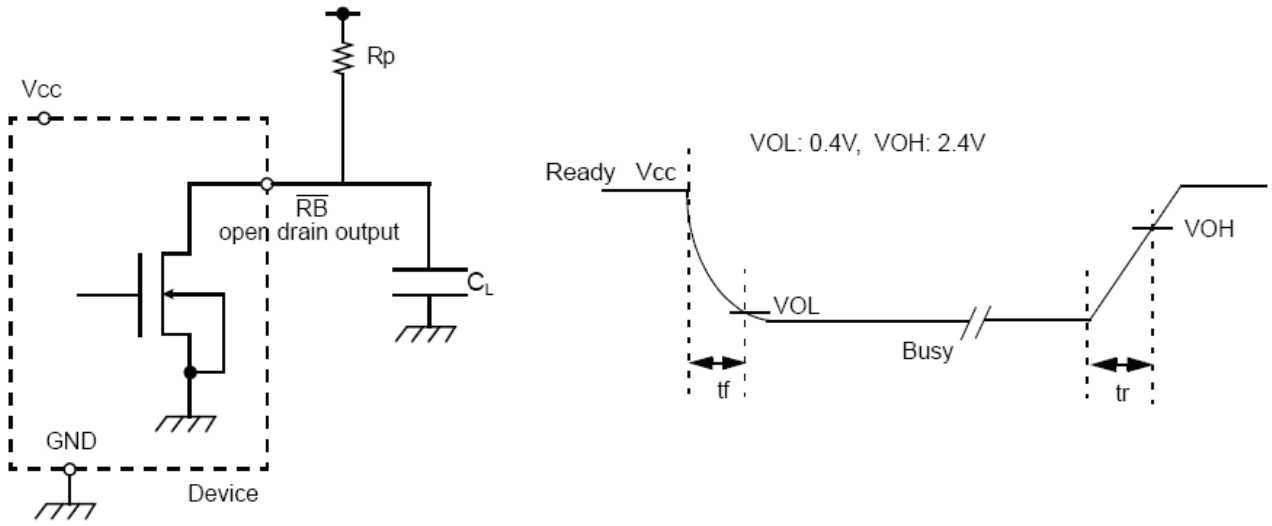
4.18. Reset Cycle Timing Chart



4.19. READY/BUSY

The device has a $\overline{RB}$ output that provides a hardware method of random read completion. The $\overline{RB}$ pin is normally high but transitions to low after random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more $\overline{RB}$ outputs to be Or-tied. Because pull-up resistor value is related to tr($\overline{RB}$), an appropriate value can be obtained with the following reference table (Rp vs tr, tf).

Rp vs tr, tf (V_{CC}=3.3V, Ta=25°C, CL=50pF)



Rp	1K	2K	3K	4K	5K	10K
tf/tr	11n/67n	11n/131n	11n/195n	11n/263n	11n/335n	11n/664n

4.20. Usage Cautions

4.20.1. Rated operation

Operation using timing other than shown in the timing charts is not guaranteed.

4.20.2. Commands that can be input

The only commands that can be input are 00H, 01H, 50H, 70H, 90H, and FFH. Do not input any other commands. If other commands are input, the subsequent operation is not guaranteed.

4.20.3. Command limitations during Busy period

Do not input commands other than the reset command and status read command during the Busy period. If a command is input during the Busy period, the subsequent operation is not guaranteed.

4.20.4. Cautions regarding $\overline{RE}$ clock

- Following the last $\overline{RE}$ clock, do not input the $\overline{RE}$ clock until the $\overline{RB}$ pin changes from Busy to Ready.
- Do not input the $\overline{RE}$ clock other than during data output.

4.20.5. Cautions upon power application

Since the state of the device is undetermined upon power on, input high level to the $\overline{CE}$ pin and execute the reset command following power on.

4.20.6. Cautions during read mode

- Perform address input immediately following command input. If address input is done without performing command input first, the correct data cannot be output because the operation mode is undetermined.
- To execute the read mode after the read mode has been stopped with the reset command (FFH) and $\overline{CE}$, input again a command and address.

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VCC	-0.5 to +4.6	V
Input Voltage	VI	-0.3 to VCC+0.3	V
Input / Output Voltage	VI/O	-0.3 to VCC+0.3 (≤ 4.6)	V
Operating Ambient Temperature	TA	0 to 70	˚C
Storage Temperature	Tstg	-65 to +150	˚C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

5.2. Capacitance (TA = 25°C)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input Capacitance	CI	f = 1 MHz	-	-	10	pF
Output Capacitance	CO		-	-	10	pF

5.3. DC Characteristics (TA = 0 to 70°C, VCC = 2.7~3.6V)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
High Level Input Voltage	VIH	-	2.0	-	VCC+0.3	V
Low Level Input Voltage	VIL	-	-0.3	-	+0.8	V
High Level Output Voltage	VOH	IOH =-400uA	2.4	-	-	V
Low Level Output Voltage	VOL	IOL = 2.1mA	-	-	0.4	V
Input Leakage Current	ILI	VI = 0 V to VCC	-	-	±10	uA
Output Leakage Current	ILO	VO = 0 V to VCC	-	-	±10	uA
Power Supply Current in Read	ICCO1	$\overline{CE}$ = VIL, IOUT =0mA, tCYCLE = 25ns	-	-	30	mA
Power Supply Current in Command Input	ICCO3	tCYCLE = 25ns	-	-	30	mA
Power Supply Current in Address Input	ICCO5	tCYCLE = 25ns	-	-	30	mA
Standby Current (CMOS)	ICCS2	$\overline{CE}$ = VCC-0.2 V	-	10	50	uA
$\overline{RB}$ Pin Output Current	IOL(RB)	VOL = 0.4 V	-	8	-	mA

5.4. AC Characteristics (TA = 0 to 70°C, VCC = 2.7~3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLE Setup Time	tCLS	0	-	-	ns
CLE Hold Time	tCLH	5	-	-	ns
$\overline{CE}$ Setup Time	tCS	20	-	-	ns
$\overline{CE}$ Hold Time	tCH	5	-	-	ns
Write Pulse Width	tWP	12	-	-	ns
ALE Setup Time	tALS	0	-	-	ns
ALE Hold Time	tALH	5	-	-	ns
Data Setup Time	tDS	12	-	-	ns
Data Hold Time	tDH	5	-	-	ns
Write Cycle Time	tWC	25	-	-	ns
$\overline{WE}$ High Hold Time	tWH	10	-	-	ns
Ready to $\overline{RE}$ Falling Edge	tRR	20	-	-	ns

Parameter	Symbol	Min.	Typ.	Max.	Unit
Read Pulse Width	tRP	12	-	-	ns
Read Cycle Time	tRC	25	-	-	ns
$\overline{RE}$ Access Time (serial data access)	tREA	-	-	20	ns
$\overline{RE}$ Access Time (ID read)	tREAID	-	-	20	ns
$\overline{RE}$ High to Output Hi-Z	tRHZ	-	-	50	ns
$\overline{RE}$ High Hold Time	tREH	10	-	-	ns
$\overline{RE}$ High to Output Hold	tRHOH	20	-	-	ns
Output Hi-Z to $\overline{RE}$ Falling Edge	tIR	0	-	-	ns
$\overline{RE}$ Access Time (status read)	tRSTO	-	-	20	ns
CLE to $\overline{RE}$ Delay	tCLR	30	-	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	tWHR	60	-	-	ns
ALE Low to $\overline{RE}$ Low (ID read)	tAR1	10	-	-	ns
$\overline{CE}$ Low to $\overline{RE}$ Low	tCR	10	-	-	ns
Memory Cell Array to Starting Address	tR	-	-	25	us
$\overline{WE}$ High to Busy	tWB	-	-	100	ns
ALE Low to $\overline{RE}$ Low (read cycle)	tAR2	10	-	-	ns
$\overline{RE}$ Last Clock Rising Edge to Busy (in sequential read)	tRB	-	-	200	ns
Device Reset Time	tRST	-	-	6	us

6. PACKAGE/PAD LOCATIONS

6.1. Ordering Information

Product Number	Package Type
GPR27P512A-NnnV-QA03x	Halogen Free Package

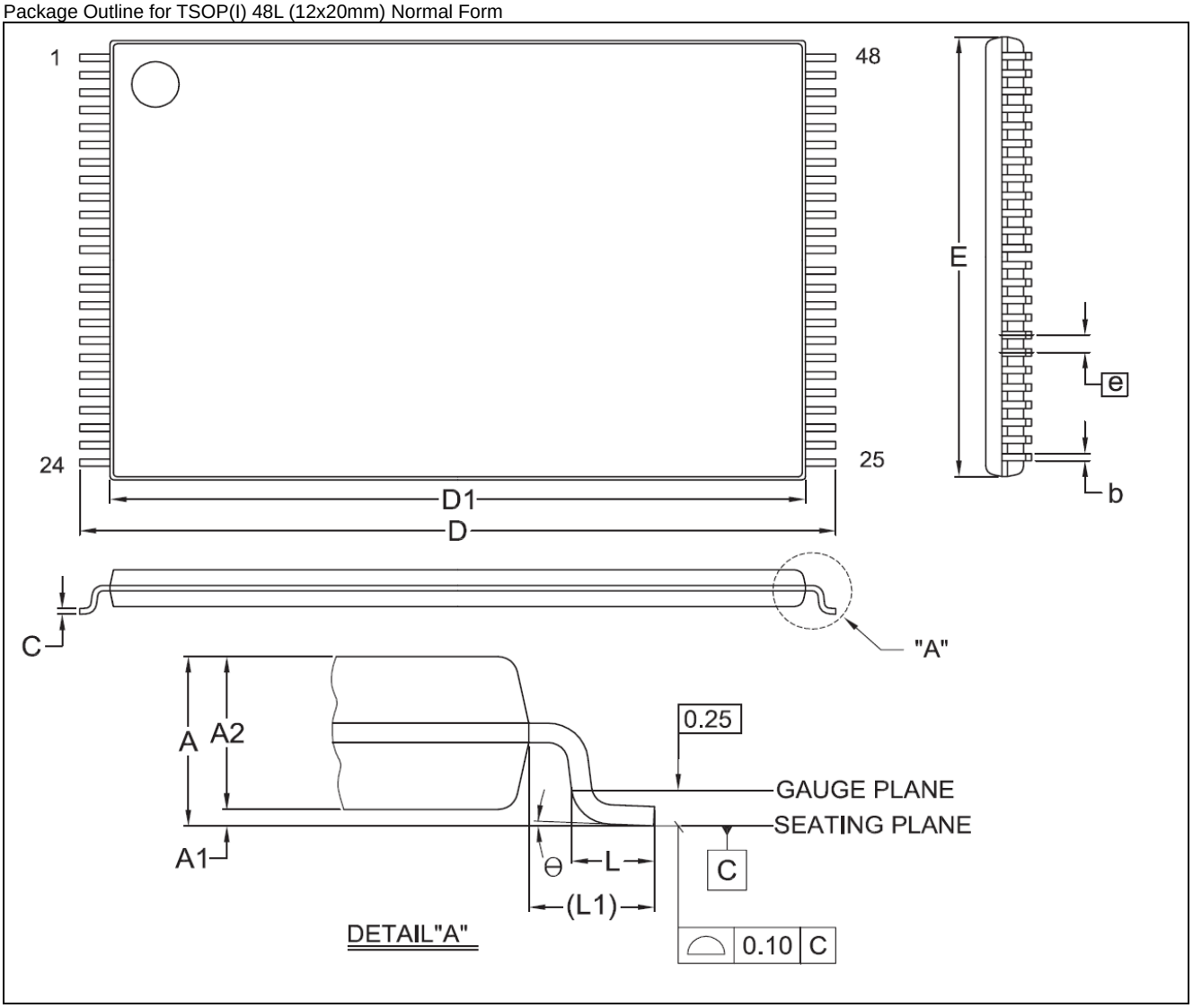
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

6.2. Package Information

Package Outline for TSOP(I) 48L (12x20mm) Normal Form



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.20	-	-	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.20	0.27	0.007	0.008	0.11
C	0.10	0.13	0.21	0.004	0.005	0.008

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
D	19.80	20.00	20.20	0.780	0.787	0.795
D1	18.30	18.40	18.50	0.720	0.724	0.728
E	11.90	12.00	12.10	0.469	0.472	0.476
e	-	0.50	-	-	0.020	-
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	0.70	0.80	0.90	0.028	0.031	0.035
θ	0°	5°	8°	0°	5°	8°

7. DISCLAIMER

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8. REVISION HISTORY

Date	Revision #	Description	Page
Nov. 21, 2011	1.5	1. Modify 4.17 ID Read. 2. Modify 5.4 AC Characteristics.	15 18
Dec. 21, 2009	1.4	Modify 4.17 ID Read.	15
Aug. 05, 2009	1.3	1. Modify 1. FEATURES. 2. Modify 5.3 DC Characteristics.	3 18
Jul. 06, 2009	1.2	Modify 4.17 ID Read.	15
Jun. 09, 2009	1.1	Modify 4.17 ID Read.	15
May 19, 2009	1.0	Original	23