FIFO_SV verification

Presented by

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GITHUB

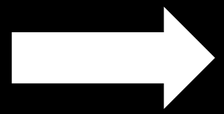
Original FIFO Design

```
8   module FIFO(data_in, wr_en, rd_en, clk, rst_n, full, empty, almostfull, almostempty, wr_ack, overflow, underflow, data_out);
9   parameter FIFO_WIDTH = 16;
10  parameter FIFO_DEPTH = 8;
11  input [FIFO_WIDTH-1:0] data_in;
12  input clk, rst_n, wr_en, rd_en;
13  output reg [FIFO_WIDTH-1:0] data_out;
14  output reg wr_ack, overflow;
15  output full, empty, almostfull, almostempty, underflow;
16
17  localparam max_fifo_addr = $clog2(FIFO_DEPTH);
18
19  reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0];
20
21  reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
22  reg [max_fifo_addr:0] count;
23
24  always @(posedge clk or negedge rst_n) begin
25      if (!rst_n) begin
26          wr_ptr <= 0;
27      end
28      else if (wr_en && count < FIFO_DEPTH) begin
29          mem[wr_ptr] <= data_in;
30          wr_ack <= 1;
31          wr_ptr <= wr_ptr + 1;
32      end
33      else begin
34          wr_ack <= 0;
35          if (full & wr_en)
36              overflow <= 1;
37          else
38              overflow <= 0;
39      end
40  end
41
42  always @(posedge clk or negedge rst_n) begin
43      if (!rst_n) begin
44          rd_ptr <= 0;
45      end
46      else if (rd_en && count != 0) begin
47          data_out <= mem[rd_ptr];
48          rd_ptr <= rd_ptr + 1;
49      end
50  end
51
52  always @(posedge clk or negedge rst_n) begin
53      if (!rst_n) begin
54          count <= 0;
55      end
56      else begin
57          if  ( ({wr_en, rd_en} == 2'b10) && !full)
58              count <= count + 1;
59          else if ( ({wr_en, rd_en} == 2'b01) && !empty)
60              count <= count - 1;
61      end
62  end
63
64  assign full = (count == FIFO_DEPTH)? 1 : 0;
65  assign empty = (count == 0)? 1 : 0;
66  assign underflow = (empty && rd_en)? 1 : 0;
67  assign almostfull = (count == FIFO_DEPTH-2)? 1 : 0;
68  assign almostempty = (count == 1)? 1 : 0;
69
70  endmodule
```

Bugs and Fixes

1-Under_Flow is a seq output

```
output reg wr_ack, overflow;
output full, empty, almostfull, almostempty, underflow;
```



```
output reg wr_ack, overflow, underflow;  //CORRECT
output full, empty, almostfull, almostempty /*underflow false*/; //UNDERFLOW IS A SEQ SO IT MUST BE REG
```

```
assign underflow = (empty && rd_en)? 1 : 0;
```

```
always @(posedge clk or negedge rst_n) begin
  if (!rst_n) begin
    rd_ptr <= 0;
    underflow <= 0;  //reseting underflow since it is a seq logic
  end else if (rd_en && !empty) begin
    data_out <= mem[rd_ptr];
    rd_ptr   <= rd_ptr + 1;
  end else if (empty && rd_en) underflow <= 1;  //ADDING UNDERFLOW LOGIC IN THE ALWAYS BLOCK
  else underflow <= 0;  //ASSERT TO 0 IF NO EMPTY AND NO read_enable
end  //ELSE IS VALID
```

2-initialization Issue

```
reg [max_fifo_addr-1:0] wr_ptr=0; //Must initialize this to zero
reg [max_fifo_addr-1:0] rd_ptr=0; //Must initialize this to zero
reg [max_fifo_addr:0] count=0;    //Must initialize this to zero
```

Bugs and Fixes

3-overflow and wr_ack must
be reseted to zero

```
if (!rst_n) begin
  wr_ptr   <= 0;
  overflow <= 0;  //since overflow is a seq so reset affects it
  wr_ack   <= 0;  //wr_ack should equal zero in reset
```

4-To make the design hit the
100% conditional coverage we
must use && instead of &

```
if (full && wr_en) overflow <= 1;  //sould be &&
```

Bugs and Fixes

5-We must add more cases
when wr_en and rd_en are asserted count must change depending is it full or empty and if !full ||!empty then count remains constant

```
end else begin
  if (({wr_en, rd_en} == 2'b10) && !full) count <= count + 1;
  else if (({wr_en, rd_en} == 2'b01) && !empty) count <= count - 1;
  else if (({wr_en, rd_en} == 2'b11) && full) count <= count - 1;  //error
  else if (({wr_en, rd_en} == 2'b11) && empty) count <= count + 1;  //error
```

6-Almostfull is when the count = FIFO_DEPTH -1

```
assign almostfull = (count == FIFO_DEPTH - 1) ? 1 : 0;  //count from 1 to 8 so almost full -1
```

FIFO DESIGN AFTER

```
module FIFO (
    data_in,
    wr_en,
    rd_en,
    clk,
    rst_n,
    full,
    empty,
    almostfull,
    almostempty,
    wr_ack,
    overflow,
    underflow,
    data_out
);
  parameter FIFO_WIDTH = 16;
  parameter FIFO_DEPTH = 8;
  input [FIFO_WIDTH-1:0] data_in;
  input clk, rst_n, wr_en, rd_en;
  output reg [FIFO_WIDTH-1:0] data_out;
  output reg wr_ack, overflow, underflow;  //CORRECT
  output full, empty, almostfull, almostempty /*underflow false*/; //UNDERFLOW IS A SEQ SO IT MUST BE REG
  localparam max_fifo_addr = $clog2(FIFO_DEPTH);
  reg [FIFO_WIDTH-1:0] mem[FIFO_DEPTH-1:0];
  reg [max_fifo_addr-1:0] wr_ptr=0; //Must initialize this to zero
  reg [max_fifo_addr-1:0] rd_ptr=0; //Must initialize this to zero
  reg [max_fifo_addr:0] count=0;    //Must initialize this to zero
```

```
  assign full = (count == FIFO_DEPTH) ? 1 : 0;
  assign empty = (count == 0) ? 1 : 0;
  assign almostfull = (count == FIFO_DEPTH - 1) ? 1 : 0;  //count from 1 to 8 so almost full -1
  assign almostempty = (count == 1) ? 1 : 0;
```

```
  always @(posedge clk or negedge rst_n) begin
    if (!rst_n) begin
      wr_ptr   <= 0;
      overflow <= 0;  //since overflow is a seq so reset affects it
      wr_ack   <= 0;  //wr_ack should equal zero in reset
    end else if (wr_en && !full) begin
      mem[wr_ptr] <= data_in;
      wr_ack <= 1;
      wr_ptr <= wr_ptr + 1;
    end else begin
      wr_ack <= 0;
      if (full && wr_en) overflow <= 1;  //sould be &&
      else overflow <= 0;
    end
  end  //WRITE LOGIC IS VALID
```

```
always @(posedge clk or negedge rst_n) begin
  if (!rst_n) begin
    rd_ptr <= 0;
    underflow <= 0;  //reseting underflow since it is a seq logic
  end else if (rd_en && !empty) begin
    data_out <= mem[rd_ptr];
    rd_ptr   <= rd_ptr + 1;
  end else if (empty && rd_en) underflow <= 1;  //ADDING UNDERFLOW LOGIC IN THE ALWAYS BLOCK
  else underflow <= 0;  //ASSERT TO 0 IF NO EMPTY AND NO read_enable
end  //ELSE IS VALID
always @(posedge clk or negedge rst_n) begin
  if (!rst_n) begin
    count <= 0;
  end else begin
    if (({wr_en, rd_en} == 2'b10) && !full) count <= count + 1;
    else if (({wr_en, rd_en} == 2'b01) && !empty) count <= count - 1;
    else if (({wr_en, rd_en} == 2'b11) && full) count <= count - 1;  //error
    else if (({wr_en, rd_en} == 2'b11) && empty) count <= count + 1;  //error
  end
end
```

VERIFICATION PLAN

LABEL	DESIGN REQUIREMENT DESCRIPTION	STIMULUS GENERATION	FUNCTIONAL COVERAGE	FUNCTIONALITY CHECK
FIFO_RST	When reset is activated all pointers must equal to the initial state	Directed at the start of the tb then reset is randomized by 5% being active	-	Checking every pointer value by assertions
FIFO_WR	Checking for writing condition if(wr_en&&!full) data should be written on FIFO and at the same time wr_ack =1	Randomized with constraints of wr_en is on 70% of time	a cross coverage is combining all possiblities of wr_en ,wr_ack and rd_en	checking the output value by using a refrence model constructed in check_result task and wr_ack is being checked by assertions
FIFO_RD	checking for read condition if(rd_en&&!empty) data should be passed to data_out	Randomized with constraints of rd_en is on 30% of time	a cross coverage is combining all possiblities of wr_en ,empty and rd_en	a refrence model is used to check the value of data_out and empty is being checked by assertions
FIFO_OVERFLOW	Checking for overflow condition when wr_en is 1 and full is 1 overflow must be asserted	randomizing till getting overflow also after the randomization it was directed to ensure wr_en is 1 for 8 cycles to check for overflow	a cross coverage is used to combining all possiblities of wr_en,overflow,rd_en	a refrence model to check data_out also overflow is checked by assertions
FIFO_UNDERFLOW	Checking for underflow condition when rd_en is 1 and empty is 1 underflow must be asserted	randomizing till getting overflow also after the randomization it was directed to ensure rd_en is 1 for 8 cycles to check for underflow	a cross coverage is used to combining all possiblities of wr_en,underflow,rd_en	a refrence model to check data_out also underflow is checked by assertions
FIFO_FULL	checking for full condition when count=8 this means it wrote 8 times equal to fifo_depth then Full is asserted	randomizing till getting FULL also after the randomization it was directed to ensure wr_en is 1 for 8 cycles	a cross coverage is used to combining all possiblities of wr_en,full,rd_en	a refrence model to check data_out also full is checked by assertions
FIFO_EMPTY	checking for empty condition when count=0 this means it wrote 0 times then empty is asserted	randomizing till getting EMPTY also after the randomization it was directed after reseting to ensure wr_en is 0 and rd_en=1 ensure no data was written	a cross coverage is used to combining all possiblities of wr_en,empty,rd_en	a refrence model to check data_out also empty is checked by assertions
FIFO_ALMOSTFULL	checking for almostfull condition when count=7 this means it wrote 7 times then almostfull is asserted	randomizing till getting ALMOSTFULL also after the randomization it was directed to ensure wr_en is 1 for 7 cycles	a cross coverage is used to combining all possiblities of wr_en,almostfull,rd_en	a refrence model to check data_out also almostfull is checked by assertions
FIFO_ALMOSTEMPTY	checking for empty condition when count=1 this means it wrote 1 times then empty is asserted	randomizing till getting ALMOSTEMPTY also after the randomization it	a cross coverage is used to combining all possiblities of wr_en,almostempty,rd_en	a refrence model to check data_out also almostempty is checked by assertions

FIFO INTERFACE AND SHARED_PKG

```
interface FIFO_IF (
    input bit clk
);
  parameter FIFO_WIDTH = 16;
  parameter FIFO_DEPTH = 8;
  bit [FIFO_WIDTH-1:0] data_in;
  logic rst_n, wr_en, rd_en;
  reg [FIFO_WIDTH-1:0] data_out;
  reg wr_ack, overflow;
  logic full, empty, almostfull, almostempty, underflow;
  modport TEST(
      output data_in, clk, rst_n, wr_en, rd_en,
      input data_out, wr_ack, overflow, full, empty, almostfull, almostempty, underflow
  );
  modport MON(
      input data_in,clk,rst_n,wr_en,rd_en,
   data_out,wr_ack,overflow,full,empty,almostfull,almostempty,underflow
  );
endinterface
```

```
package shared_pkg;
  int error_count = 0;
  int correct_count = 0;
  bit test_finished = 0;
  parameter FIFO_WIDTH = 16;
  parameter FIFO_DEPTH = 8;
endpackage

```

FIFO_TRANSACTION
TOP_MODULE AND TB

```
package trans_pkg;
  import shared_pkg::*;
  class FIFO_Transaction;
    parameter FIFO_WIDTH = 16;
    parameter FIFO_DEPTH = 8;
    rand logic [FIFO_WIDTH-1:0] data_in;
    rand logic rst_n, wr_en, rd_en;
    reg [FIFO_WIDTH-1:0] data_out;
    reg wr_ack, overflow;
    logic full, empty, almostfull, almostempty, underflow;
    int RD_EN_ON_DIST, WR_EN_ON_DIST;
    function new(input int RD_EN_ON_DIST, int WR_EN_ON_DIST);
      this.RD_EN_ON_DIST = RD_EN_ON_DIST;
      this.WR_EN_ON_DIST = WR_EN_ON_DIST;
      data_in = 0;
      rst_n = 1;
      wr_en = 0;
      rd_en = 0;
    endfunction
    constraint cons {
      rst_n dist {
        1 := 95,
        0 := 5
      };
      wr_en dist {
        1 := WR_EN_ON_DIST,
        0 := 100 - WR_EN_ON_DIST
      };
      rd_en dist {
        1 := RD_EN_ON_DIST,
        0 := 100 - RD_EN_ON_DIST
      };
    }
  endclass

endpackage
```

```
module FIFO_TOP ();
  bit clk;
  initial begin
    clk = 0;
    forever begin
      #10 clk = ~clk;
    end
  end
  FIFO_IF FIFO_IF_obj (clk);
  FIFO DUT (
      FIFO_IF_obj.data_in,
      FIFO_IF_obj.wr_en,
      FIFO_IF_obj.rd_en,
      clk,
      FIFO_IF_obj.rst_n,
      FIFO_IF_obj.full,
      FIFO_IF_obj.empty,
      FIFO_IF_obj.almostfull,
      FIFO_IF_obj.almostempty,
      FIFO_IF_obj.wr_ack,
      FIFO_IF_obj.overflow,
      FIFO_IF_obj.underflow,
      FIFO_IF_obj.data_out
  );
  FIFO_tb TEST (FIFO_IF_obj);
  FIFO_mon MON (FIFO_IF_obj);
endmodule

```

```
import shared_pkg::*;
import trans_pkg::*;
module FIFO_tb (
    FIFO_IF.TEST FIFO_tb_if
);
  initial begin
    FIFO_Transaction trans_obj;
    trans_obj = new(30, 70);
    //first reset
    @(negedge FIFO_tb_if.clk);
    FIFO_tb_if.rst_n = 0;
    @(negedge FIFO_tb_if.clk);
    //now randomize
    repeat (10000) begin
      assert (trans_obj.randomize());
      FIFO_tb_if.rst_n   = trans_obj.rst_n;
      FIFO_tb_if.wr_en   = trans_obj.wr_en;
      FIFO_tb_if.rd_en   = trans_obj.rd_en;
      FIFO_tb_if.data_in = trans_obj.data_in;
      @(negedge FIFO_tb_if.clk);
    end
    @(negedge FIFO_tb_if.clk);
    FIFO_tb_if.rst_n = 0;
    @(negedge FIFO_tb_if.clk);
    repeat (8) begin
      @(negedge FIFO_tb_if.clk);
      FIFO_tb_if.wr_en   = 1;
      FIFO_tb_if.rst_n   = 1;
      FIFO_tb_if.rd_en   = 0;
      FIFO_tb_if.data_in = trans_obj.data_in;
    end
    @(negedge FIFO_tb_if.clk);
    FIFO_tb_if.rst_n = 0;
    @(negedge FIFO_tb_if.clk);
    repeat (20) begin
      @(negedge FIFO_tb_if.clk);
      FIFO_tb_if.wr_en   = 0;
      FIFO_tb_if.rst_n   = 1;
      FIFO_tb_if.rd_en   = 1;
      FIFO_tb_if.data_in = trans_obj.data_in;
    end
    //hard coding these sequence to ensure design is working sussesfully
    #10;
    test_finished = 1;
  end
endmodule

```

FIFO COVERAGE AND MONITOR

```
package cvg_pkg;
  import trans_pkg::*;
  class FIFO_coverage;
    FIFO_Transaction F_cvg_txn = new(30, 70);
    covergroup cvr_gp;
      wr_en_cv: coverpoint F_cvg_txn.wr_en {bins wr_en_1 = {1}; bins wr_en_0 = {0};}
      rd_en_cv: coverpoint F_cvg_txn.rd_en {bins rd_en_1 = {1}; bins rd_en_0 = {0};}
      wr_ack_cv: coverpoint F_cvg_txn.wr_ack {bins wr_ack_1 = {1}; bins wr_ack_0 = {0};}
      overflow_cv: coverpoint F_cvg_txn.overflow {bins overflow_1 = {1}; bins overflow_0 = {0};}
      full_cv: coverpoint F_cvg_txn.full {bins full_1 = {1}; bins full_0 = {0};}
      empty_cv: coverpoint F_cvg_txn.empty {bins empty_1 = {1}; bins empty_0 = {0};}
      almostfull_cv: coverpoint F_cvg_txn.almostfull {
        bins almostfull_1 = {1}; bins almostfull_0 = {0};
      }
      almostempty_cv: coverpoint F_cvg_txn.almostempty {
        bins almostempty_1 = {1}; bins almostempty_0 = {0};
      }
      underflow_cv: coverpoint F_cvg_txn.underflow {bins underflow_1 = {1}; bins underflow_0 = {0};}
      wr_ack_cv_cross : cross wr_en_cv, rd_en_cv, wr_ack_cv{}
      overflow_cv_cross : cross overflow_cv, rd_en_cv, wr_en_cv{}
      full_cv_cross : cross wr_en_cv, rd_en_cv, full_cv{}
      empty_cv_cross : cross wr_en_cv, rd_en_cv, empty_cv{}
      almost_full_cv_cross : cross wr_en_cv, rd_en_cv, almostfull_cv{}
      almostempty_cv_cross : cross wr_en_cv, rd_en_cv, almostempty_cv{}
      underflow_cv_cross : cross wr_en_cv, rd_en_cv, underflow_cv{}
    endgroup : cvr_gp
    function new();
      cvr_gp = new;
    endfunction
    function void sample_data(input FIFO_Transaction F_txt);
      F_cvg_txn = F_txt;
      cvr_gp.sample;
    endfunction
  endclass

endpackage
```

```
import shared_pkg::*;
import trans_pkg::*;
import cvg_pkg::*;
import sb_pkg::*;
module FIFO_mon (
    FIFO_IF.MON MON_IF
);
  FIFO_Transaction FIFO_Transaction_obj;
  FIFO_scoreboard FIFO_scoreboard_obj;
  FIFO_coverage FIFO_coverage_obj;
  initial begin
    FIFO_scoreboard_obj = new();
    FIFO_coverage_obj = new();
    FIFO_Transaction_obj = new(30, 70);
    forever begin
      @(negedge MON_IF.clk);
      FIFO_Transaction_obj.data_in = MON_IF.data_in;
      FIFO_Transaction_obj.rst_n = MON_IF.rst_n;
      FIFO_Transaction_obj.wr_en = MON_IF.wr_en;
      FIFO_Transaction_obj.wr_ack = MON_IF.wr_ack;
      FIFO_Transaction_obj.rd_en = MON_IF.rd_en;
      FIFO_Transaction_obj.overflow = MON_IF.overflow;
      FIFO_Transaction_obj.full = MON_IF.full;
      FIFO_Transaction_obj.empty = MON_IF.empty;
      FIFO_Transaction_obj.underflow = MON_IF.underflow;
      FIFO_Transaction_obj.almostfull = MON_IF.almostfull;
      FIFO_Transaction_obj.almostempty = MON_IF.almostempty;
      FIFO_Transaction_obj.data_out    = MON_IF.data_out;
      fork  //run in //
        FIFO_scoreboard_obj.check_data(FIFO_Transaction_obj);
        FIFO_coverage_obj.sample_data(FIFO_Transaction_obj);
      join
      if (test_finished) begin
        $display("Correct_count=%d ", correct_count);
        $display("error_count=%d ", error_count);
        $stop;
      end
    end
  end
endmodule
```

FIFO_SB

```
1  package sb_pkg;
2    import trans_pkg::*;
3    import shared_pkg::*;
4    class FIFO_scoreboard;
5      parameter FIFO_WIDTH = 16;
6      parameter FIFO_DEPTH = 8;
7      reg [FIFO_WIDTH-1:0] data_out_ref;
8      reg wr_ack_ref, overflow_ref;
9      logic full_ref, empty_ref, almostfull_ref, almostempty_ref, underflow_ref;
10     reg [FIFO_WIDTH-1:0] mem_sb[FIFO_DEPTH-1:0];
11     parameter max_fifo_addr = $clog2(FIFO_DEPTH);
12     logic [max_fifo_addr-1:0] wr_pointer = 0;
13     logic [max_fifo_addr-1:0] rd_pointer = 0;
14     logic [max_fifo_addr:0] count = 0;
15     task check_data(input FIFO_Transaction trans_obj);
16       if (trans_obj.data_out === data_out_ref) begin
17         correct_count++;
18       end else begin
19         error_count++;
20         $display(
21             "=================================================ERROR DETAILS=================================
22         $display("Error at [%0t]", $time());
23         $display("rst_n       = %d", trans_obj.rst_n);
24         $display("wr_en       = %d", trans_obj.wr_en);
25         $display("rd_en       = %d", trans_obj.rd_en);
26         $display("data_in     = %4h", trans_obj.data_in);
27         $display("data_out    = %4h  refrence %4h", trans_obj.data_out, data_out_ref);
28         $display("count_sb=%d", count);
29         $display("false_count=%d", error_count);
30         $display(
31             "================================================================================================
32       end
33       reference_model(trans_obj);
34     endtask
35     task reference_model(input FIFO_Transaction trans_obj);
36       full_ref = (count == FIFO_DEPTH);
37       almostfull_ref = (count == FIFO_DEPTH - 1);
38       empty_ref = (count == 0);
39       almostempty_ref = (count == 1);
40       overflow_ref = (full_ref && trans_obj.wr_en);
41       underflow_ref = (empty_ref && trans_obj.rd_en);
42       if (~trans_obj.rst_n) begin  // write reset
43         wr_pointer = 0;
44         wr_ack_ref = 0;
45         count = 0;
46       end else if (~full_ref)
47         if (trans_obj.wr_en) begin
48           mem_sb[wr_pointer] = trans_obj.data_in;
49           wr_pointer = (wr_pointer + 1);
50           count++;
51           wr_ack_ref = 1;
52         end else wr_ack_ref = 0;
53       if (~trans_obj.rst_n) begin  // read reset
54         rd_pointer = 0;
55       end else if (~empty_ref)
56         if (trans_obj.rd_en) begin
57           data_out_ref = mem_sb[rd_pointer];
58           rd_pointer   = (rd_pointer + 1);
59           count--;
60           wr_ack_ref = 0;
61         end
62     endtask
63   endclass
```

FIFO ASSERTIONS

```
69  `ifdef SIM
70  property rst_;
71    @(posedge clk) ~rst_n |=> (~count && ~rd_ptr && ~wr_ptr);
72  endproperty
73  assert_rst:   assert property (rst_) else $error("Reset error");
74  cover_rst_:    cover property (rst_);
75
77  property wr_ack_;
78    disable iff(!rst_n)
79    @(posedge clk) (wr_en && ~full) |=> (wr_ack);
80  endproperty
81  assert_wr_ack_:  assert property (wr_ack_) else $error("wr_ack error");
82  cover_wr_ack_:   cover property (wr_ack_);
83
85  property overflow_;
86    disable iff(!rst_n)
87    @(posedge clk) (wr_en && full) |=> (overflow);
88  endproperty
89  assert_overflow_: assert property (overflow_) else $error("Overflow error");
90  cover_overflow_:  cover property (overflow_);
91
```

```
1   property underflow_;
2     disable iff(!rst_n)
3     @(posedge clk) (rd_en && empty) |=> (underflow);
4   endproperty
5   assert_underflow_: assert property (underflow_) else $error("Underflow error");
6   cover_underflow_:  cover property (underflow_);
7
8
9   property empty_;
10    disable iff(!rst_n)
11    @(posedge clk) (count == 0) |-> (empty);
12  endproperty
13  assert_empty_:  assert property (empty_) else $error("Empty error");
14  cover_empty_:   cover property (empty_);
15
16
17  property full_;
18    disable iff(!rst_n)
19    @(posedge clk) (count == FIFO_DEPTH) |-> (full);
20  endproperty
21  assert_full_:  assert property (full_) else $error("Full error");
22  cover_full_:   cover property (full_);
23
24
25  property almostfull_;
26    disable iff(!rst_n)
27    @(posedge clk) (count == FIFO_DEPTH-1) |-> (almostfull);
28  endproperty
29  assert_almostfull_:  assert property (almostfull_) else $error("Almostfull error");
30  cover_almostfull_:   cover property (almostfull_);
```

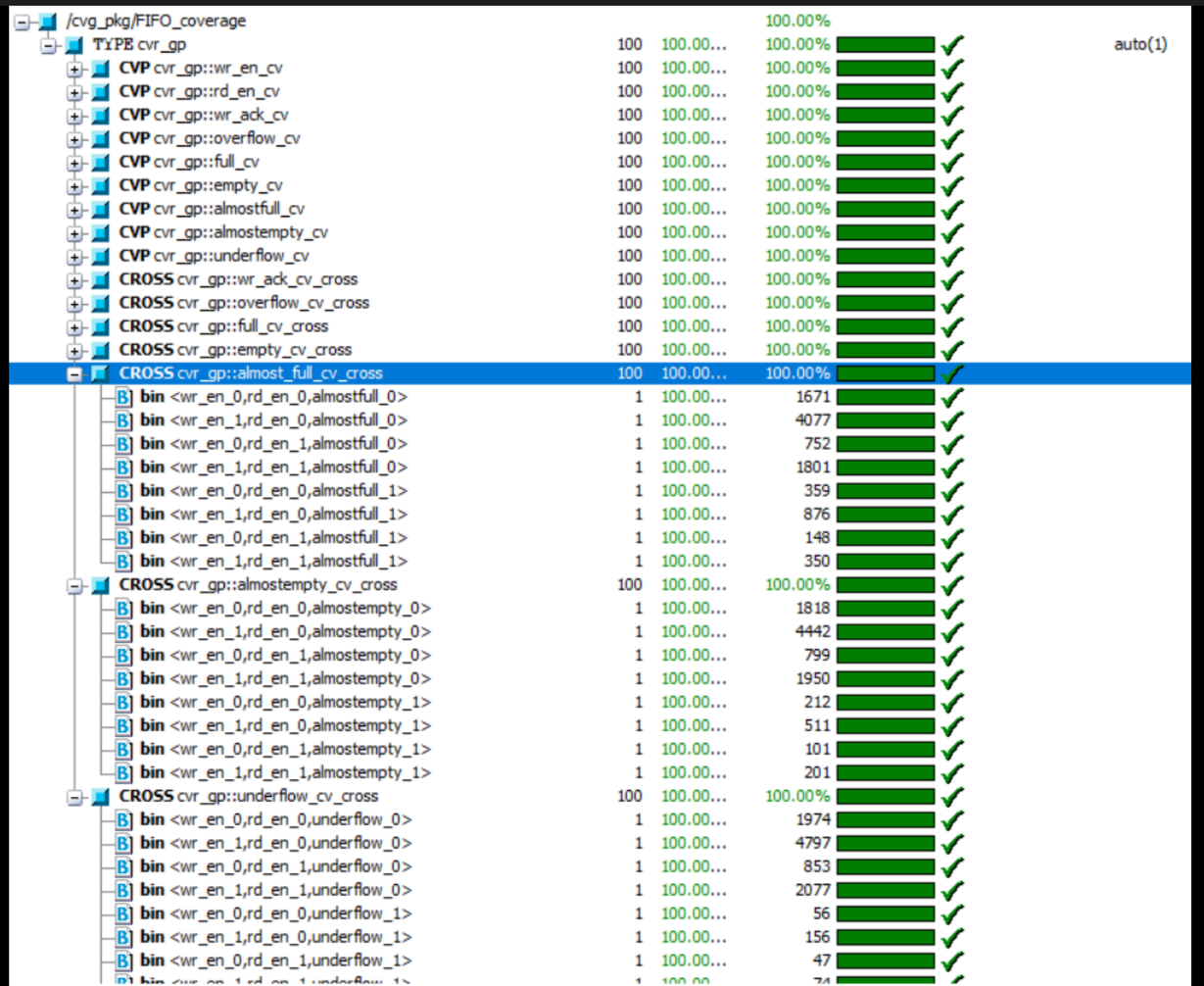
FIFO ASSERTIONS

```
125   property almostempty_;
126     disable iff(!rst_n)
127     @(posedge clk) (count == 1) |-> (almostempty);
128   endproperty
129   assert_almostempty_:  assert property (almostempty_) else $error("Almostempty error");
130   cover_almostempty_:   cover property (almostempty_);
131
132
133   property wr_pointer_0;
134     disable iff(!rst_n)
135     @(posedge clk) (wr_ptr == FIFO_DEPTH-1 && wr_en &&~full) |=> (wr_ptr == 0);
136   endproperty
137   assert_wr_pointer_0_:  assert property (wr_pointer_0) else $error("Writepointer error");
138   cover_wr_pointer_0_:   cover property (wr_pointer_0);
139
140
141   property rd_pointer_0;
142     disable iff(!rst_n)
143     @(posedge clk) (rd_ptr == FIFO_DEPTH-1 && rd_en&&~empty) |=> (rd_ptr == 0);
144   endproperty
145   assert_rd_pointer_0_:  assert property (rd_pointer_0) else $error("Readpointer error");
146   cover_rd_pointer_0_:   cover property (rd_pointer_0);
147
148
149   property wr_pointer_rst;
150     @(posedge clk) (~rst_n) |=> (wr_ptr == 0);
151   endproperty
152   assert_wr_pointer_rst_: assert property (wr_pointer_rst) else $error("Writepointer not reset");
153   cover_wr_pointer_rst_:  cover property (wr_pointer_rst);
```

```
156   property rd_pointer_rst;
157     @(posedge clk) (~rst_n) |=> (rd_ptr == 0);
158   endproperty
159   assert_rd_pointer_rst_: assert property (rd_pointer_rst) else $error("Readpointer not reset");
160   cover_rd_pointer_rst_:  cover property (rd_pointer_rst);
161
162
163   property count_rst;
164     @(posedge clk) (~rst_n) |=> (count == 0);
165   endproperty
166   assert_count_rst_: assert property (count_rst) else $error("Count not reset");
167   cover_count_rst_:  cover property (count_rst);
168
169
170   property wr_pointer_max;
171     @(posedge clk) wr_ptr < FIFO_DEPTH;
172   endproperty
173   assert_wr_pointer_max_: assert property (wr_pointer_max) else $error("Writepointer greater than depth");
174   cover_wr_pointer_max_:  cover property (wr_pointer_max);
175
176
177   property rd_pointer_max;
178     @(posedge clk) rd_ptr < FIFO_DEPTH;
179   endproperty
180   assert_rd_pointer_max_: assert property (rd_pointer_max) else $error("Readpointer greater than depth");
181   cover_rd_pointer_max_:  cover property (rd_pointer_max);
182
183
184   property count_max;
185     @(posedge clk) count <= FIFO_DEPTH;
186   endproperty
187   assert_count_max_: assert property (count_max) else $error("Count greater than depth");
188   cover_count_max_:  cover property (count_max);
189   `endif
```

DO FILE AND FUNCTIONAL COVERAGE RESULTS

```
1  vlib work
2  vlog -sv +define+SIM FIFO.sv FIFO_IF.sv FIFO_Trans.sv shared_pkg.sv FIFO_cvg.sv FIFO_sb.sv FIFO_mon.sv FIFO_tb.sv FIFO_TOP.sv +cover -covercells
3  vsim -voptargs=+acc work.FIFO_TOP -cover
4  add wave sim:/FIFO_TOP/FIFO_IF_obj/*
5  coverage save FIFO_TOP.ucdb -onexit
6  run -all
```



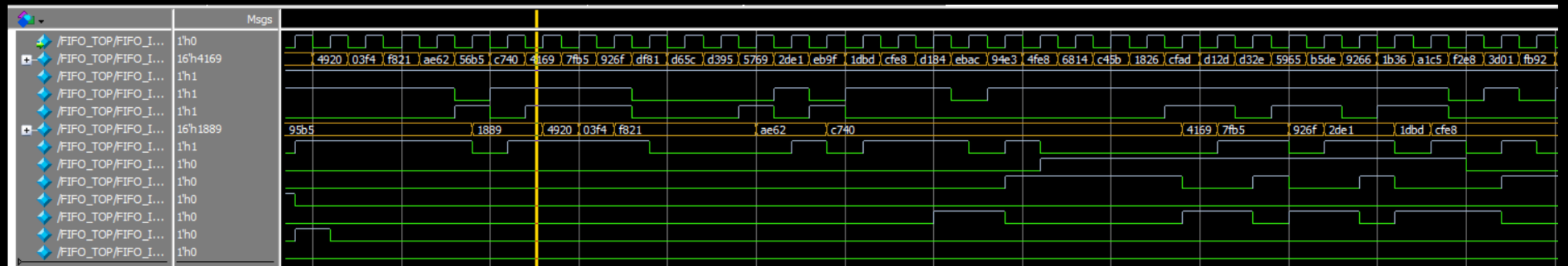
/cvg_pkg/FIFO_coverage			100.00%	
TYPE cvr_gp	100	100.00...	100.00%	auto(1)
CVP cvr_gp::wr_en_cv	100	100.00...	100.00%	
CVP cvr_gp::rd_en_cv	100	100.00...	100.00%	
CVP cvr_gp::wr_ack_cv	100	100.00...	100.00%	
CVP cvr_gp::overflow_cv	100	100.00...	100.00%	
CVP cvr_gp::full_cv	100	100.00...	100.00%	
CVP cvr_gp::empty_cv	100	100.00...	100.00%	
CVP cvr_gp::almostfull_cv	100	100.00...	100.00%	
CVP cvr_gp::almostempty_cv	100	100.00...	100.00%	
CVP cvr_gp::underflow_cv	100	100.00...	100.00%	
CROSS cvr_gp::wr_ack_cv_cross	100	100.00...	100.00%	
CROSS cvr_gp::overflow_cv_cross	100	100.00...	100.00%	
CROSS cvr_gp::full_cv_cross	100	100.00...	100.00%	
CROSS cvr_gp::empty_cv_cross	100	100.00...	100.00%	
CROSS cvr_gp::almost_full_cv_cross	100	100.00...	100.00%	
bin <wr_en_0,rd_en_0,almostfull_0>	1	100.00...	1671	
bin <wr_en_1,rd_en_0,almostfull_0>	1	100.00...	4077	
bin <wr_en_0,rd_en_1,almostfull_0>	1	100.00...	752	
bin <wr_en_1,rd_en_1,almostfull_0>	1	100.00...	1801	
bin <wr_en_0,rd_en_0,almostfull_1>	1	100.00...	359	
bin <wr_en_1,rd_en_0,almostfull_1>	1	100.00...	876	
bin <wr_en_0,rd_en_1,almostfull_1>	1	100.00...	148	
bin <wr_en_1,rd_en_1,almostfull_1>	1	100.00...	350	
CROSS cvr_gp::almostempty_cv_cross	100	100.00...	100.00%	
bin <wr_en_0,rd_en_0,almostempty_0>	1	100.00...	1818	
bin <wr_en_1,rd_en_0,almostempty_0>	1	100.00...	4442	
bin <wr_en_0,rd_en_1,almostempty_0>	1	100.00...	799	
bin <wr_en_1,rd_en_1,almostempty_0>	1	100.00...	1950	
bin <wr_en_0,rd_en_0,almostempty_1>	1	100.00...	212	
bin <wr_en_1,rd_en_0,almostempty_1>	1	100.00...	511	
bin <wr_en_0,rd_en_1,almostempty_1>	1	100.00...	101	
bin <wr_en_1,rd_en_1,almostempty_1>	1	100.00...	201	
CROSS cvr_gp::underflow_cv_cross	100	100.00...	100.00%	
bin <wr_en_0,rd_en_0,underflow_0>	1	100.00...	1974	
bin <wr_en_1,rd_en_0,underflow_0>	1	100.00...	4797	
bin <wr_en_0,rd_en_1,underflow_0>	1	100.00...	853	
bin <wr_en_1,rd_en_1,underflow_0>	1	100.00...	2077	
bin <wr_en_0,rd_en_0,underflow_1>	1	100.00...	56	
bin <wr_en_1,rd_en_0,underflow_1>	1	100.00...	156	
bin <wr_en_0,rd_en_1,underflow_1>	1	100.00...	47	

ASSERTIONS RESULTS

/FIFO_TOP/DUT/assert_rst	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge clk) (~rst_n)|=...	✓
/FIFO_TOP/DUT/assert_wr_ack_	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(disable iff (~rst_n) (@(pos...	✓
/FIFO_TOP/DUT/assert_overflow_	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(disable iff (~rst_n) (@(pos...	✓
/FIFO_TOP/DUT/assert_underflow_	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(disable iff (~rst_n) (@(pos...	✓
/FIFO_TOP/DUT/assert_empty_	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(disable iff (~rst_n) (@(pos...	✓
/FIFO_TOP/DUT/assert_full_	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(disable iff (~rst_n) (@(pos...	✓
/FIFO_TOP/DUT/assert_almostfull_	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(disable iff (~rst_n) (@(pos...	✓
/FIFO_TOP/DUT/assert_almostempty_	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(disable iff (~rst_n) (@(pos...	✓
/FIFO_TOP/DUT/assert_wr_pointer_0_	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(disable iff (~rst_n) (@(pos...	✓
/FIFO_TOP/DUT/assert_rd_pointer_0_	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(disable iff (~rst_n) (@(pos...	✓
/FIFO_TOP/DUT/assert_wr_pointer_rst_	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge clk) (~rst_n)|=...	✓
/FIFO_TOP/DUT/assert_rd_pointer_rst_	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge clk) (~rst_n)|=...	✓
/FIFO_TOP/DUT/assert_count_rst_	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge clk) (~rst_n)|=...	✓
/FIFO_TOP/DUT/assert_wr_pointer_max_	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge clk) wr_ptr<8)	✓
/FIFO_TOP/DUT/assert_rd_pointer_max_	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge clk) rd_ptr<8)	✓
/FIFO_TOP/DUT/assert_count_max_	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge clk) count<=8)	✓
/FIFO_TOP/TEST/#ublk#182146786#6/#ublk#182146786#14/immed__15	Immediate	SVA	on	0	1	-	-	-	-		off	assert (randomize(...))	✓

/FIFO_TOP/DUT/cover_rst_	SVA	✓	Off	485	1	Unli...	1	100%	✓	0	0	0 ns 0
/FIFO_TOP/DUT/cover_wr_ack_	SVA	✓	Off	4813	1	Unli...	1	100%	✓	0	0	0 ns 0
/FIFO_TOP/DUT/cover_overflow_	SVA	✓	Off	1621	1	Unli...	1	100%	✓	0	0	0 ns 0
/FIFO_TOP/DUT/cover_underflow_	SVA	✓	Off	256	1	Unli...	1	100%	✓	0	0	0 ns 0
/FIFO_TOP/DUT/cover_empty_	SVA	✓	Off	768	1	Unli...	1	100%	✓	0	0	0 ns 0
/FIFO_TOP/DUT/cover_full_	SVA	✓	Off	2372	1	Unli...	1	100%	✓	0	0	0 ns 0
/FIFO_TOP/DUT/cover_almostfull_	SVA	✓	Off	1643	1	Unli...	1	100%	✓	0	0	0 ns 0
/FIFO_TOP/DUT/cover_almostempty_	SVA	✓	Off	983	1	Unli...	1	100%	✓	0	0	0 ns 0
/FIFO_TOP/DUT/cover_wr_pointer_0_	SVA	✓	Off	417	1	Unli...	1	100%	✓	0	0	0 ns 0
/FIFO_TOP/DUT/cover_rd_pointer_0_	SVA	✓	Off	167	1	Unli...	1	100%	✓	0	0	0 ns 0
/FIFO_TOP/DUT/cover_wr_pointer_rst_	SVA	✓	Off	485	1	Unli...	1	100%	✓	0	0	0 ns 0
/FIFO_TOP/DUT/cover_rd_pointer_rst_	SVA	✓	Off	485	1	Unli...	1	100%	✓	0	0	0 ns 0
/FIFO_TOP/DUT/cover_count_rst_	SVA	✓	Off	485	1	Unli...	1	100%	✓	0	0	0 ns 0
/FIFO_TOP/DUT/cover_wr_pointer_max_	SVA	✓	Off	10035	1	Unli...	1	100%	✓	0	0	0 ns 0
/FIFO_TOP/DUT/cover_rd_pointer_max_	SVA	✓	Off	10035	1	Unli...	1	100%	✓	0	0	0 ns 0
/FIFO_TOP/DUT/cover_count_max_	SVA	✓	Off	10035	1	Unli...	1	100%	✓	0	0	0 ns 0

```
# Correct_count=       10035
# error_count=           0
# ** Note: $stop    : FIFO_mon.sv(36)
#    Time: 200700 ns  Iteration: 1  Instance: /FIFO_TOP/MON
```



COVERAGE

Toggles - by instance (/FIFO_TOP/DUT)

- sim:/FIFO_TOP/DUT
  - almostempty
  - almostfull
  - clk
  - count
  - data_in
  - data_out
  - empty
  - full
  - overflow
  - rd_en
  - rd_ptr
  - rst_n
  - underflow
  - wr_ack
  - wr_en
  - wr_ptr

Statements - by instance (/FIFO_TOP/DUT)

FIFO.sv

```
28 always @(posedge clk or negedge rst_n) begin
30 wr_ptr   <= 0;
31 overflow <= 0;  //since overflow is a seq so reset affects it
32 wr_ack   <= 0;  //wr_ack should equal zero in reset
34 mem[wr_ptr] <= data_in;
35 wr_ack <= 1;
36 wr_ptr <= wr_ptr + 1;
38 wr_ack <= 0;
39 if (full && wr_en) overflow <= 1;  //sould be &&
40 else overflow <= 0;
44 always @(posedge clk or negedge rst_n) begin
46 rd_ptr <= 0;
47 underflow <= 0;  //reseting underflow since it is a seq logic
49 data_out <= mem[rd_ptr];
50 rd_ptr   <= rd_ptr + 1;
51 end else if (empty && rd_en) underflow <= 1;  //ADDING UNDERFLOW LOGI
52 else underflow <= 0;  //ASSERT TO 0 IF NO EMPTY AND NO read_enable
54 always @(posedge clk or negedge rst_n) begin
56 count <= 0;
58 if (({wr_en, rd_en} == 2'b10) && !full) count <= count + 1;
59 else if (({wr_en, rd_en} == 2'b01) && !empty) count <= count - 1;
60 else if (({wr_en, rd_en} == 2'b11) && full) count <= count - 1;  //error
61 else if (({wr_en, rd_en} == 2'b11) && empty) count <= count + 1;  //error
65 assign full = (count == FIFO_DEPTH) ? 1 : 0;
66 assign empty = (count == 0) ? 1 : 0;
67 assign almostfull = (count == FIFO_DEPTH - 1) ? 1 : 0;  //count from 1 to 8 so almost full -1
68 assign almostempty = (count == 1) ? 1 : 0;
```

Branches - by instance (/FIFO_TOP/DUT)

FIFO.sv

```
29 if (!rst_n) begin
33 end else if (wr_en && !full) begin
37 end else begin
39 if (full && wr_en) overflow <= 1;  //sould be &&
40 else overflow <= 0;
45 if (!rst_n) begin
48 end else if (rd_en && !empty) begin
51 end else if (empty && rd_en) underflow <= 1;  //ADDING UNDERFLOW LOGIC IN THE ALWAYS BLOCK
52 else underflow <= 0;  //ASSERT TO 0 IF NO EMPTY AND NO read_enable
55 if (!rst_n) begin
57 end else begin
58 if (({wr_en, rd_en} == 2'b10) && !full) count <= count + 1;
59 else if (({wr_en, rd_en} == 2'b01) && !empty) count <= count - 1;
60 else if (({wr_en, rd_en} == 2'b11) && full) count <= count - 1;  //error
61 else if (({wr_en, rd_en} == 2'b11) && empty) count <= count + 1;  //error
65 assign full = (count == FIFO_DEPTH) ? 1 : 0;
66 assign empty = (count == 0) ? 1 : 0;
67 assign almostfull = (count == FIFO_DEPTH - 1) ? 1 : 0;  //count from 1 to 8 so almost full -1
68 assign almostempty = (count == 1) ? 1 : 0;
```

Conditions - by instance (/FIFO_TOP/DUT)

FIFO.sv

```
33 end else if (wr_en && !full) begin
39 if (full && wr_en) overflow <= 1;  //sould be &&
48 end else if (rd_en && !empty) begin
51 end else if (empty && rd_en) underflow <= 1;  //ADDING UNDERFLOW LOGIC IN THE ALWAYS BLOCK
58 if (({wr_en, rd_en} == 2'b10) && !full) count <= count + 1;
59 else if (({wr_en, rd_en} == 2'b01) && !empty) count <= count - 1;
60 else if (({wr_en, rd_en} == 2'b11) && full) count <= count - 1;  //error
61 else if (({wr_en, rd_en} == 2'b11) && empty) count <= count + 1;  //error
65 assign full = (count == FIFO_DEPTH) ? 1 : 0;
66 assign empty = (count == 0) ? 1 : 0;
67 assign almostfull = (count == FIFO_DEPTH - 1) ? 1 : 0;  //count from 1 to 8 so almost full -1
68 assign almostempty = (count == 1) ? 1 : 0;
```

COVERAGE REPORT ON GITHUB

Thank You

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