ECE 121DB Project Report

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Abstract

Using Medici and Tsuprem TCAD software, we were able to design 20 nm gate length nmos and pmos transistors that meet the 2013 ITRS requirements and a fabrication process to manufacture all the necessary doping profiles. Due to the onset of severe short channel effects, we use novel techniques such as 40nm thin body mosfet and buffering layer for low energy ion implantation in order to accomplish our designs. We characterize and evaluate the electrical performance of our device through multiple IV curve simulations and function demonstration by building a simple 1:1 inverter.

1. Introduction

1.1. Social Context of the Project

The computational needs of human society continue to grow as consumer electronics take over every aspect of our lives. In order to continue delivering electronic products that are cheaper, faster, and more efficient, the shrinking of transistors which make up these devices has become a crucial area of research. For digital electronics in particular, smaller transistors offer huge benefits such as faster speeds, lower power consumption, cheaper cost, and smaller area footprint. Thus, transistor technology must continue improving to meet growing consumer demands.

1.2. Main Technical Issues and Solutions

The main issues we faced in this project were short channel effects and controlling diffusion in high concentration doping profiles. Short channel effects such as DIBL and velocity saturation make it much more difficult to get a large difference between the on and off current of a device. Our solution against this was to use a thin body structure and two layer channel doping. Another problem on the fabrication side is that short channel devices often require higher doping concentrations than longer channel devices, which means the dopants will diffuse more easily and make controlling the profile more difficult. Our solution is multiple implants with techniques such as punching through the body and using a buffering layer to further fine tune the doping profile.

1.3. Report Outline

This paper will cover our design process for the NMOS and PMOS devices including the structural Medici design and TSUPREM fabrication process to realize the various doping profiles. We discuss the major difficulties, limits and constraints as well as how we sought to overcome them. Then, we characterize the devices through simulating and analyzing their IV characteristics and build a 1:1 inverter as demonstration of their use. In the end, we summarize what we achieved relative to the goals and what could be done in the future to further improve our designs.

2. Technical Background

2.1. Relevant Theory

The primary function of a transistor is to control the flow of current between the source and drain through a voltage on the gate which creates an inversion layer that acts as a channel for charge carriers to flow. However, as transistors are scaled down in size this function becomes degraded by short channel effects, most significant of which are drain induced barrier lowering (DIBL) and velocity saturation.

Drain induced barrier lowering is the phenomenon where the drain voltage is able to significantly influence the operation of the transistor. In a short channel device, the source and drain are much closer together, meaning that a high voltage on the drain could create a partial inversion layer and significantly lower the threshold voltage. This is undesirable because the conduction of current no longer only depends on the gate, making the device worse at switching and often causing a lot of unwanted leakage current.

Velocity saturation is the phenomenon where charge carriers have a maximum velocity that they cannot surpass due to frequent collisions with other charges within the

material, even if the electric field is increased even further. This is an issue for short channels because the voltage is applied within a very short length, creating very high electric fields and causing velocity saturation. Once velocity saturation occurs, the current will no longer increase even when additional voltage is applied, and the only way to increase the current further would be to increase the number of charge carriers. Thus, velocity saturation limits the drive current that the transistor can support, which is a key factor for switching speed.

A modern transistor is made up of a silicon substrate doped with various impurities that give the device certain electrical properties. Just like particles in the air, dopants within silicon undergo diffusion which strongly depend on both temperature and the concentration gradient. In a scenario where there is a sharp concentration gradient, diffusion occurs more easily, which makes it harder to control where the dopants end up. This is a problem when designing fabrication processes for devices with sharp concentration gradients.

All of these problems are encountered within our design of the short channel transistor, and understanding the physics behind why they occur is the first step to overcoming them.

2.2. Current Technical State

The first commercially successful transistors were planar FETs, where the source and drain are embedded into the surface of a flat wafer and the gate spans the space between them. This is the geometry that we will be using for our design. While these planar FETs are easy to manufacture, they suffer a lot from short channel effects because the gate only has control of the channel from one side. As transistors scale down even further, foundries have moved away from traditional planar FETs to newer geometries such as the FINFET.

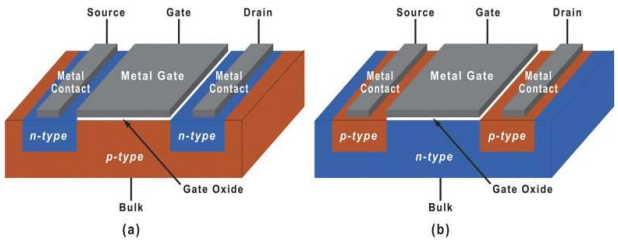

Figure 1. Planar NMOS and PMOS FETs [4]

Unlike the planar FET which is mostly a 2D structure, the FINFET has a source, drain, and channel that rises up from the substrate and a gate that surrounds the channel from 3 sides. This gives the gate much stronger control over current conduction in the channel and significantly reduces short channel effects. Although this geometry is much more difficult to manufacture, its superior electrical properties has made it the standard for modern day transistors.

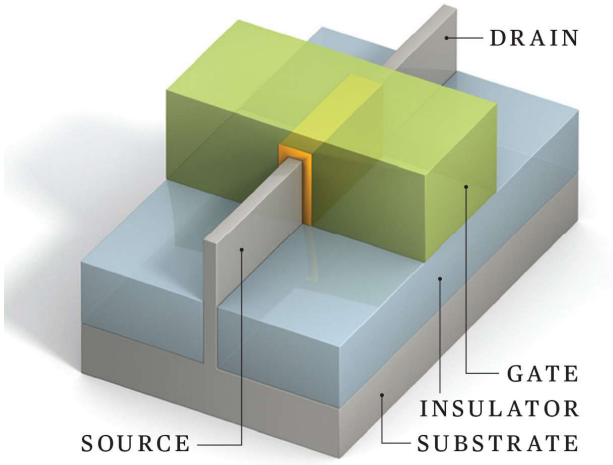

Figure 2. FINFET Image Structure [5]

However, even the FINFET is starting to reach its limit as transistors scale down to single digit nanometer scales. More advanced geometries such as gate all around (GAAFET) and multi bridge channel (MBCFET) where the gate encompasses the channel on four sides have been proposed as possible successors of the FINFET. Foundries continuously work with researchers to explore new solutions to these problems.

2.3. Standards Employed

Technical standards are crucial in the design of new products since they provide a common framework for interoperability and reliability. The standards are also essential for ensuring that our innovations meet industry expectations and can be effectively implemented. For this project, the International Technology Roadmap for Semiconductors (ITRS) serves as a foundational reference point. The ITRS is a set of documents coordinated by various experts throughout the semiconductor industry as a guideline for semiconductor technological development. Designing according to ITRS guidelines ensures alignment with industry standards and streamline integration with manufacturing processes.

3. Design Description

The main difficulty in meeting the ITRS standards for Medici design specification is the large difference between on and off current. With only 0.86 volts of headroom, it is difficult to get the required 4 orders of magnitude

difference, especially with short channel effects such as velocity saturation and DIBL setting in.

The main difficulty in TSUPREM fabrication specification is coming up with a realistic process to fabricate our theoretical device. High doping concentrations mean diffusion will be hard to control and the concentration difference in certain places are less than the recommended 1 order of magnitude, making the device very sensitive to process.

Overcoming these difficulties require more than just fine tuning parameters but novel design approaches that can offer significantly improved performance and characteristics. Thus, this section will highlight the key design choices made to achieve the performance targets.

3.1. Medici Design Approach

Our first key design choice was to use Hafnium Dioxide(HfO_2) instead of Silicon Dioxide(SiO_2) for the gate oxide. An EOT of 0.8nm is basically impossible to achieve in process and quantum tunneling effects start coming into play at around 2~3nm. By using Hafnium Dioxide with a much larger dielectric constant (25 vs 3.9), we can boost the gate oxide thickness up to 5 nm while maintaining the same electric field strength and eliminating leakage current due to quantum tunneling effects. Hafnium Dioxide must be grown through atomic layer deposition, meaning that the process will be more involved but also more precise.

Our second key design choice was to use the concept of thin body structure, motivated by this paper discussing methods to counteract short channel effects [1]. A thin body mosfet is one where the substrate body is extremely thin, usually only the thickness of the source and drain. For our design we used a body thickness of 40 nm. This structure eliminates a lot of body area where leakage current could travel and grants the gate much stronger control since the influence of the gate electric field can effectively reach the entire body of the device. This design makes the mosfet behave much more like a long channel device and allows us to go from 1 order magnitude to over 3 order magnitude difference between on and off currents. Thin body wafers are very difficult to fabricate in reality, but we couldn't meet the design requirements with only traditional techniques.

Although the thin body structure offers a lot of benefits, it limits the drive current by limiting the size of the source and drain. Because this is a short channel device, velocity saturation limits the rate of current gain we are able to achieve, meaning that the primary method to further increase drive current would be to increase the number of carriers available, which is done by increasing the depth of the source and drain. However, this leads to a tradeoff since deeper source/drain will also lead to greater leakage current. Thus, we need to reinforce the channel against leakage while maintaining high drive current to meet our design targets.

Our third key design choice to counteract leakage current is a two layer doping for the channel. There is a deep doping layer that started out as halo implants to reinforce the center body against leakage, but we realized that having it span the entire channel worked the best. After putting in the deep reinforcement, we realized through simulations that most of the leakage now traveled under the gate due to DIBL. Thus, we added a shallow layer just under the gate and tuned the doping ratio between the two layers to achieve the best results. We ended up with a shallow to deep doping ratio of 1.55~1.6, meaning that we actually doped the shallow layer more heavily than the deep layer. We hypothesize that due to DIBL, it is acceptable to have heavier channel doping because when the drain is high it helps form the gate form the inversion layer as well, meaning that drive current isn't too heavily impacted. The two layer channel doping for nmos is shown below:

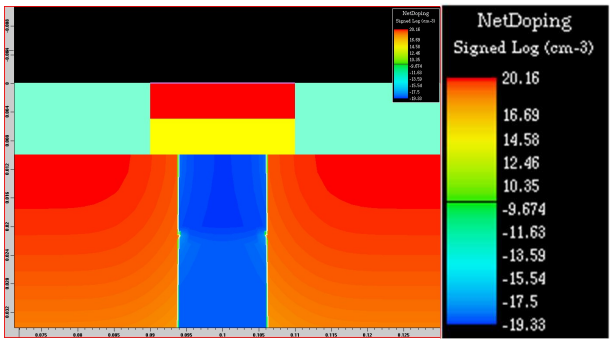

Figure 2. Channel Doping Profile for NMOS

After the nmos structure was defined, we simply utilized the same structure and tuned the doping concentrations for the pmos. Due to the lower mobility of holes, we expect both leakage current and drive current to be lower for the pmos, so we used lower doping concentrations overall. This also means that it's not really possible to get a pmos device with similar performance as nmos. Thus, we made a purposeful design choice to have the pmos current targets hit around ½ those of the nmos. In digital circuit design, there is a beta value defined as the ratio of nmos : pmos width for the two devices to have the same "drive strength", which can be approximated in our case by the drive current. Modern processes have a beta value around 2 and all CMOS circuits are designed with this limitation in mind, so we believe that it is better to tune the pmos for better processing reliability instead of better performance past half current nmos.

3.2. Medici Constraints and Limitations

As mentioned above, getting a 40 nm thin silicon body requires processes more complicated than traditional wafers. An example process for manufacturing 40nm thin silicon is demonstrated in this IEEE paper [3], where they started by depositing a 100 nm thick silicon film and then used thermal oxidation to gradually convert parts of the wafer to oxide until reaching the desired silicon depth. The oxide left on the backside can be used as an insulator and structural support. Thus, the 40nm thin silicon body is feasible but fairly involved.

Another difficulty is the extremely high doping concentrations required in such a small area. Our initial design that met the requirement actually went over the solid solubility limit of the dopants in silicon, so we had to lower the concentrations and retune the ratios to get another working design, trading a bit of performance for much better fabrication ability.

Peak Doping Concentration			
NMOS		PMOS	
Arsenic Used	1e20	Boron Used	7e19
Arsenic SSL @ 900C	3e20	Boron SSL @ 900C	1e20
Boron Used	2.33e19	Phosphorus Used	2.35e19
Boron SSL @ 900C	1e20	Phosphorus SSL @ 900C	3e20

Figure 3. Peak Doping Concentrations vs SSL @ 900C

According to this graph [2], all peak concentrations used are within the electrically active solid solubility limit in silicon at 900 degrees celsius, which is a fairly reasonable processing temperature.

In anticipation that we will also need to create a process to implement our design, we used a common background doping of 1e16 boron for both pmos and nmos so that both devices can be manufactured on the same wafer if needed. This proved to be useful for our inverter simulation later since we simply had to join the two devices together.

3.3. Medici Design Cross Section

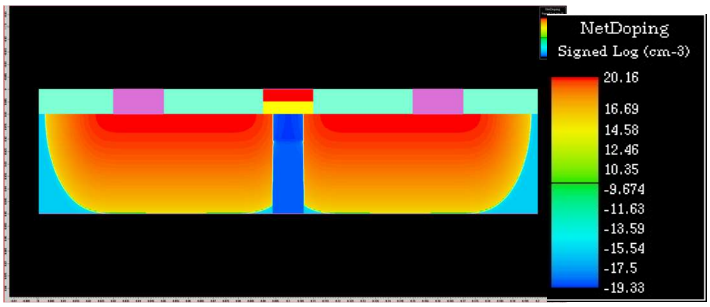

Figure 4. NMOS Cross-Section Profile

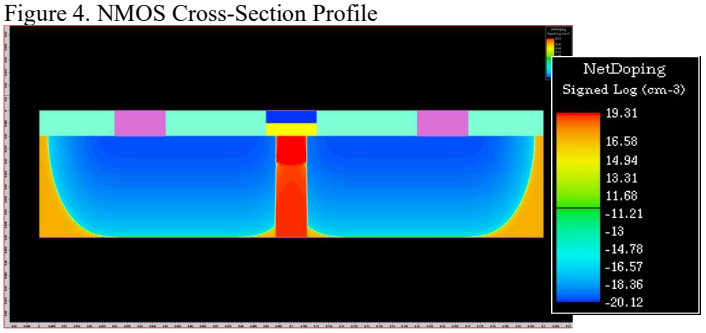

Figure 5. PMOS Cross-Section Profile

-Physical Parameters-
Gate length: 20nm
Gate thickness: 5nm
Source/Drain length: 70nm
Channel length: 12nm
Body thickness: 40nm

3.4. TSUPREM Design Approach

The goal for our process is to integrate both nmos and pmos on the same wafer. Thus, we start with a thin body wafer with background doping of 1e16 boron and then proceed with n-well, channel doping, and finish with source/drain doping.

To achieve the two-layer reinforced channel, our first key design choice was to use two implant schedules at two different energies for each channel. The first implant is performed at higher energy that mostly punches through the wafer, leaving behind an inverted doping profile that is more concentrated at the bottom. Then, a second implant is performed at lower energy that will concentrate more at the surface. The peak of the second implant will act as the shallow doping layer we had in medici, and the tail of the second implant will combine with the tail of the first implant to form the deep doping layer in the bulk substrate.

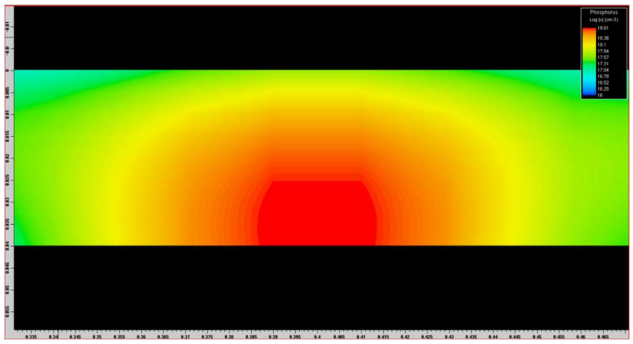

Figure 6. PMOS Channel after First Implant (Deep)

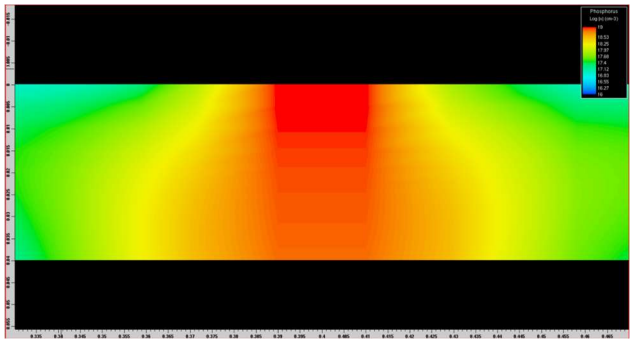

Figure 7. PMOS Channel after Second Implant (Shallow)

Although this plan sounds good in theory, we quickly realized that our wafer is simply too thin, meaning that even with the lowest energy implant the peak concentration for the second implant ends up at least halfway deep into the substrate instead of at the surface where it is desired. Thus, our second key design choice was to deposit a blocking/buffering layer on the wafer before performing the second implant to limit the range that the dopants travel, allowing us to create an implant that concentrates at the very surface of the wafer after the blocking/buffering layer is removed.

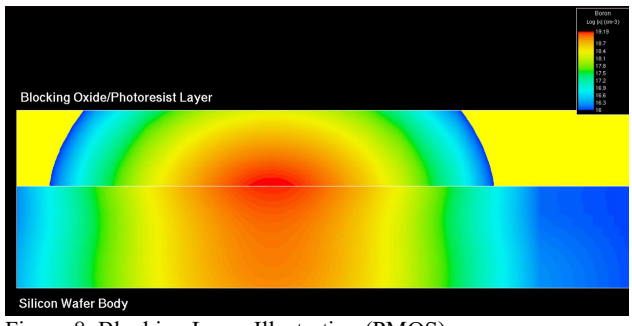

Figure 8. Blocking Layer Illustration (PMOS)

With the reinforced channel in place, we just did a simple single implantation for the source/drain. During this process, the exact dosage for the channel doping also had to be adjusted for diffusion from the source/drain implants, with the pmos requiring more higher channel doping because of greater diffusion from boron.

We did not include gate, poly, or metal contact steps because all of them are pure deposition steps that can be done more easily without needing high temperature. As mentioned previously, HfO2 must be deposited and cannot be grown from the substrate.

3.5. Tsuprem Constraints and Limitations

It is possible to create a more smoothly doped and possibly more resilient channel with 3 or more implant schedules, but we decided that 2 was good enough for this particular design since it is meant as a proof of concept. Using 2 implants, we were able to get the top half doping profile very similar to our medici profile, which is the crucial part for drive current performance. For the pmos in particular there is a second concentration peak at the bottom of the channel which isn't present in our medici design, but realistically what this will do is reduce body leakage current which is a good thing anyways. Because the pmos channel ended up a lot thinner due to boron diffusion than the nmos channel, it will experience more body leakage so the two effects may partially cancel out.

We originally wanted to use photoresist for the blocking layer like is done in reality, but testing shows that tsuprem considers photoresist completely opaque to ion implantation no matter how thin the layer is. Thus, in our design we used deposited oxide instead, but the principle of operation is the same and can be switched out in a realistic process.

The sensitivity to doping for our process will likely be poor due to the device design itself and not necessarily because of poor process design.

Dopant activation may be a problem for our process since the extremely high concentrations mean any time under high temperature will significantly alter the doping profile. In our tsuprem design we did not explicitly specify any annealing schedules, but it seems that tsuprem will specify one automatically if one is not specified. In our simulation it claims that over 50% of the dopants are indeed activated, but we are unsure about the default annealing condition and cannot comment more about it.

We believe the biggest flaw with our design is the mask alignment. We specified two completely separate masks for the channel and source/drain doping. In a classical process, the channel mask could also be used to grow the gate oxide which can then be used as a mask for the source/drain implant, meaning that everything is self-aligned. However, this cannot work in our process because our gate oxide must be deposited. Aligning the two masks precisely on the scale of nanometers is extremely difficult and cannot be done consistently. We do not have a good solution in mind for this problem.

3.6. Tsuprem Design Cross Section

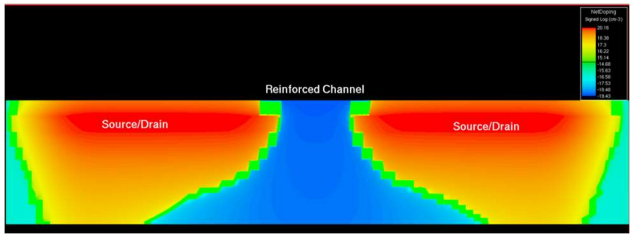

Figure 9. NMOS Doping Profile

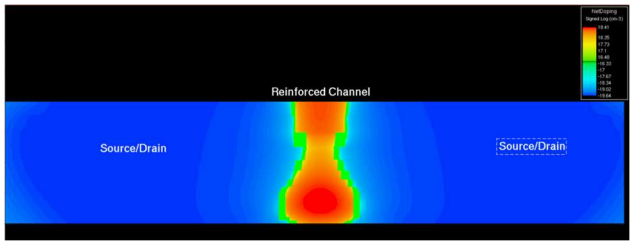

Figure 10. PMOS Doping Profile

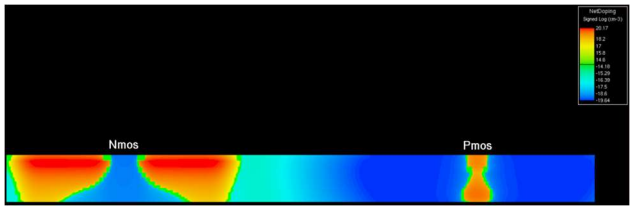

Figure 11. Combined NMOS/PMOS Doping Profiles

Source/Drain Doping			
NMOS Doping		PMOS Doping	
Target	Achieved	Target	Achieved
1e20	1e20	7e20	4e20

Figure 12. Doping Profile Values

-Nmos-
Deep channel doping: Boron 1e14 12keV
Shallow channel doping: Boron 2e14 10keV
Blocking oxide thickness: 30 nm
Source/drain: Arsenic 3e14 10keV

-Pmos-
Deep channel doping: Phosphorus 3e14 16keV
Shallow channel doping: Phosphorus 1.7e14 11keV
Blocking oxide thickness: 13 nm
Source/drain: Boron 1e15 10keV

Source/Drain implant edge has a 10nm gap to the gate/channel to help control diffusion effects.

3.7. Inverter Design

For the inverter, we simply put the medici designs for pmos and nmos together onto one substrate and connected the terminals in an inverter fashion. One thing to note is that as mentioned before, in classic CMOS design the pmos is always a factor of beta wider than the nmos to compensate for the inferior pmos current drive. Because the TCAD tools we use are two dimensional and cannot simulate width, our CMOS inverter will have a beta value of 1, meaning that the nmos will be twice as strong as the pmos. Thus, we predict that the inverter will have a voltage transfer curve heavily shifted to the left, since the pulldown path is a lot stronger than the pullup.

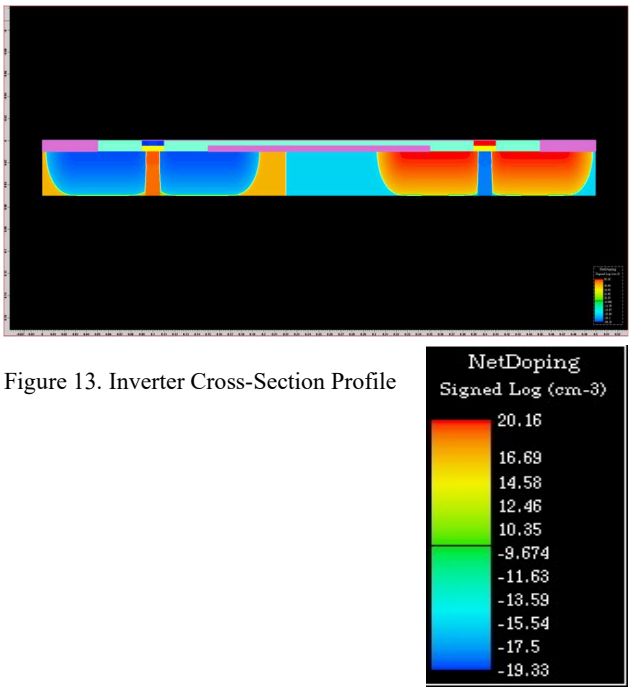

Figure 13. Inverter Cross-Section Profile

4. Testing and Validation

4.1. Experimental Procedures and Justification

To verify the electrical characteristics of our transistor designs, we ran 6 IV curves for the nmos and pmos each. Two curves are Id-Vg curves at high and low Vd to show device response to changes in gate voltage. Four curves are Id-Vd curves to demonstrate device response to changes in drain voltage. From these curves, we extracted drive current, off current, saturation threshold voltage, and subthreshold swing values to further characterize device performance.

4.2. Transistor Id-Vg Curve Results

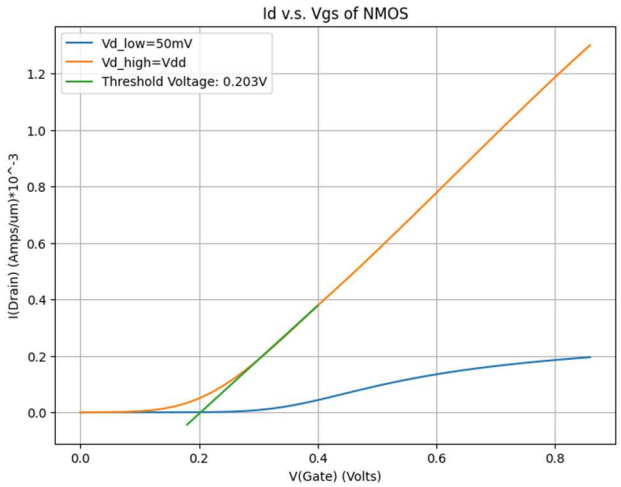

Figure 14. Threshold Voltage of NMOS

$$I_{sat,NMOS} = 1301.4\ \mu A/\mu m$$
$$I_{off,NMOS} = 98.97\ nA/\mu m$$

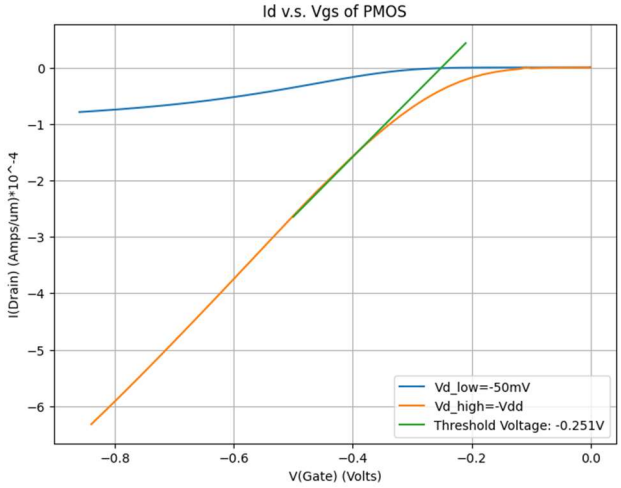

Figure 15. Threshold Voltage of PMOS

$$I_{sat,PMOS} = -652.2\ \mu A/\mu m$$
$$I_{off,PMOS} = -42.96\ nA/\mu m$$

4.3. Transistor Id-Vg Analysis & Discussion

For the high Vd Id-Vg curve, we immediately observe that the slope is fully linear almost immediately after turning on. This indicates that velocity saturation occurs either at or below threshold. Doing a simple sanity check, with 0.86 volts applied across drain and source over a distance of 20 nm the electric field is on the order of 40 kV/cm. This lines up with the typical values cited between 10k and 100kV/cm for silicon. Thus, for high values of Vd the device saturates immediately after turning on, which is a major factor in limiting the drive current since current increases linearly instead of quadratically with gate voltage.

For the low Vd Id-Vg curve, the current seems to taper off after turning on, increasing at a rate even lower than linear. Additionally, it seems that the threshold voltage is a lot higher, ~0.3V for nmos and ~-0.35V for pmos, corresponding to a 0.1V decrease from low Vd to high Vd condition. This is clear evidence for the DIBL effect happening in our transistor.

4.4. Transistor Id-Vd Curve Results

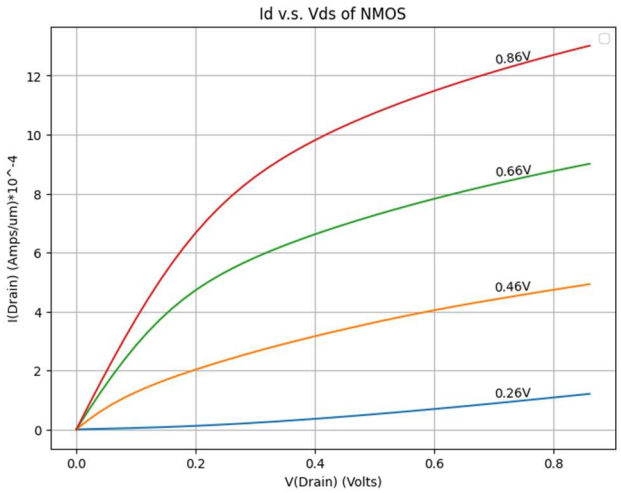

Figure 16. I/V Curves for Different Gate Voltages of NMOS

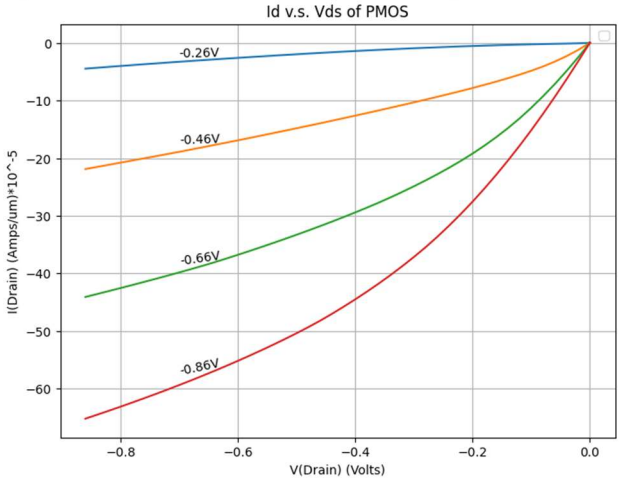

Figure 17. I/V Curves for Different Gate Voltages of PMOS

4.5. Transistor Id-Vd Analysis & Discussion

For an ideal long channel transistor the Id-Vd curves should be approximately flat after turning on, but the curves for our devices have a fairly steep curve that clearly demonstrates the channel pinch off effect. Channel pinch off happens when high Vd causes the inversion layer to disappear at the drain end which “shortens” the channel

and slightly decreases the channel resistance, leading to an increase in current. This is another effect that becomes more pronounced for short channels since the pinched off region could occupy a significant portion of the gate length, so seeing it happen to our device is not a surprise.

4.6. Transistor Subthreshold Slope Results

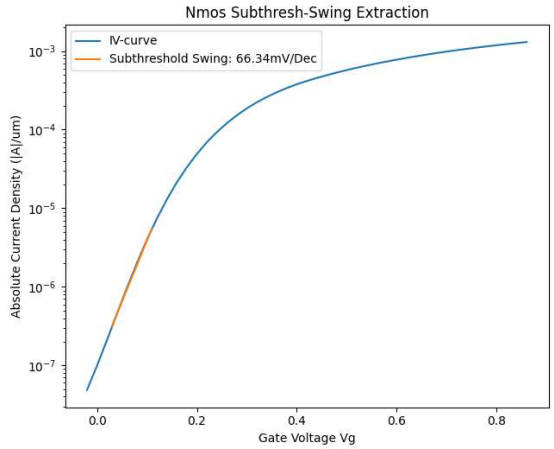

Figure 18. Subthreshold Swing of NMOS

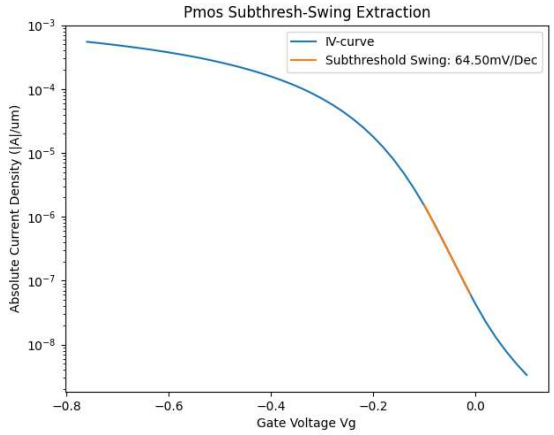

Figure 19. Subthreshold Swing of PMOS

4.7. Transistor Subthreshold Slope Discussion

Our subthreshold slope measurements came out far better than expected, achieving around 65mV/decade at room temperature for both pmos and nmos. Given that the theoretical ideal value is around 60mV, it is extremely surprising to get such a steep subthreshold slope, especially for a short channel device like ours where all kinds of short channel effects cause leakage currents that degrade the subthreshold slope. We believe it is our choice of thin body structure and reinforced channel doping that helped us achieve this feat. The suppression of leakage current through a steep subthreshold slope is likely one of the key reasons why our design was able to succeed, since it helps us achieve a higher difference between on and off current which is a crucial parameter for transistors.

4.8. ITRS Target (2013) v.s. Achieved Values

	NMOS			PMOS		
	Target	Achieved	% Diff	Target	Achieved	% Diff
L_g(nm)	20	20	-	20	20	-
V_{dd}(V)	0.86	0.86	-	-0.86	-0.86	-
EOT(nm)	0.8	0.8	-	0.8	0.8	-
I_{off}(nA/μm)	100	99	-1.0%	50	43	-14%
$I_{d,sat}$(μA/μm)	1,348	1,301	-3.5%	674	652	-3.3%
$V_{t,sat}$(mV)	200	203	+1.5%	-200	-251	+25%

Figure 20. MOSFET Target vs Achieved Values

4.9. Model Inverter Voltage Transfer Curves

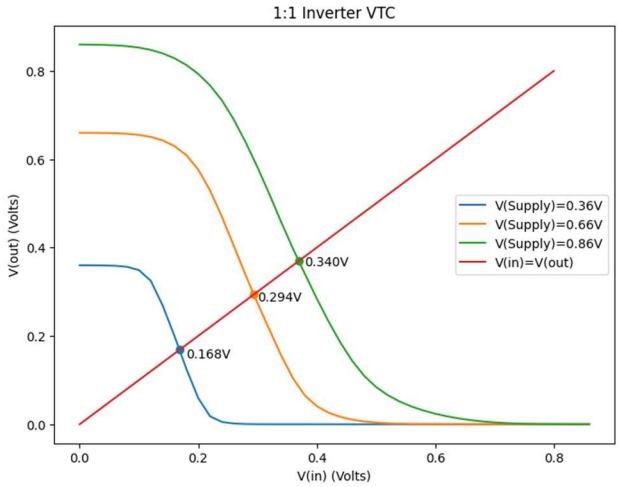

Figure 21. Inverter VTCs

4.10. Inverter Characteristic Analysis

As expected, the VTC for our 1:1 inverter is heavily shifted to the right due to the stronger nmos. The switching threshold at a supply of 0.86V is only 0.34V as opposed to the ideal value of 0.43V. However, it seems to perform fairly well otherwise with a decently steep transition slope and good noise margins across wide supply voltage ranges.

It's not really possible for the supply to go much lower than 0.3V otherwise the pmos won't even turn on.

Using the piecewise linear approximation, at a supply of 0.86V, VIL~0.2V and VIH~0.5V, giving us noise margins of ~0.2V and ~0.36V for low and high inputs respectively. This demonstration is good evidence that the devices we designed have good characteristics and can function as the building blocks of actual digital circuits.

An interesting pattern we observe is that as the supply voltage drops, the amount of left shift in the VTC actually decreases. While the switching threshold is 21% below ideal at a supply voltage of Vdd, this gap drops to 11% at 0.66V and only 6.7% at 0.36V. The transition also seems to get steeper with decreasing supply voltage, which possibly indicates that the drive strength of the two transistors get closer as supply voltage drops. We do not have a good theoretical explanation for this phenomenon but it is certainly worth investigating in the future.

5. Conclusion

In conclusion, we were able to come up with transistor designs that generally satisfy the 2013-2014 ITRS requirements. All physical dimensions were satisfied perfectly and we achieved off current completely within specification while being less than 3.5% short of drive current targets. Our pmos saturation threshold voltage is a little higher than specification, but this may not be a bad tradeoff for the much lower off state current. Especially considering that we are designing planar FETs at a dimension where foundries have already begun moving to FINFETs, our design has been mostly a success.

The large difference between on and off currents was definitely the largest hurdle for our design, and most of our design process was focused on increasing this difference. We were able to find a couple innovative design approaches in device geometry and doping profile to vastly improve on short channel effects and get to the finish line through fine tuning the dimensions and concentrations with the help of simulation.

The main thing that wasn't successful about our design was the fabrication process for the pmos. Due to the boron's high rate of diffusion, we were not able to achieve the desired source/drain concentrations without completely killing the channel in the process. The highest source/drain concentration we could achieve was around 57% of the desired concentration, which may cut the drive current by over ⅓ based on our medici design experience.

In comparison, the nmos actually came out surprisingly well, with the top half of the channel almost identical to our medici design and the bottom fan out is an interesting profile that may actually be a good thing since it further limits body leakage without heavily affecting drive current.

5.1. Future Directions / Possible Improvements

Main improvements for our design would definitely revolve around better fabrication and manufacturability. A good design for widespread adoption cannot only have good characteristics but also can't be almost impossible to manufacture. Our focus would be around finding ways to decrease the doping concentrations through more creative doping profiles and geometries. Some processing techniques that could be explored for this goal are implantation at an angle and silicon deposition.

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