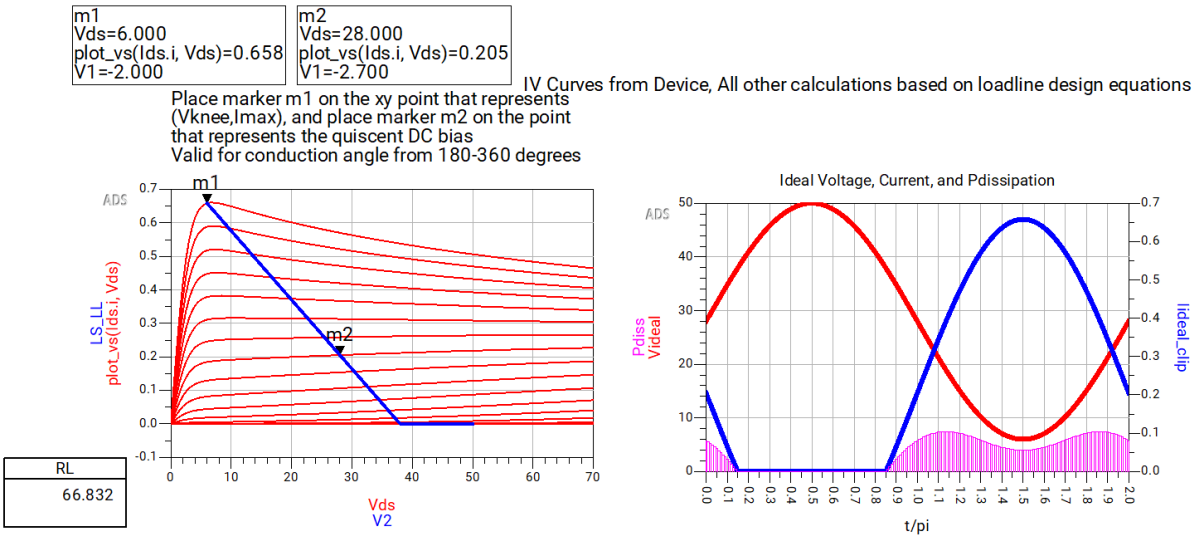
279A Power Amplifier Design Project

Justin Hu, Jun Sang Lee

Since neither of us have much background with power amplifiers, this youtube series by Anurag Bhargava has been immensely helpful in understanding the key concepts and tradeoffs in power amplifier design.
https://www.youtube.com/watch?v=-GLPH9BYvSo&t=2656s
Our goal is mainly to get a better understanding of the design process, so we did not set particular performance goals for this project. We optimized our matching networks for a narrower bandwidth of 200Mhz (100Mhz each side).

Referring to the specs for the CGH40010 transistor, we set the gate quiescent voltage at the recommended -2.7V. Through simulation with the help of Keysight's PA design workspace (https://www.youtube.com/watch?v=WAingaHfBMs), this corresponds to a conduction angle of 256 degrees, forming a class AB amplifier.



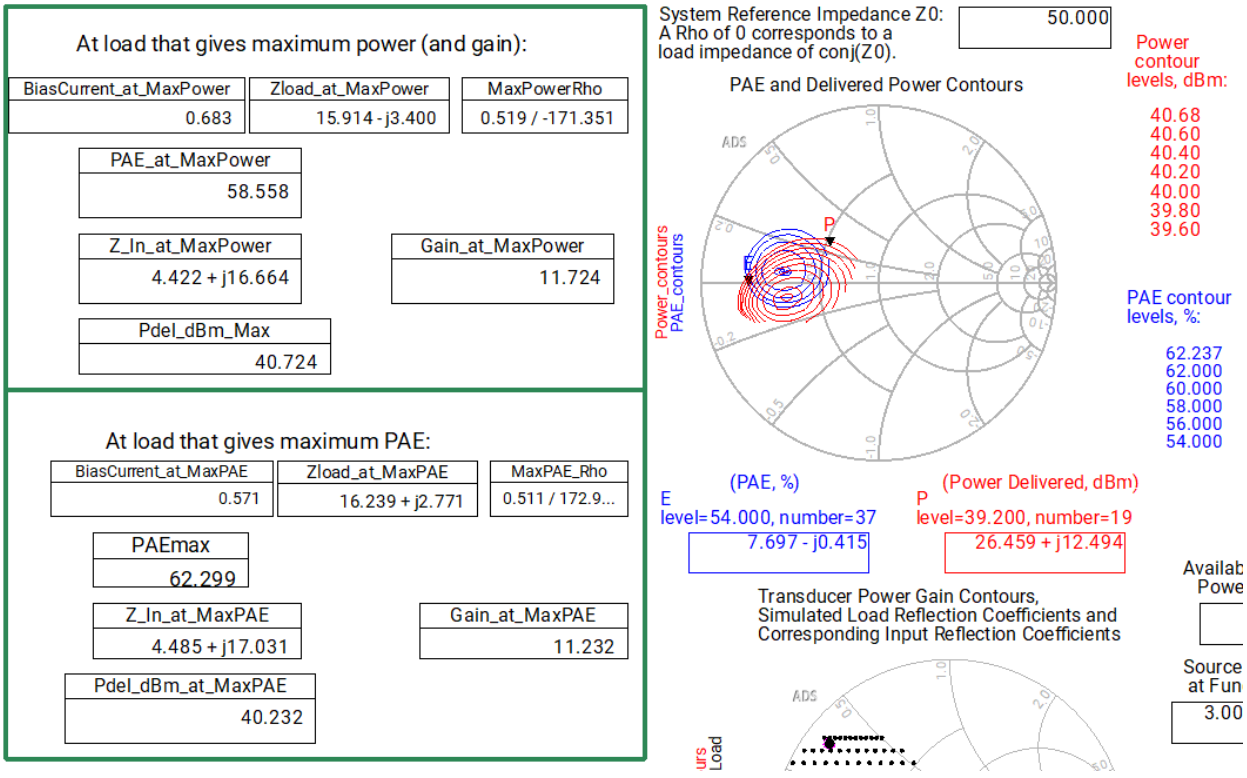
Pout_Max	SS_Gain	LS_Gain	n_max	Idc	Conduction_Angle	Duty_Cycle
35.59	15.20	12.28 / -0.00	46.09	0.28	256.00	71.11

Eqn Zin=50

To get a starting point for ideal matching conditions, we perform a one tone load pull simulation at the fundamental frequency of 3.8Ghz. Referencing the datasheet, we set initial load and source impedances by referencing data sheet values at 3.5Ghz.

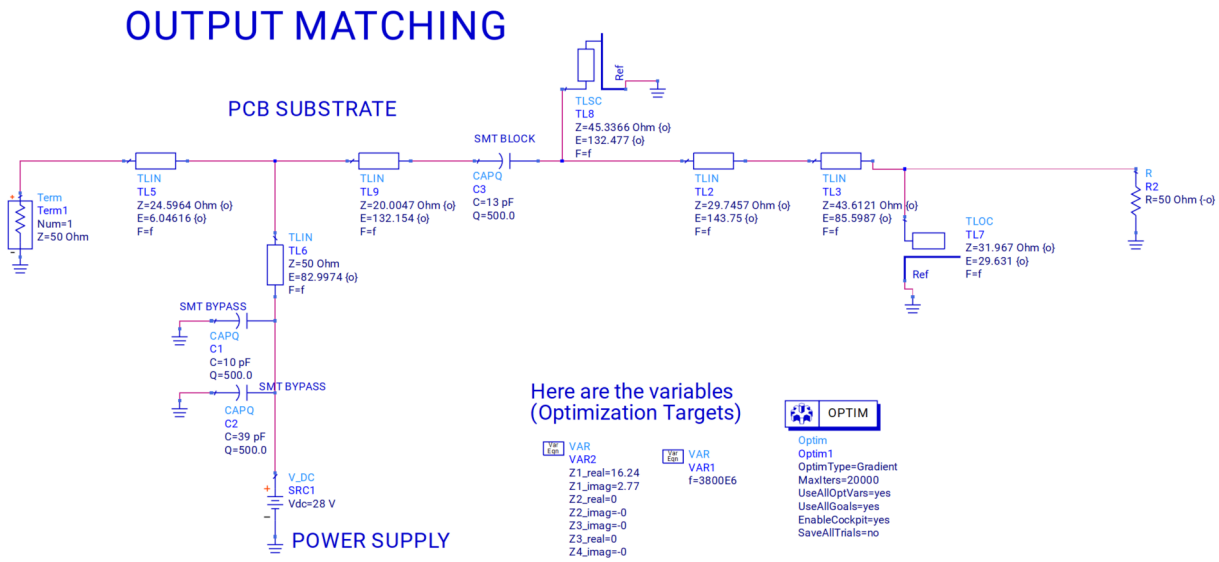
Frequency (MHz)	Z Source	Z Lead
500	20.2 + j16.18	51.7 + j15.2
1000	8.38 + j9.46	41.4 + j28.5
1500	7.37 + j0	28.15 + j29
2500	3.19 - j4.76	19 + j9.2
3500	3.18 - j13.3	14.6 + j7.45

We were recommended to add a small resistance to the gate of the transistor which will help with stability and matching by reducing the reflection coefficients. We do observe that higher resistance values reduce gain, power delivered, and PAE, so we start with a value of 3 ohms for load pull as recommended by a friend.

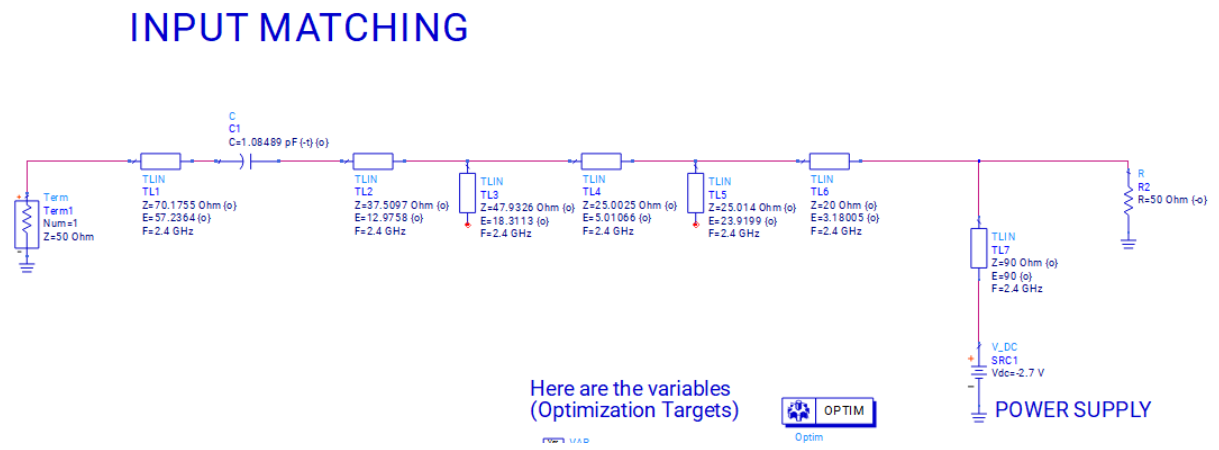


From this simulation, we see that the maximum power and maximum efficiency points for the fundamental frequency actually lie fairly closely on the smith chart. Since the trade-off in gain and output power seem relatively small compared to the gain in PAE from max power to max PAE point, we will start by using maximum PAE point.

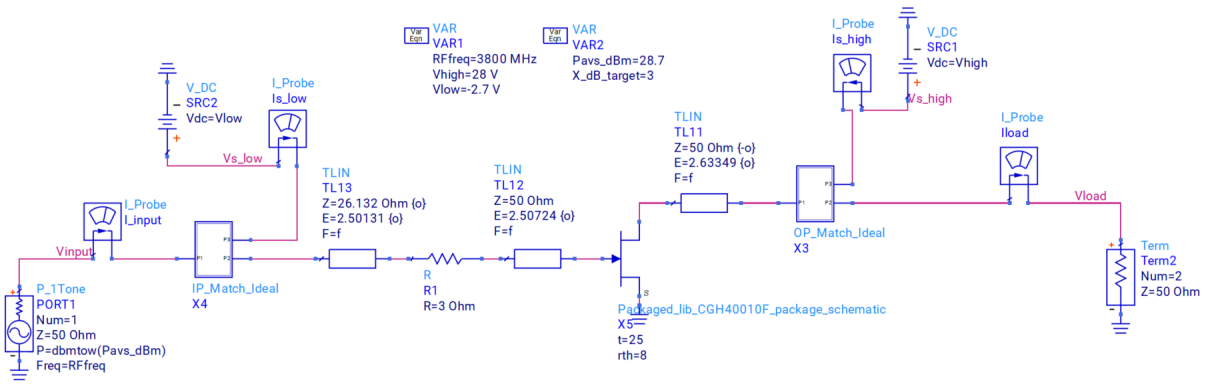
We referenced the input and output matching networks that also provide gate and drain DC biasing designed by Anurag and shown in his videos to help us better understand good matching network design for power amplifiers. Values shown are not final.



The output matching network design consists of a T junction to feed in the DC drain bias followed by a DC blocking coupling capacitor to the output. At the output, there is a short circuit and open circuit stub respectively to allow more optimization freedom in blocking harmonics.

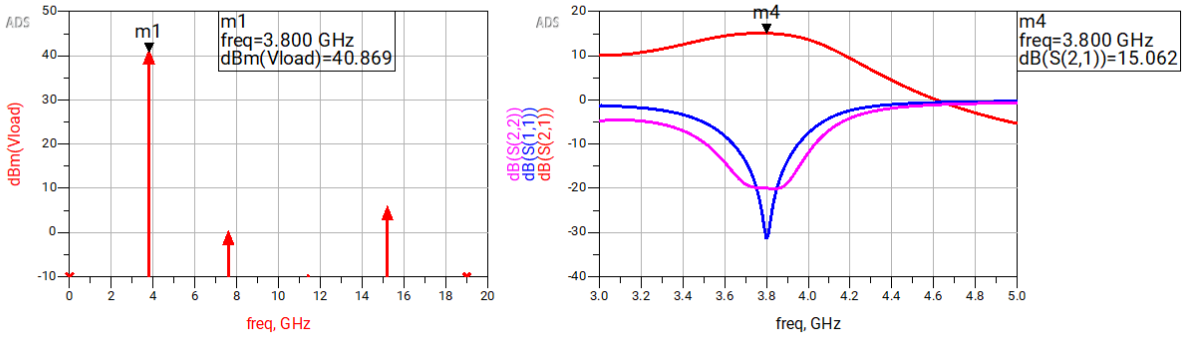


The input matching network consists of a coupling capacitor followed by simple two transmission line stubs for matching.



This is our initial single ended design w/ transmission lines. Since the transistor claims a Psat of 13W (41 dBm), if we aim for a large signal gain of 10dB+ we can set our input power around 29 dBm. After short optimization, we get these initial results:

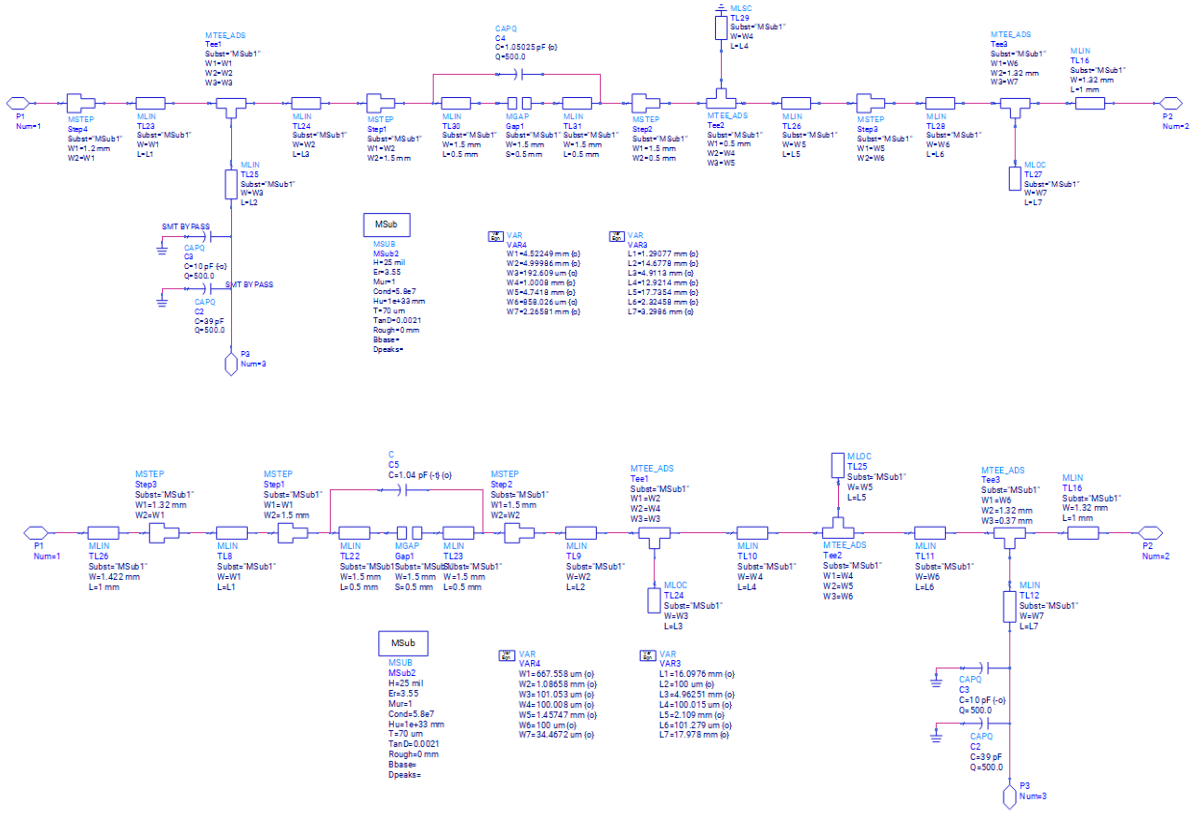
Pdel_dBm	PAE	Deff	LS_Gain_dB	Pdel_W
40.869	64.360	68.422	12.169	12.215



We deliver almost 41dbM of power with a PAE of 64% and large signal gain of 12 dB, matching and harmonics look decent.

We tried directly taking this transmission line based design and making it differential by mirroring a copy and coupling them with rat race couplers (180 ring hybrid), with the idea of converting to microstrip line representation after, but the circuit behavior changed significantly and ADS couldn't find a way to optimize the circuit. Thus, we decided to go back to our single PA design and convert it to microstrip line representation first before attempting to make it differential. In hindsight, we believe this is because the generated rat race coupler uses a microstrip line model, which may interact in weird ways with the rest of the circuit based on transmission line models.

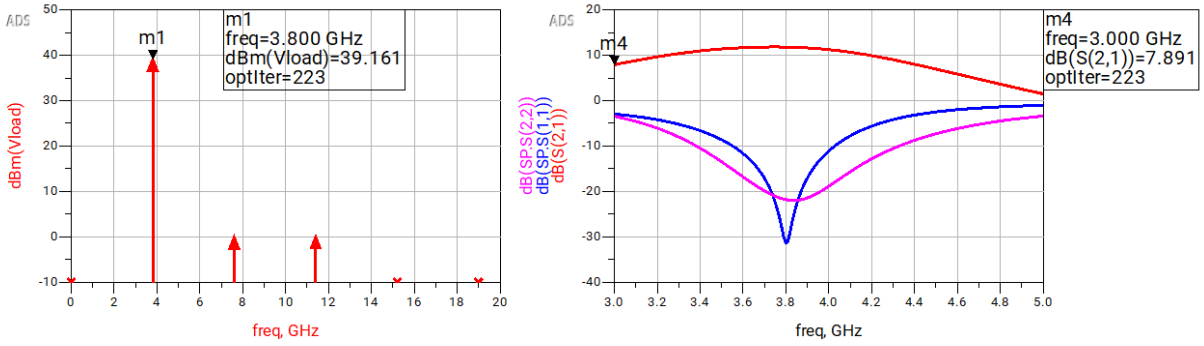
Output (top) and Input (bottom) matching circuits after conversion to microstrip line



At this point we must define our PCB substrate through MSUB, which we choose to be the RO4003. Substrate specs such as dielectric constant and dissipation factor are taken from the datasheet. Conductor is assumed to be copper, with trace thickness 70um and conductivity of 5.8e7.

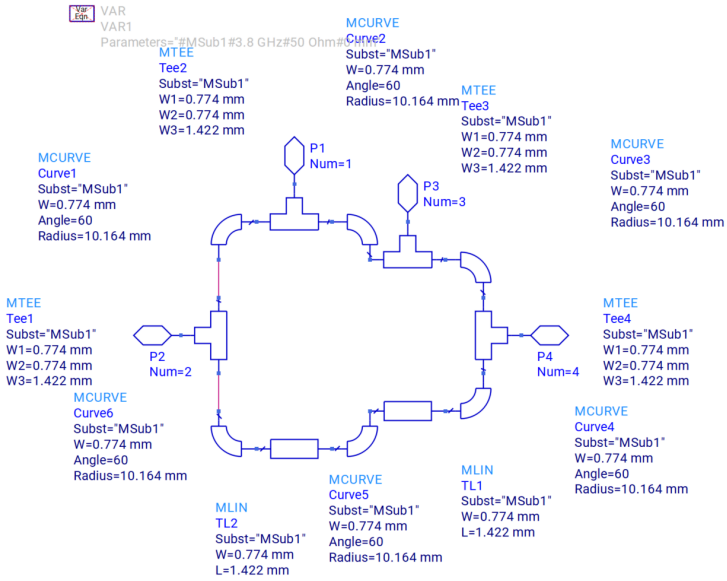
After reoptimization, we see that the performance drops off quite a bit.

optIter	Pdel_dBm	PAE	Deff	LS_Gain_dB	Pdel_W
223	39.161	54.824	60.651	10.161	8.244

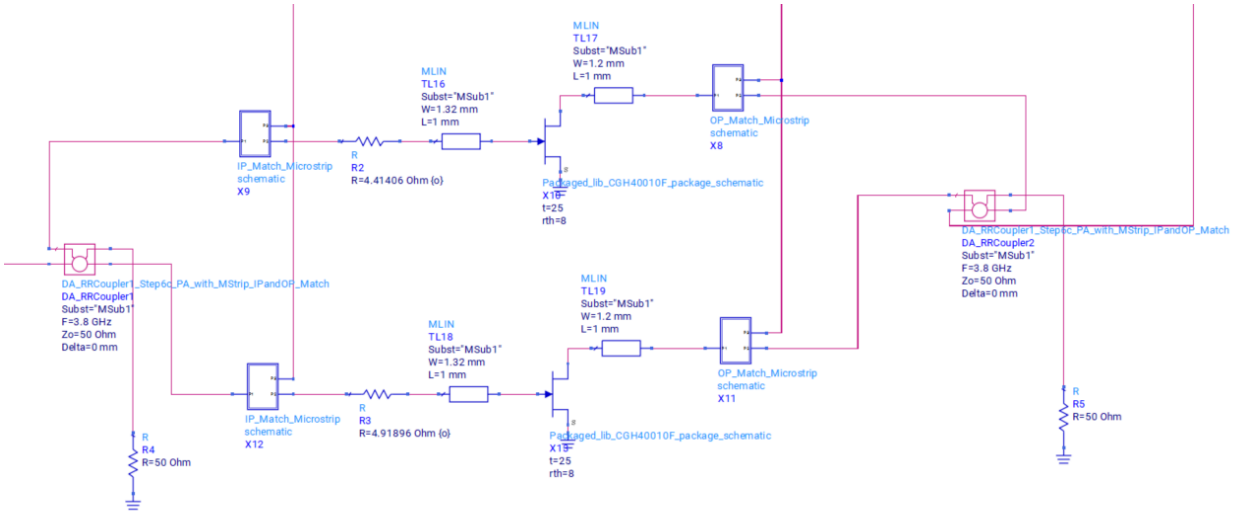


Now, we make it differential by adding a mirror copy and coupling the two with rat race couplers (used as 180 ring hybrid) at the input and output.

We design a rat race coupler with the help of ADS design guide. By specifying the desired center frequency, ADS can generate a rat race coupler made of microstrip line.

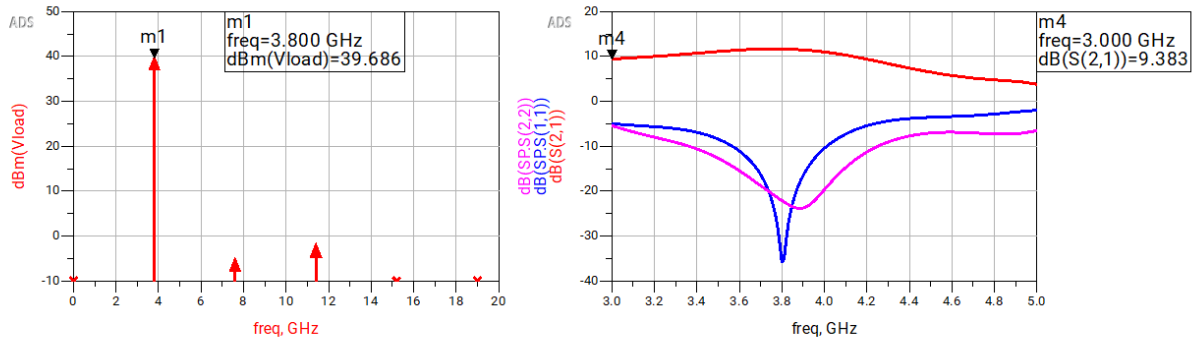


Here is the differential design (input/output and biasing not in picture)



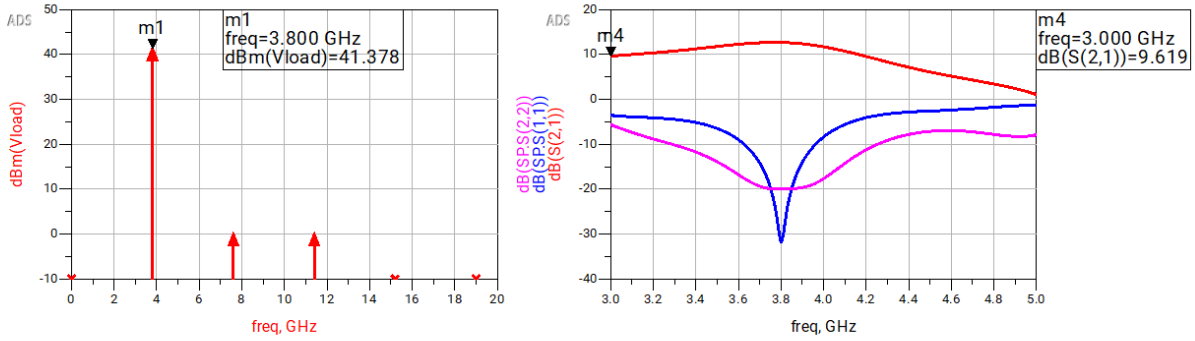
Here is differential performance before re-optimization

Pdel_dBm	PAE	Deff	LS_Gain_dB	Pdel_W
39.686	40.461	44.230	10.686	9.303



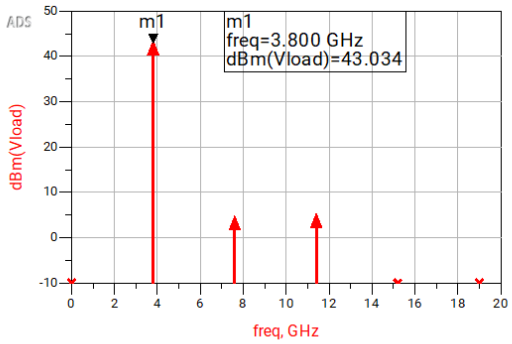
We see that the efficiency drops and the output matching is slightly disturbed, but the output power increases. We believe this is because with 2 PAs in parallel, the amplifier is able to handle a lot more power, so we need to operate at a higher input power to achieve the same relative gain compression which is where peak efficiency occurs. We found that by increasing the output power, we were able to get significantly better efficiency with small tradeoffs in gain.

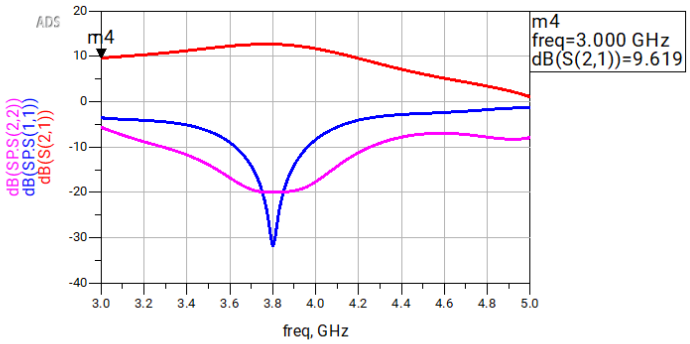
Pdel_dBm	PAE	Deff	LS_Gain_dB	Pdel_W
41.378	51.763	55.814	11.378	13.733



After some optimization, we obtain these results. Note that by simply increasing the input power and moving deeper into gain compression, we operate closer to saturation to obtain much higher efficiency at the cost of gain. Shown below is the same circuit simulated at an input power of 33dBm.

Pdel_dBm	PAE	Deff	LS_Gain_dB	Pdel_W
43.034	61.238	67.930	10.034	20.110

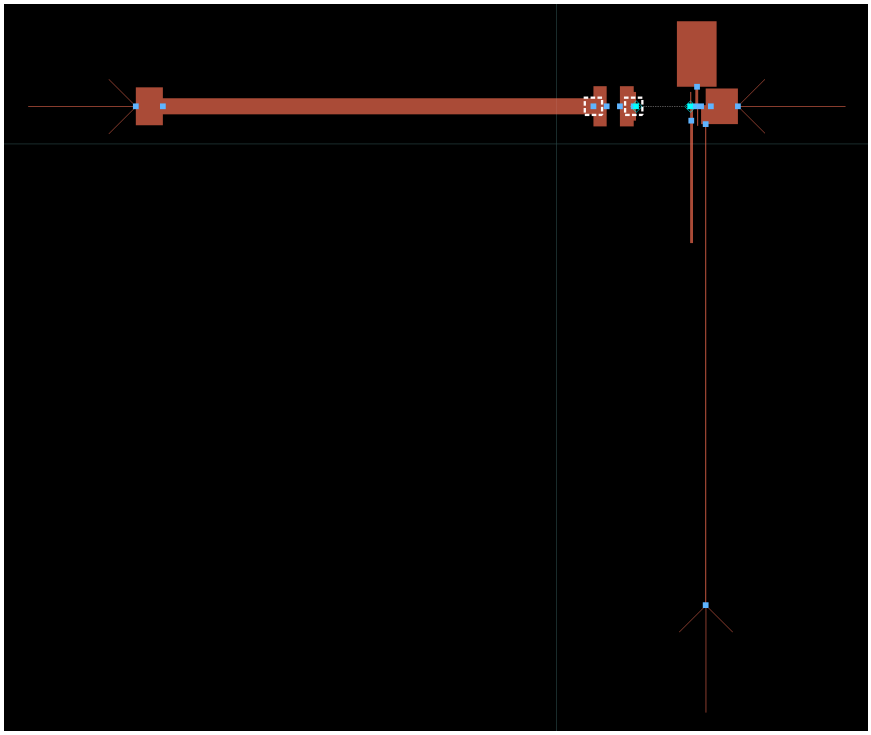


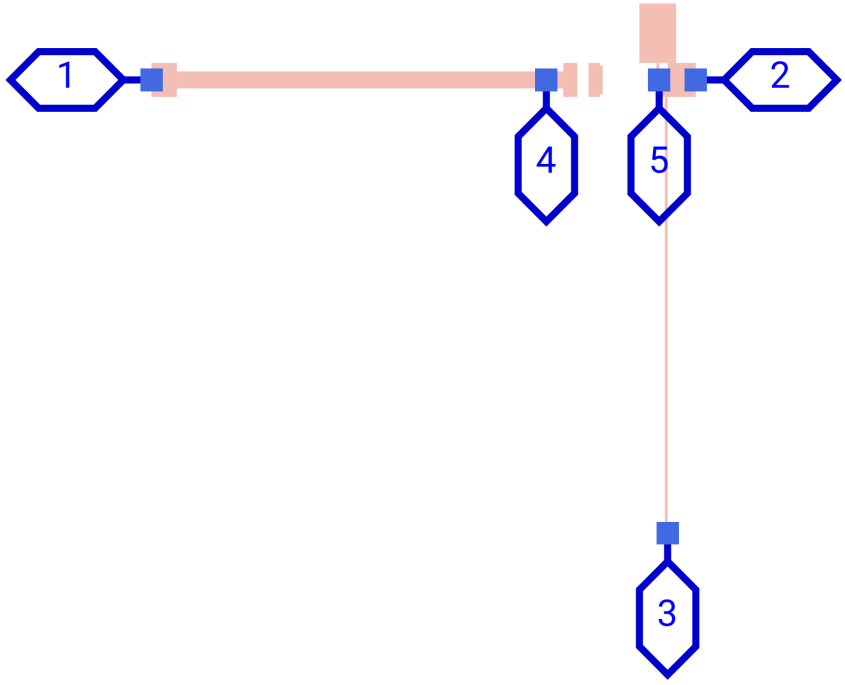


Multiple optimization runs were tested for the differential amplifier to get a satisfactory design. Depending on which variables were tunable and the optimization range, ADS would give different results with varying levels of performance. Additionally, we ran into convergence problems with the simulator when the microstrips joining at a T-junction had widths that were too different from each other. We also accidentally used a microstrip thickness of 70mm instead of 70um, which threw off our initial results.

Now that we have our design in microstrip, we convert it to a physical layout to simulate using more accurate EM models. We laid out the microstrip in 4 distinct sections: rat race coupler, input matching network, output matching network, and an MGAP for the gate resistor + transistor interfacing section.

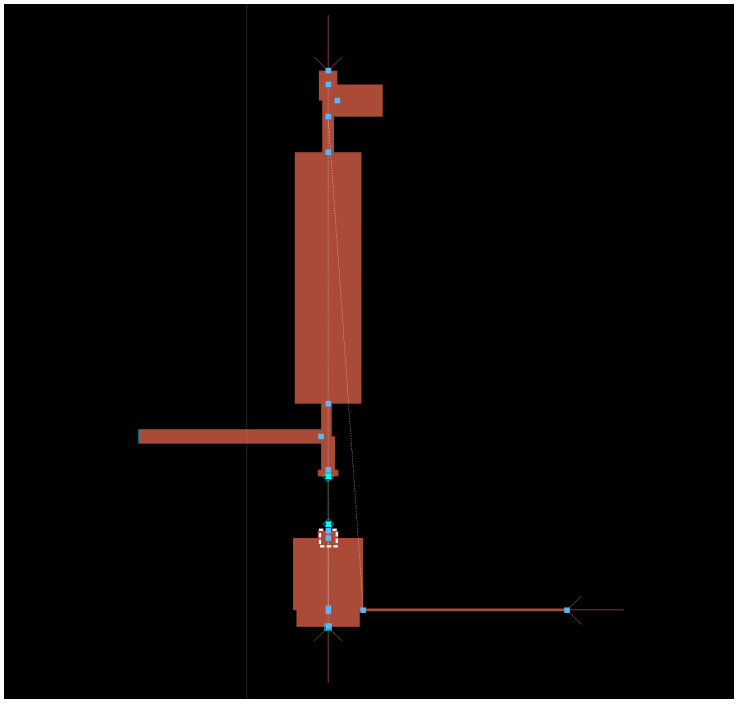
Input matching layout and EM cosim symbol

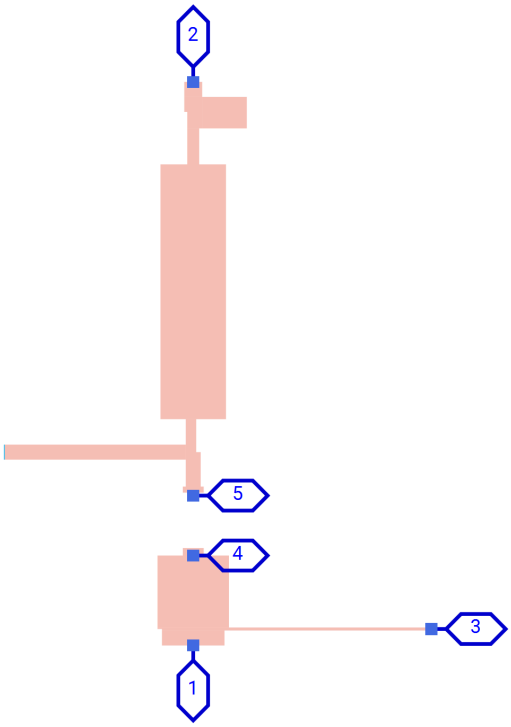




Port 1: input signal
Port 2: output to transistor
Port 3: Voltage bias
Port 4 and 5: interface with capacitor in input matching network

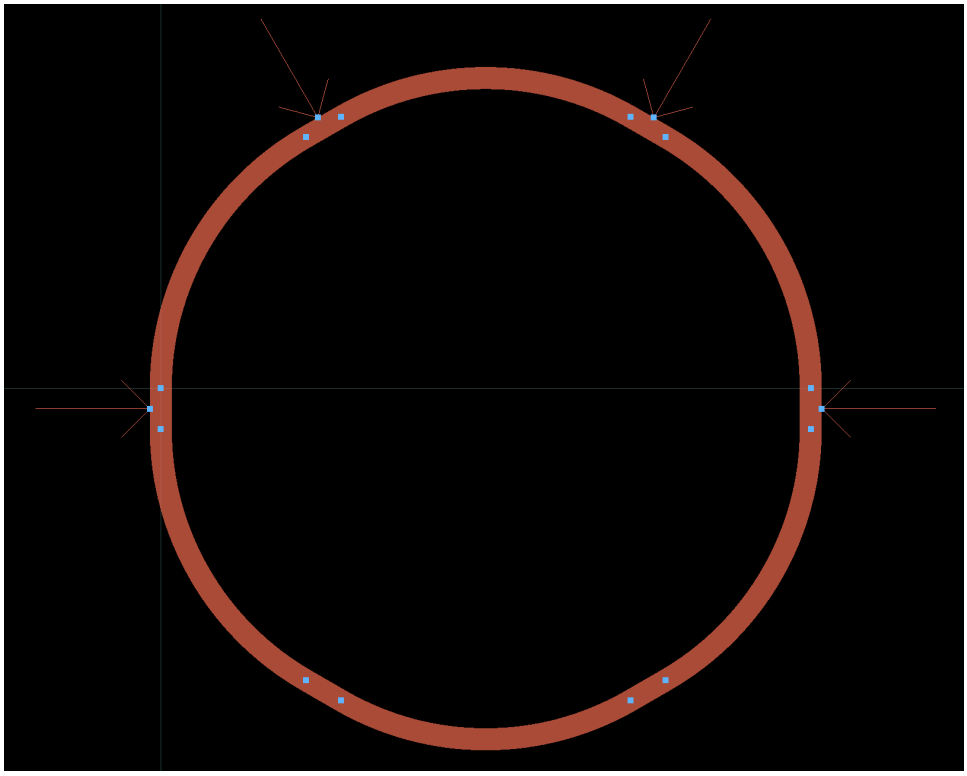
Output matching layout and EM cosim symbol

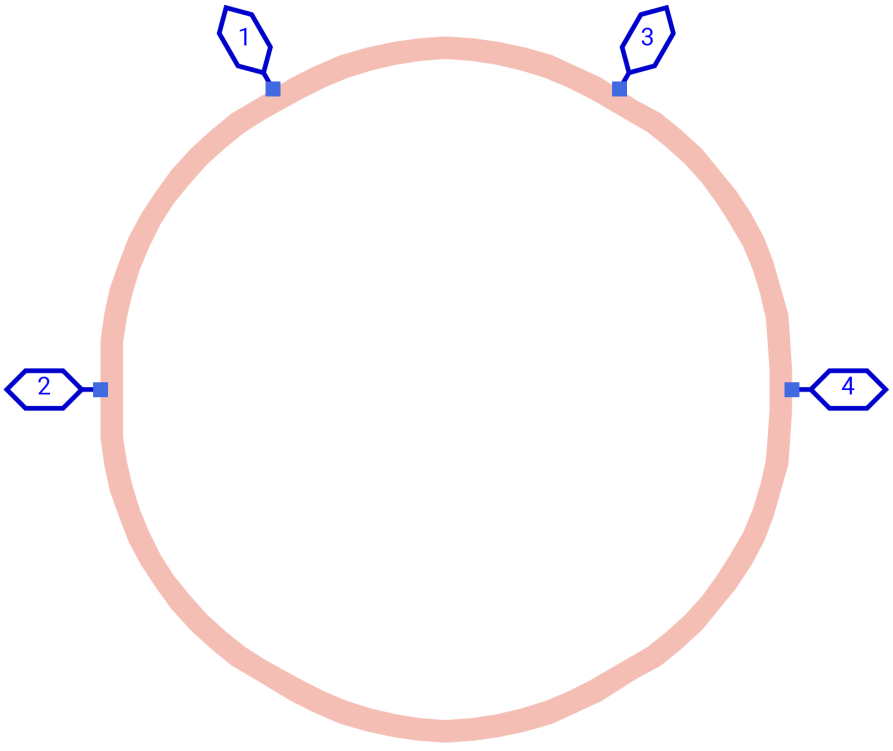




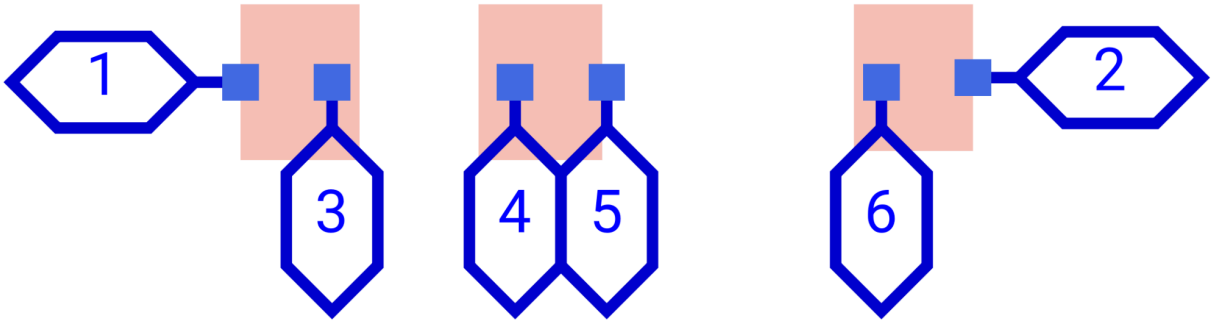
Port 1: input from transistor
Port 2: output signal
Port 3: Voltage bias
Port 4 and 5: interface with capacitor in input matching network

Rat race coupler layout and EM cosim symbol



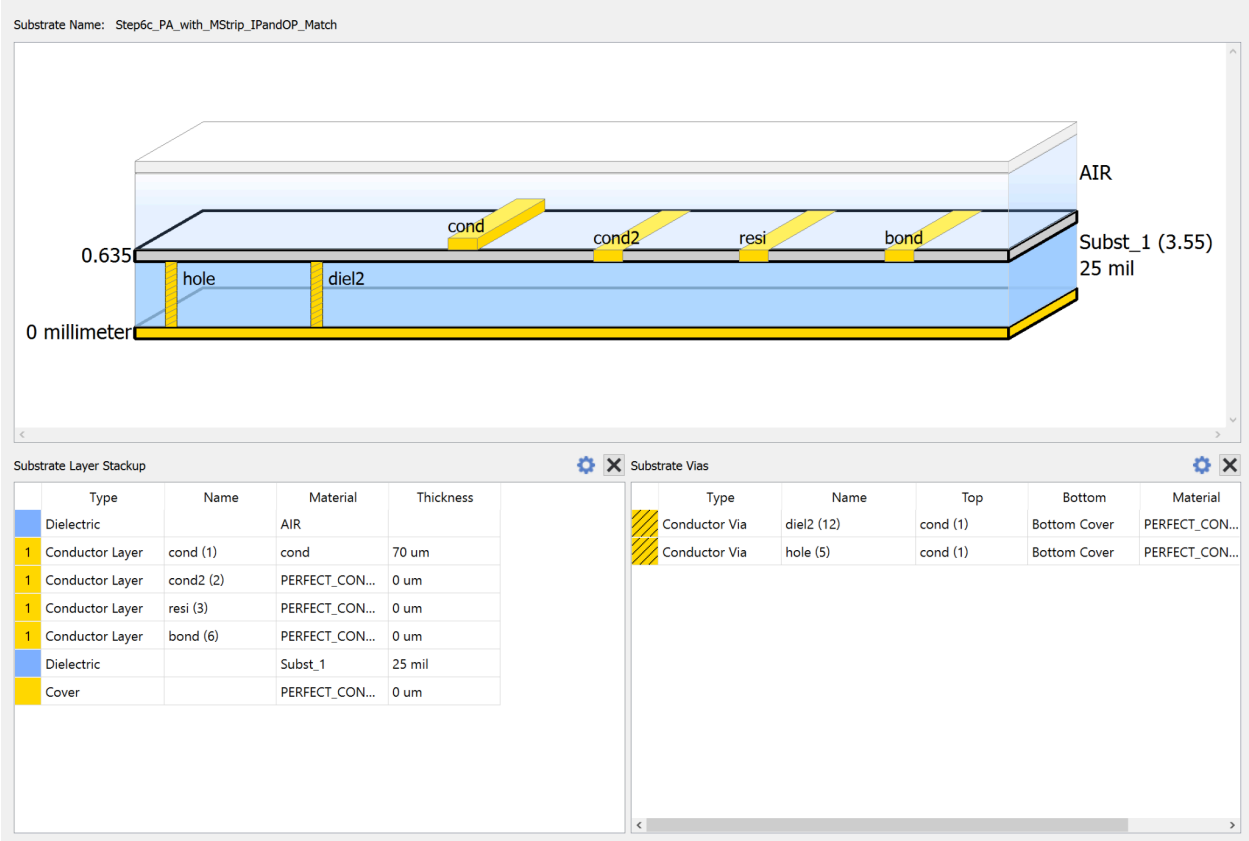


Transistor and bias resistor EM cosim symbol



Port 1: input from input matching network
Port 2: output to output matching network
Port 3 and 4: interface with bias resistor
Port 5 and 6: interface with transistor gate and drain (source is grounded)

EM cosim substrate

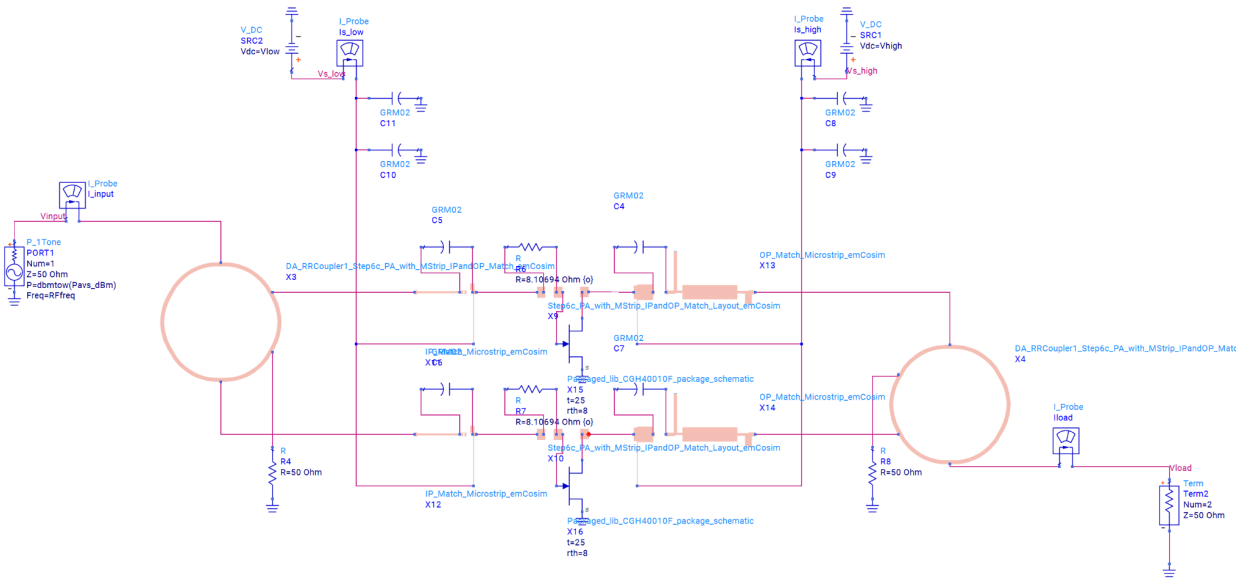


MSub

MSUB
MSub1
H=25 mil
Er=3.55
Mur=1
Cond=5.8e7
Hu=1e+33 mm
T=70 um
TanD=0.0021
Rough=0 mm
Bbase=
Dpeaks=

We define the substrate to be used for the more accurate Momentum based EM simulation of our microstrip layout models.

Full layout schematic:



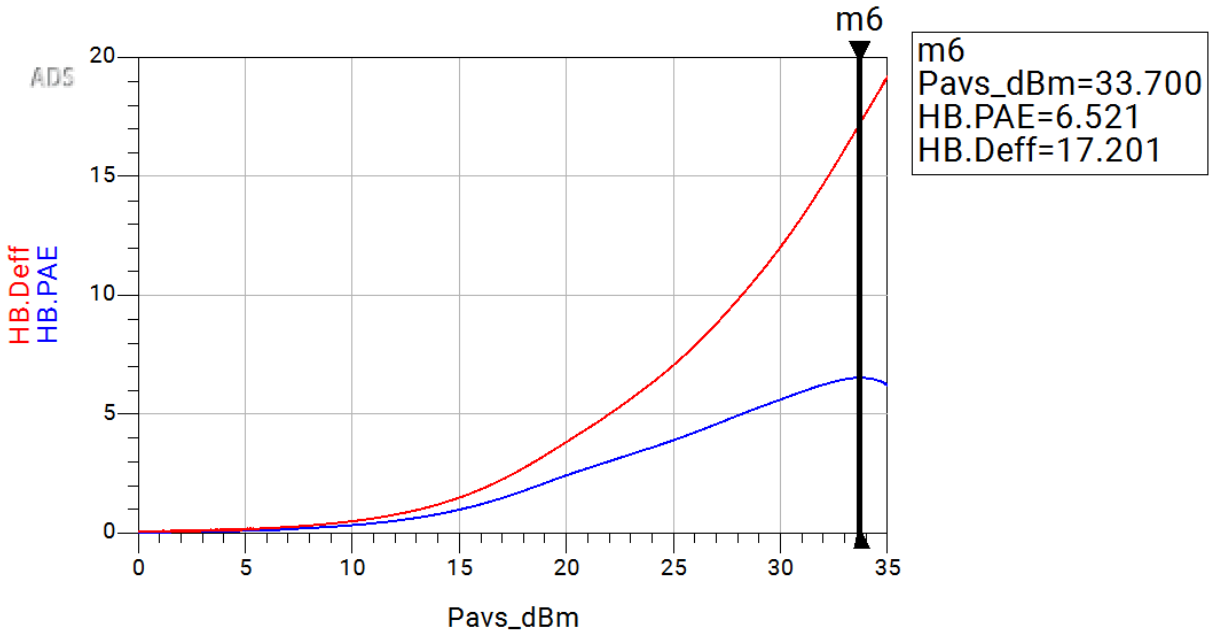
Here is our final differential amplifier designed based on real lumped elements. All ideal microstrip has been replaced with laid out microstrip with parameters found through Momentum base EM simulation. Ideal capacitors have been replaced with the closest value caps we could find from the Murata capacitor library (https://www.murata.com/-/media/webrenewal/tool/library/common-pdf/dynamic-model/component-list-d-mlcc-2410).
Bypass capacitors were added to the DC biasing points to short any stray RF power that might leak through from either the amplifiers or DC sources.

*Although the project spec says to use realistic models for all lumped elements, we couldn't find a library for non-ideal resistors and a friend confirmed with the professor that ideal resistors were ok for now.

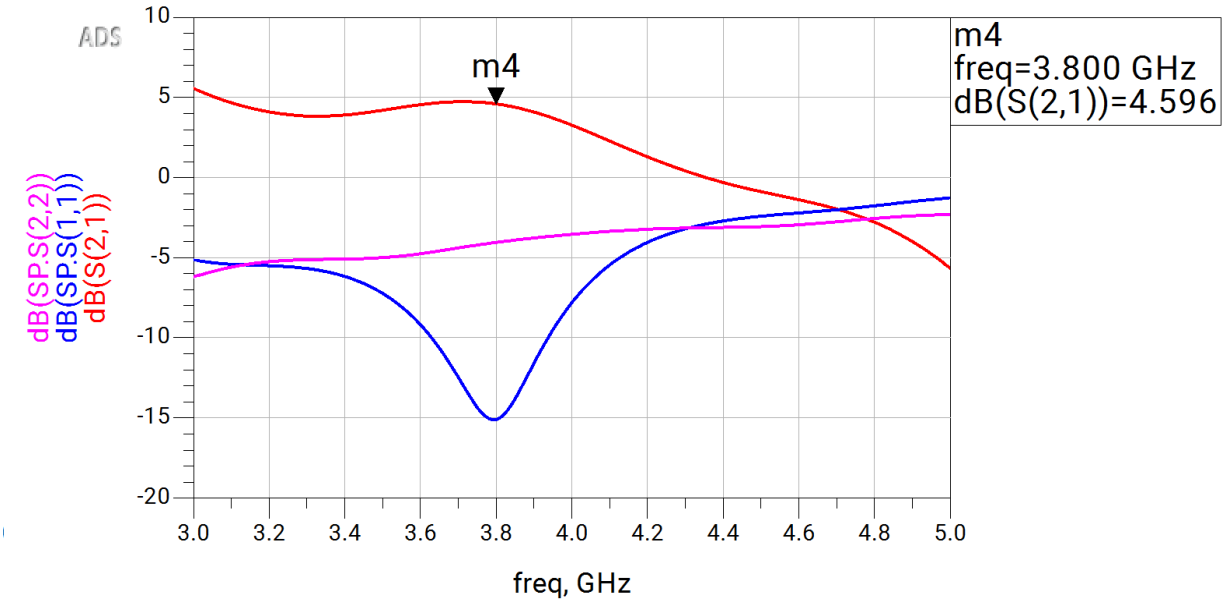
Final circuit simulations:

*These plots were made with the help of Anurag's sample workspace. Power is calculated by measuring the current and voltages at all nodes and then calculating Pavg = ½ * Re{V*I}, with ammeters visible in every schematic we have shown above.

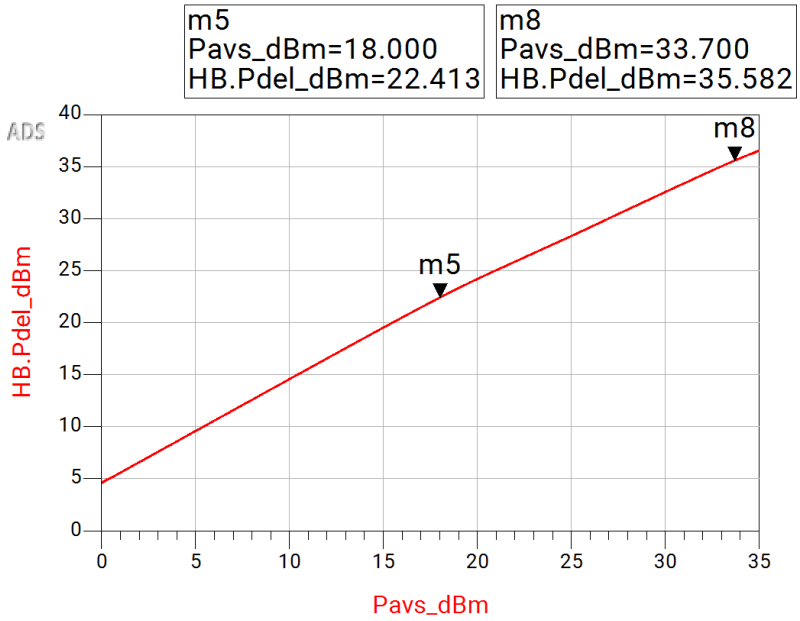
PAE vs input power



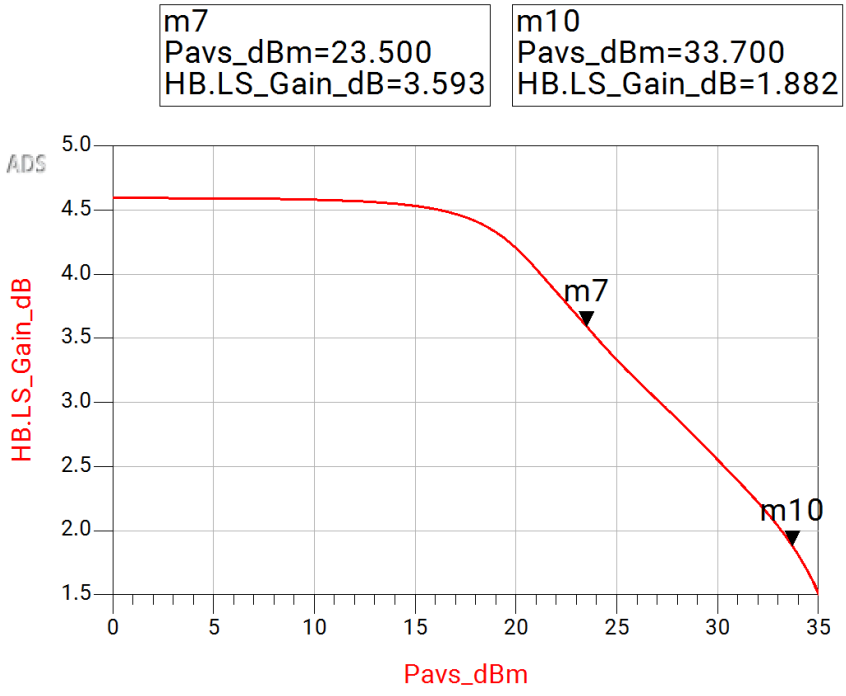
Power over frequency (input power set at max PAE point = 33.7dBm)



Output power vs input power



Gain vs input power



*Note that there is a discrepancy in large signal gain in our power vs frequency and input power vs output power plots. This is because the power vs frequency plot was computed using s-parameters, which doesn't factor in gain compression from input power delivered, resulting in a higher gain than what the gain actually is. The actual output power for this plot should be around 3dB lower than where it currently is.

*Although it was listed as a metric in the project spec, the power bandwidth doesn't appear to be particularly meaningful in this case since our amplifier barely works. S-parameters suggest that the gain remains fairly consistent before rolling off after 3.8Ghz, but we did not simulate results below 3Ghz since the circuit doesn't function anyways. We can do a rough approximation by using the center lump of the S(2,1) curve which corresponds to the large signal gain, which shows a peak at 3.7Ghz and bandwidth of 500Mhz for 1dB drop off.

Evaluation of final results:

Max PAE (%)	**Large signal gain (dB)**	**Output power (dBm)**	**Power Bandwidth (Mhz)**
6.5%	**1.9**	**35.6**	**500**

The performance of our final laid out circuit is drastically worse than what we had in the ideal microstrip line based circuit. We tried multiple solutions to no avail and eventually ran out of time. There's a lot that changes from the transition between ideal microstrip and EM based layout simulation, and something likely went very wrong in this process.

Our best hypothesis is that we were overly aggressive with optimization and did not give enough consideration to having realistic width ratios of different microstrip segments that were going to be joined. In particular, we allowed ADS to freely change our transmission line impedance and therefore microstrip line width, resulting in lots of high transition ratios in the layout of our microstrip line matching networks. For our optimization runs, we allowed very broad ranges of values to be tried by the optimizer, meaning we likely optimized the circuit into a weird, non-realistic set of parameters that work well with the ideal model equations but fall apart upon more realistic EM simulations. For example, in both the input and output matching networks there was a microstrip line that was substantially thinner than the other lines by a ratio of up to x20. Although ADS did warn us about this during initial simulations, it was already too late and there wasn't a simple way to fix it without starting from scratch.

If given more time, the biggest thing we would do differently is to be more restrictive on the optimization. Instead of allowing the optimizer to change all parameters freely, we would start with a more restrictive set of limitations, for example by keeping the impedances of the transmission lines in the matching networks set to 50 ohms, and only allowing the optimizer to change electrical length. In addition, we would start with smaller optimization ranges to stop it from deviating too far from the design we obtained from smith chart matching and linecalc conversion from transmission line to microstrip, since otherwise our matching design work would just be overridden by the optimizer.