EE 215A Analog Integrated Circuits Design Final Project

Justin Hu, Jun Sang Lee

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1. Minimum power design - Justin Hu

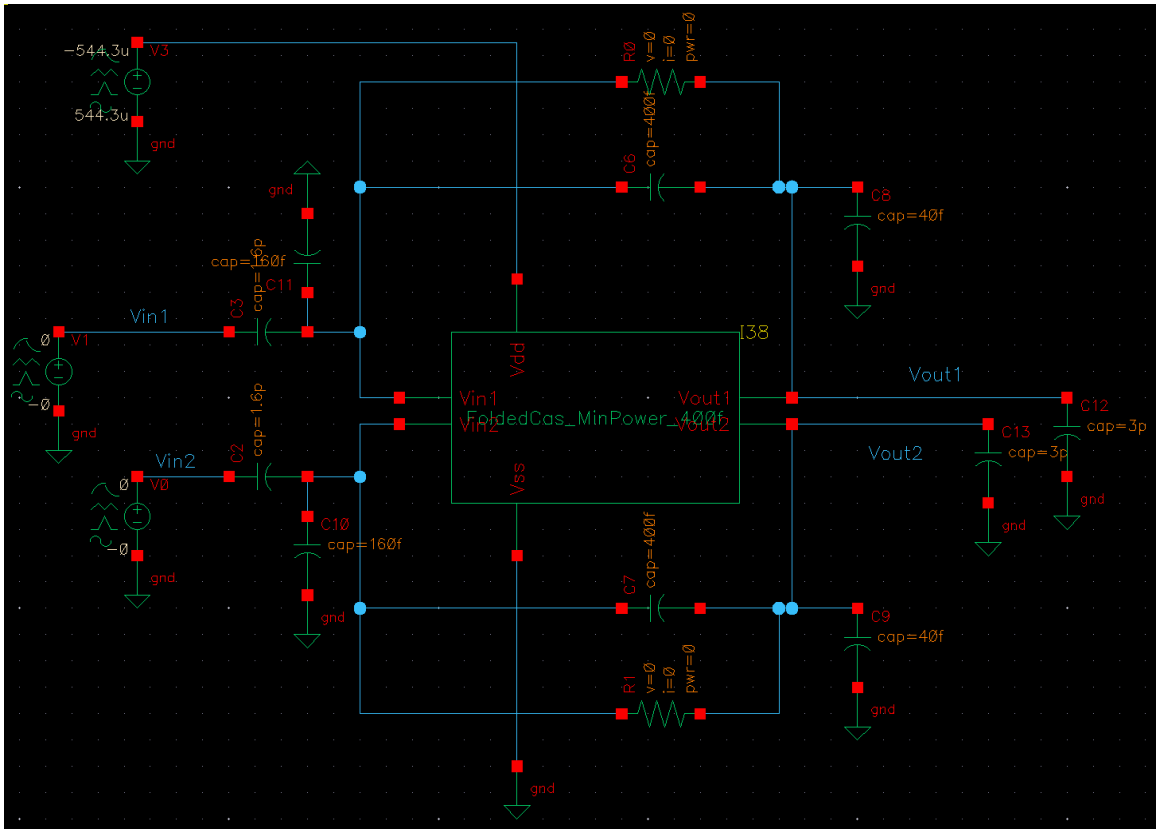
Results: 979.74uW DC Power consumption @ 39.92ns settling time w/ 1.8% gain error

2. Minimum settling time design - Jun Sang Lee

Results: 14.99mW DC Power consumption @ 7.96ns settling time w/ 1.46425% gain error

Minimum Power Design (Justin Hu)

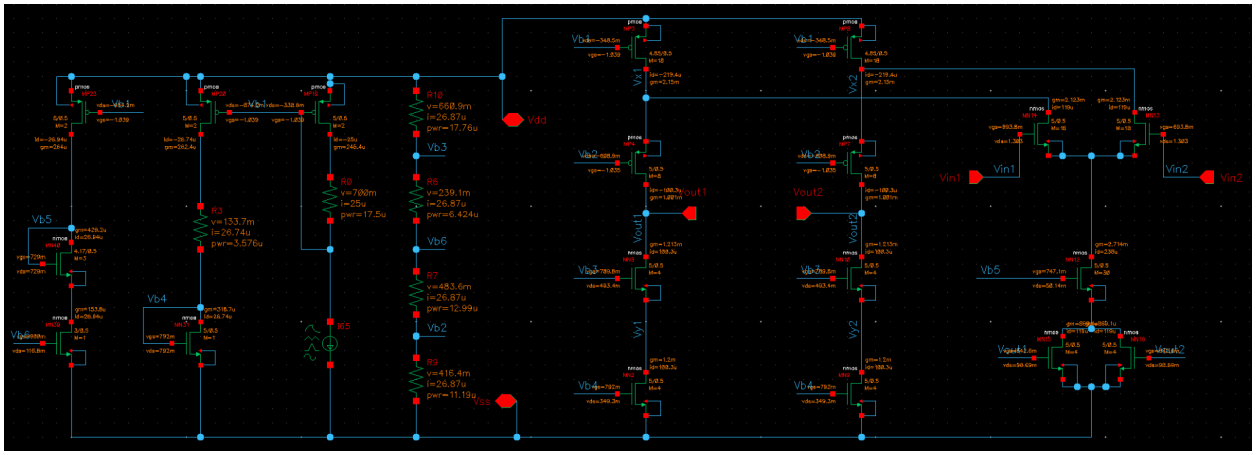
High level schematic with closed loop feedback, all parasitics, and load capacitors



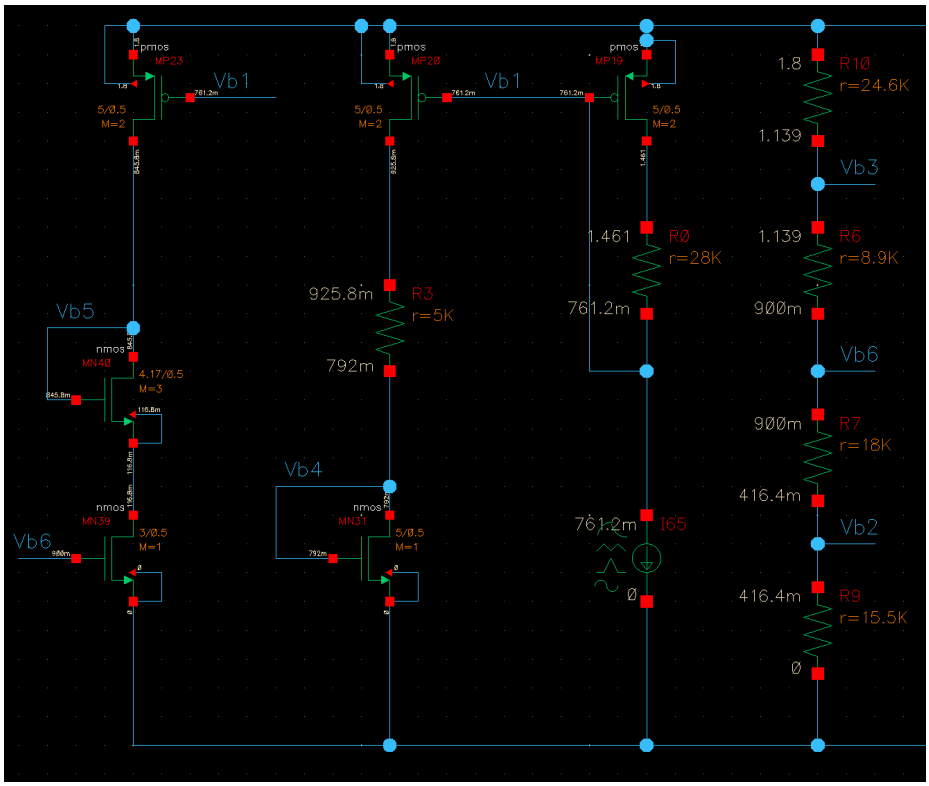
From the schematic, we also see a total DC current draw of **544.3uA**, corresponding to a total DC power consumption of 544.3uA*1.8V = **979.74uW.** This is the minimum power achieved by my design.

Feedback resistors were set large enough as to not affect the output settling value within our time window of interest. I chose capacitor values of **1.6pF and 400fF** for my feedback capacitors. Through simulation, I found that feedback capacitors that were too large would slow the circuit down by introducing too much capacitance to the output, but feedback capacitors that were too small would reduce the closed loop gain and also make the circuit slower due to reduced gain. These particular values were selected after sweeping a range of values to find the optimal point for my particular circuit. I also found that ideal feedback capacitor size was positively correlated with the total current draw (power) of the amplifier, which explains why the ideal feedback capacitance for this design was so small, close to the minimum allowed value of 1.2pF and 300fF. Since my partner is designing for minimum settling time at a much higher power, the ideal feedback capacitor sizes for his circuit are much larger than mine.

Overall open-loop schematic (with operating points)



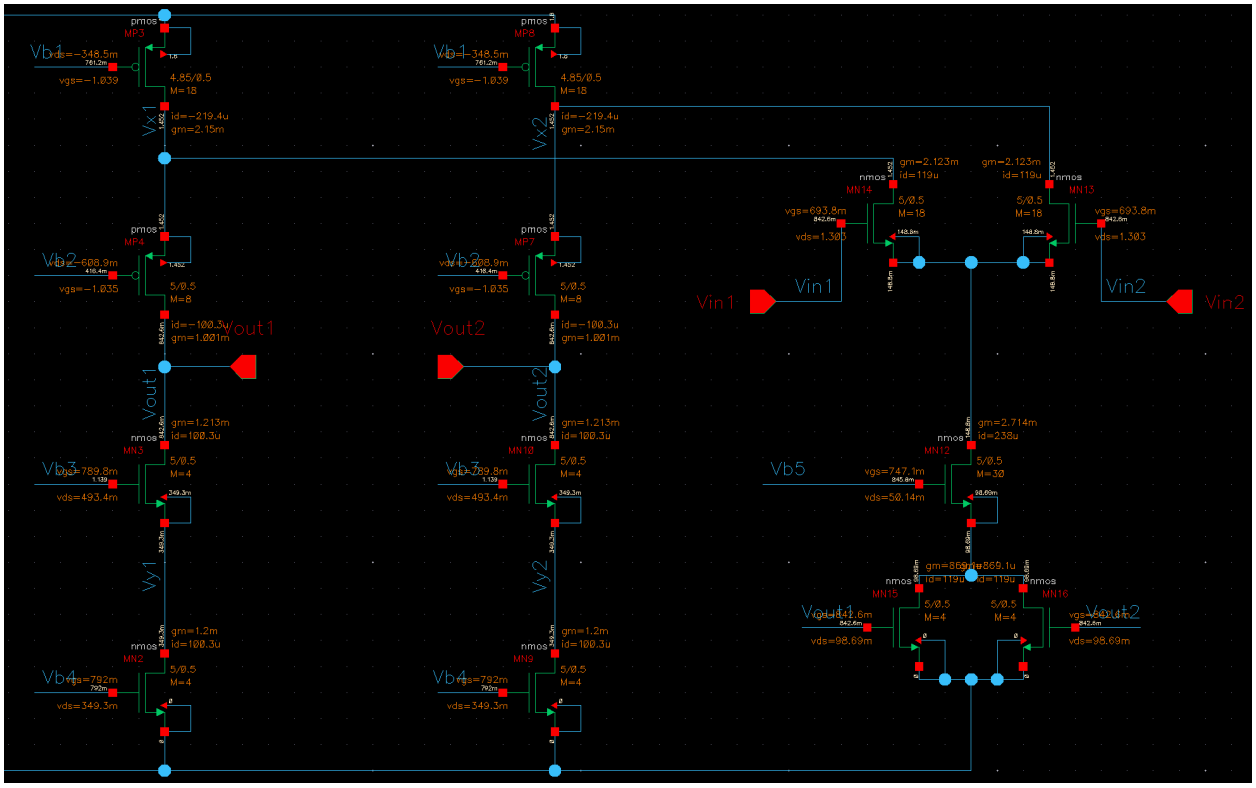
Biasing network closeup (current mirrors and voltage divider) w/ sizes & biasing voltages



Total resistance used for current mirrors is 5k + 28k = 33k ohms
Total resistance used for voltage divider is 24.6k + 8.9k + 18k + 15.5k = 67k ohms
Total resistance used is <u>100k ohms</u>, the exact amount allowed by the project specifications.

The biasing network draws around 105.5uA of total current after modifications to save power. The ideal current source draws 25uA through the first pmos before being mirrored to the 2 other branches, due to imperfect mirroring the 3 branches draw around 78.6uA total (instead of 75uA). The resistive divider branch has 67k ohm total resistance meaning 1.8/67k = 26.9uA current draw.

Folded cascode amplifier closeup (~201uA through cascodes, ~238uA through input branch)

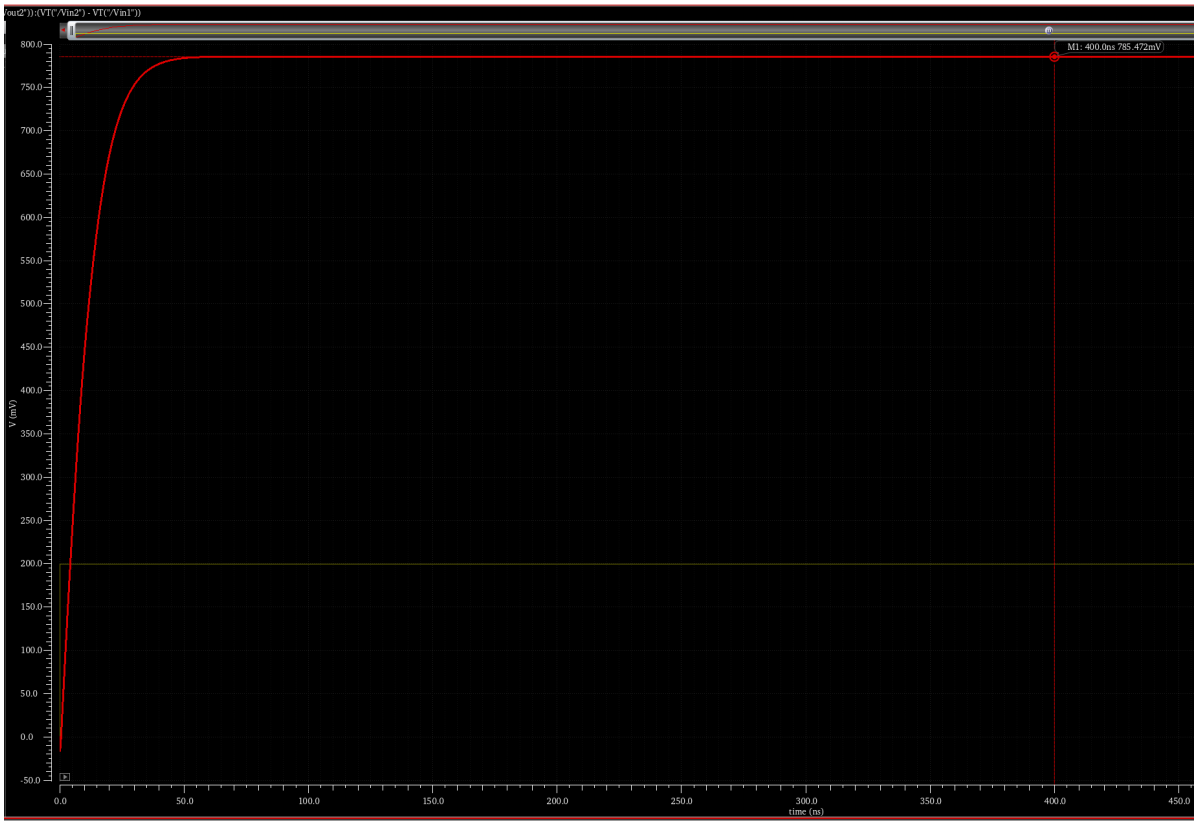


Drain-source voltages of the cascode branch were distributed in a 350/550/550/350 fashion from the top down. The idea was to give the middle transistors more Vds, since they are handling the majority of the output swing. The pmos are sized to be twice as large as the nmos for the same current so that the overdrives are around the same to account for pmos being inherently weaker due to lower carrier mobility and hopefully achieve greater headroom.

The input branch was not given strict Vds assignments, but the goal was for the tail current mirror and CMFB transistors to not drop too much voltage so that the input transistors can be a reasonable size. Since the common mode output level was defined to be 900mV and the threshold voltage for nmos is around 660mV, the input pair needs at least 700+mV Vgs, meaning the tail current and CMFB combined should drop less than 200mV. If the Vgs were made any lower, the overdrive would be too low and the input transistors would need to be made extremely large to compensate and match the current draw of the tail current mirror.

For this particular design, I also made the input and cascode branch current draw slightly mismatched to increase gain efficiency. Notice how the top pmos has a multiplier of 18 (90um), while the cascode branch pmos has a multiplier of 8 (40um). This means that slightly more current is forced to flow through the input branch, which I hypothesized would increase the output current swing generated when the circuit is drawing the same total current and therefore increase open loop gain and closed loop speed. Although the effect is complex, I managed to find this sizing which did achieve higher efficiency, allowing me to reducing the total power consumption by around 30uW while achieving similar settling time.

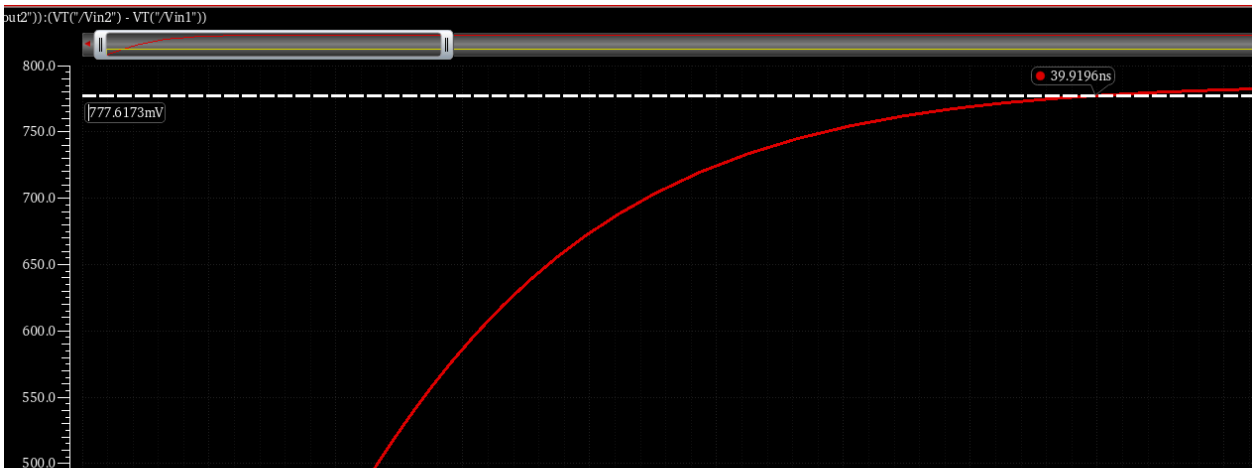
Closed Loop Transient Simulation:



Given a differential input step of 200mV (polarity reversed so both input and output can be seen together), the resulting output step settles at a value of 785.472mV, taken after 400ns to ensure it has settled properly. This corresponds to a linear gain of 785.472/200 ~ **3.9274**. Since our ideal gain is 4, this is a gain error of (4 - 3.9274)/4 ~ **1.8%**. Thus, this amplifier meets the gain error and output swing requirements in the spec.

To find the 1% settling time, we find the 1% settle boundary:
Upper bound: 785.472*1.01 = 793.3267
Lower bound: 785.472*0.99 = 777.6173

Since this is a low power design, the amplifier is slow (weak) and barely overshoots, peaking at about 785.844mV (only 0.4mV above settled value) at 65.5ns before coming back down. Thus, the 1% settling time is determined by the lower bound.



Zooming into the initial rise, the amplifier reaches the 1% settling lower bound after around **39.92ns**. Thus, this amplifier meets the large signal settling time requirements.

In summary:

This design uses **979.74uW of power** to achieve a **39.92ns settling time** with a linear closed loop **gain of 3.9274**, which is a **gain error of 1.8%** from our target gain of 4.

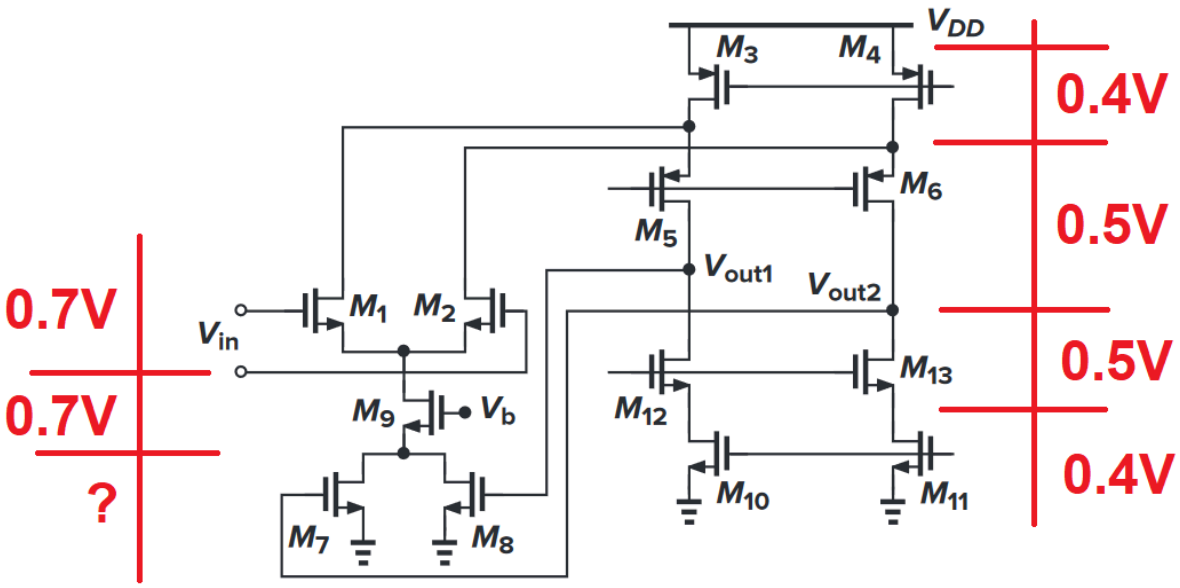
General design philosophy:

I started by designing a circuit which has equal current draw of 1mA through the cascode and 1mA through the input branch. The vast majority of my time spent was getting this initial working design. I fixed the current draw and Vds of the transistors and set transistor widths which allowed for reasonable bias points without resulting in too much capacitance, which would slow down the circuit. Once I got the circuit biased and working, I simply had to scale the circuit down and reduce the power consumption. My initial design was around 13ns @ 4mW. The first issue I encountered with downsizing was reducing power consumed by my biasing network. It initially drew around 450uA total, so I scaled it down by a little over 4x to 105uA. In this process, I had to slightly modify the finger width for the input tail biasing mirror (the only transistor in my circuit with a finger width not equal to 5um) since the multiples I initially settled on couldn't be perfectly divided, but feedback allowed the circuit to tolerate this nonlinear change without issue.

After scaling down my initial circuit and optimizing the biasing network, my design was using around 1015uW of power. Although this already seems decently good, I was so close to breaking 1mW, so I started brainstorming and eventually came up with the cascode-input mismatch idea that I explained above. In order to simplify the initial design process, I restricted the degrees of freedom I had in my initial design so that the two branches had the same current draw. With the experience I've gained in this project and more time, perhaps I could explore this unbalanced design further and make it even more efficient.

Minimum Settling Time Design (Jun)

The open loop design topology is the folded cascode opamp with common mode feedback through the tail current of the input differential pair. The design process was an iterative process that involves distributing a set amount of headroom to each transistor in the structure. The headroom distribution of the VDD of 1.8V is shown below.

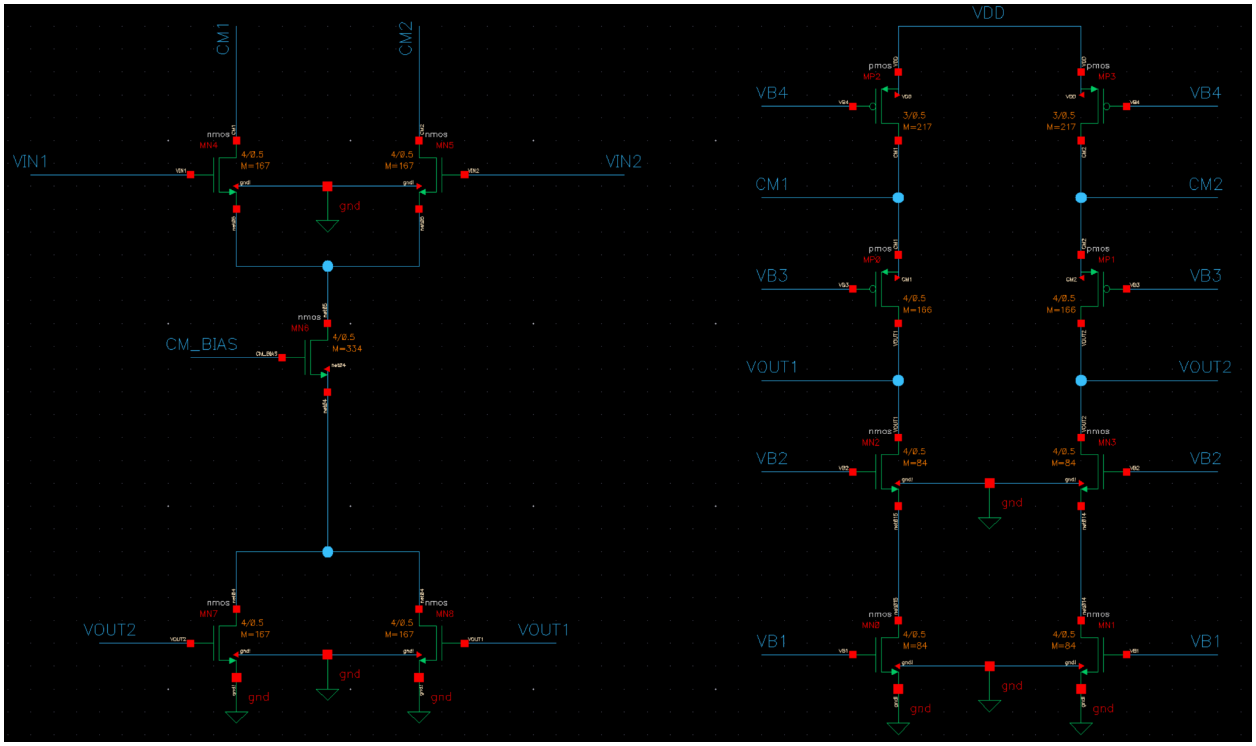


Before design, a specific width and length are pre-determined for each transistor. The nmos transistors start at a W/L of 400um/0.5um, while the pmos transistors start at a W/L of 800um/0.5um. The pmos transistors are double the length of the nmos transistors due to difference in mobility and driving strength.

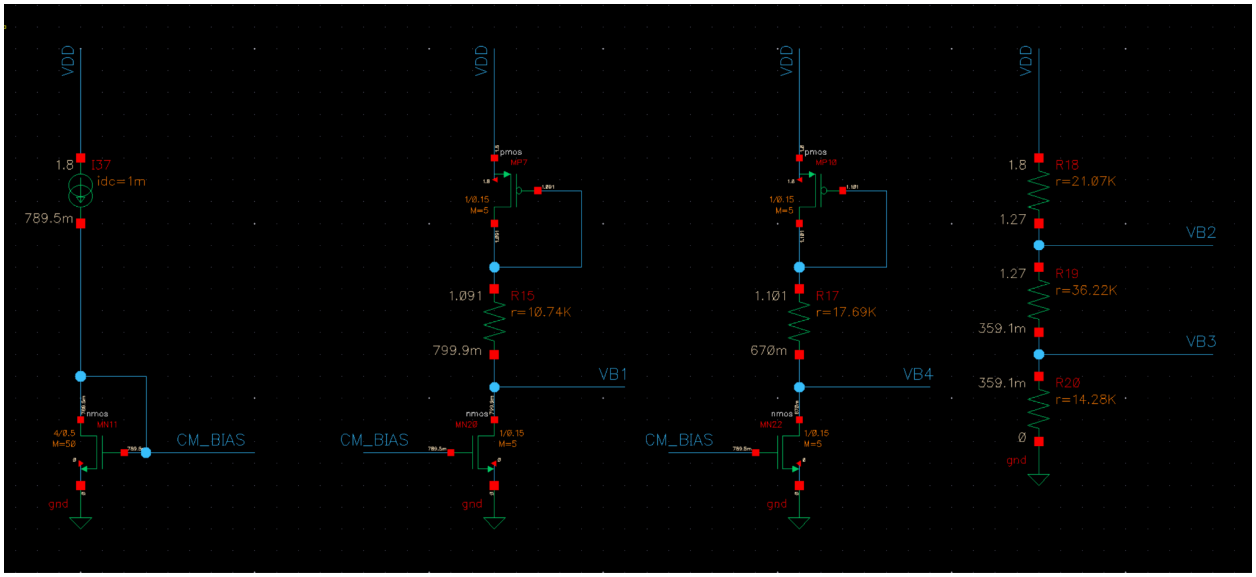
Starting with the bottom transistors of a single stage structure, the optimal bias point is found for each transistor to give each transistor it's designated headroom. The common mode feedback transistor is only added after the rest of the circuit is biased since it can carry little headroom.

After biasing, the single stage structure is translated into the differential structure, which requires some adjusting of the top pmos biasing to enforce headroom conditions. This results in very high open loop gain of little bandwidth.

The transistor widths can now be scaled now equally to lower current draw until the 15mW power budget is satisfied, without affecting bias values and headroom conditions. Due to non-integer indivisibility of odd numbers, the transistor width and multiple ratio was changed to accommodate for fractional multiple values. The finished open loop design is below.



The bias voltages were generated through the circuits below.



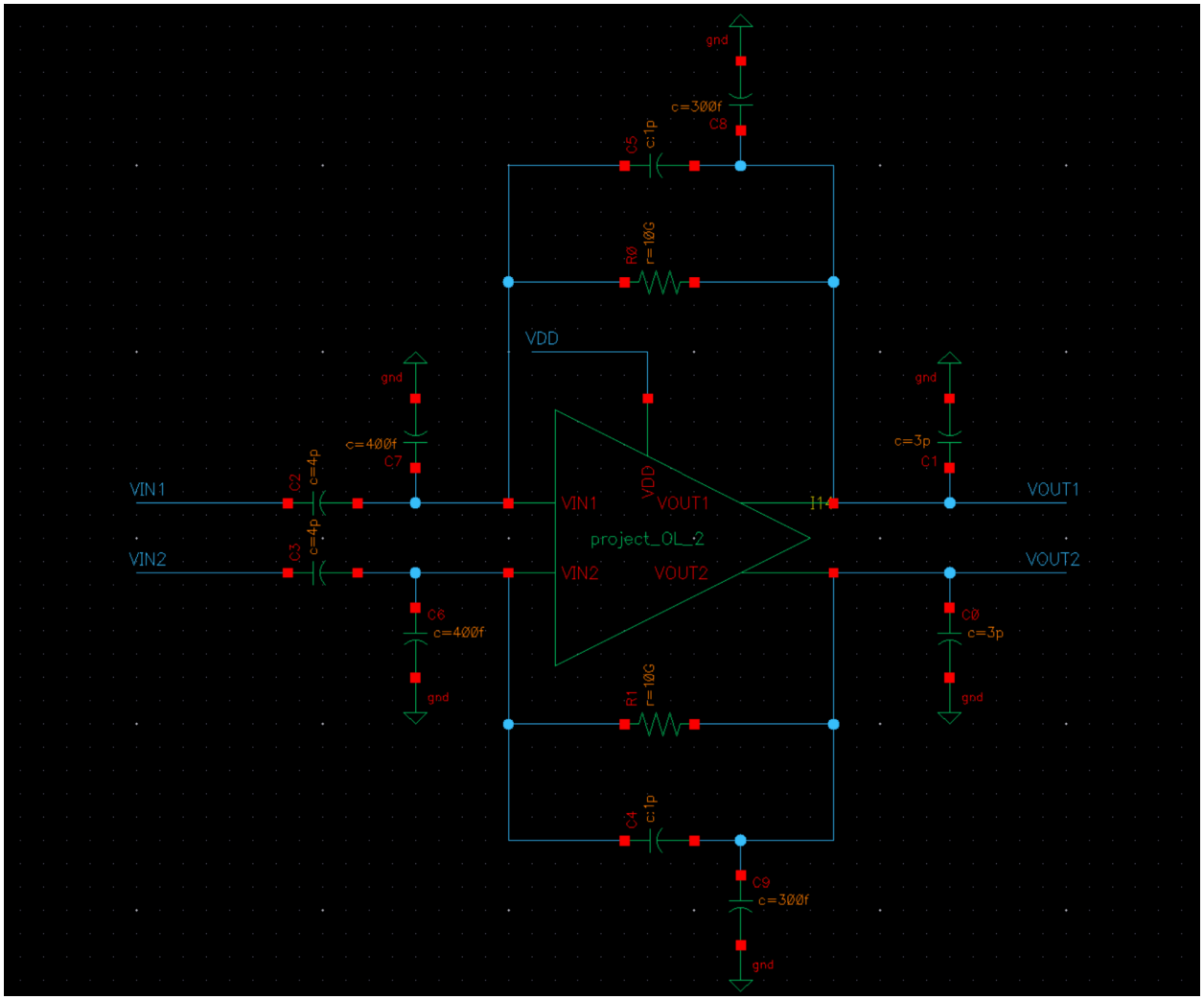
Total resistance: 10.74k+17.69k+21.07k+36.22k+14.28k = 100k ohms (within resistor budget)

Table of bias values:

1	VB4	670m
2	VB3	359.1m
3	VB2	1.27
4	VB1	800m

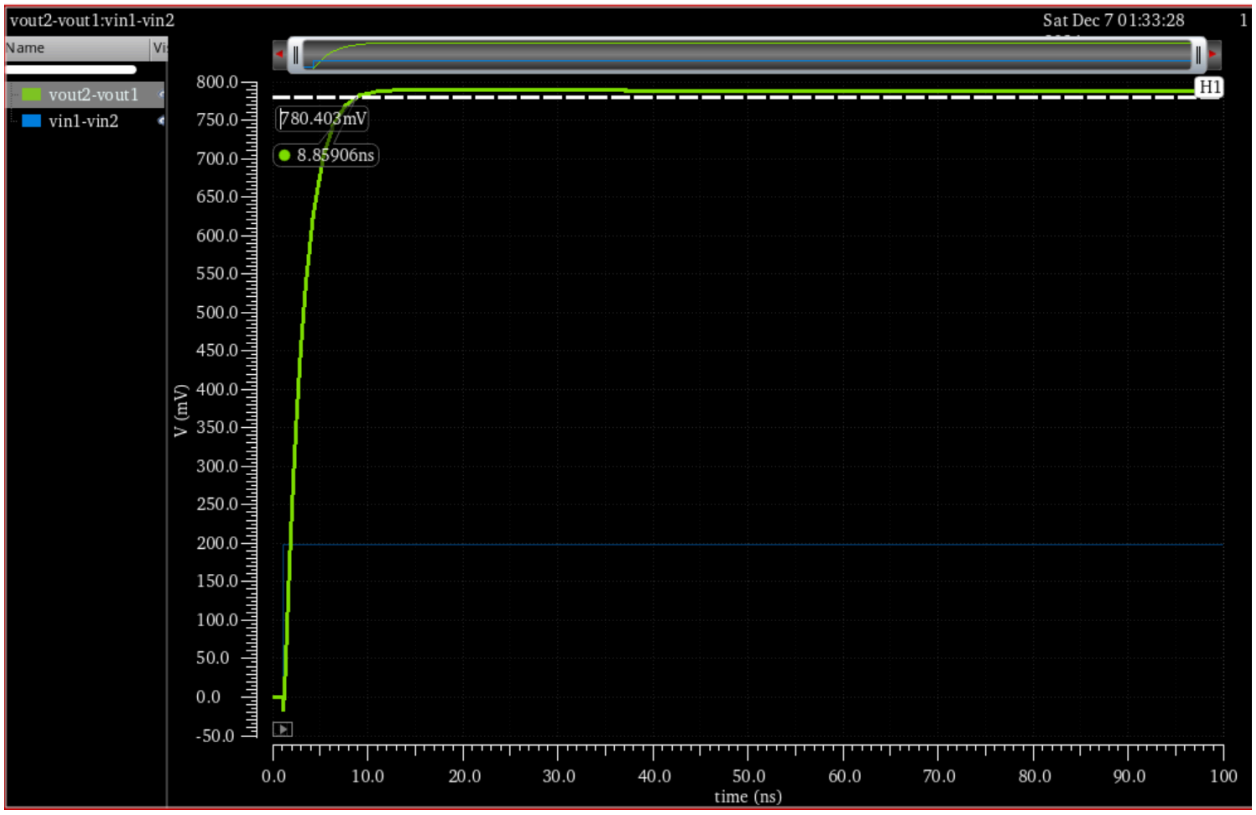
The closed loop design involves adding resistors and capacitors in feedback to set input and output common mode and reduce the gain of the op amp to 4. The resistors were chosen to be 10G ohms so that they act as ideal as possible in terms of setting the common mode of the input and output together.

The capacitors must have a ratio of 4 to 1 in order to get a closed loop gain of 4, so the capacitor values were chosen to be 4pF and 1pF, which are the smallest possible capacitance values that could be used before the circuit starts exhibiting unwanted behavior. Due to parasitic effects, shunt capacitors were also added after the feedback capacitors to model the parasitics. The full closed loop design is below.



The entire circuit draws 8.329mA of current, meaning that the total power consumption is:
P = I * VDD = 8.329mA * 1.8V = 14.99mW < 15mW (within power budget)

With this closed loop design, the setting time of the opamp when a 200mV differential input step is applied is shown below.



Steady state value: 788.286mV
1% error above: 788.286*1.01 = 796.16886mV
1% error below: 788.286*0.99 =780.40314mV
Peak value: 789.696mV
Settling time (accounting for 1ns input delay): 8.95906 - 1 = **7.95906ns**

Gain: 788.286/200 = 3.94143
Gain error: (4-3.94143)/4 * 100% = **1.46425%** error < 2% error (within error spec)

In conclusion, the op amp has a minimum settling time of 7.95906ns with a power budget of 15mW, with a gain error of 1.46425% for the target closed loop gain of 4.