Dynamic Design Analysis

# ECU 1: -

* State Machine Design for ECU 1:

Diagram

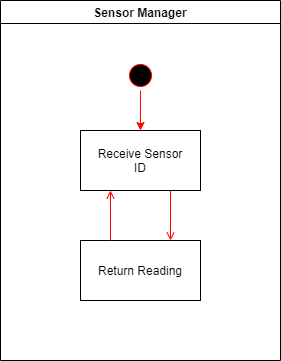
Description automatically generated

Diagram

Description automatically generated

Diagram

Description automatically generatedDiagram

Description automatically generatedDiagram

Description automatically generated

Diagram

Description automatically generatedDiagram

Description automatically generated

Diagram

Description automatically generated

* Sequence Diagram of ECU 1: -

Diagram

Description automatically generated

Diagram

Description automatically generatedDiagram

Description automatically generated

* Diagram

  Description automatically generatedCPU Load for ECU 1: -

We have three tasks: (Assume Execution Time)

T1: {Periodicity: 10ms, Execution Timer: 1ms}

T2: {Periodicity: 5ms, Execution Timer: 1ms}

T3: {Periodicity: 20ms, Execution Timer: 1ms}

Hyperperiod = 20 ms

CPU Load = Ʃ E/H = ((1\*2+1\*4+1\*1) /20)\*100 = 35%

# ECU 2: -

* State Machine Design for ECU 2:

Diagram

Description automatically generatedDiagram

Description automatically generated

Diagram

Description automatically generated

Diagram, schematic

Description automatically generated

Diagram, schematic

Description automatically generated

Diagram

Description automatically generated

* Diagram

  Description automatically generated with low confidenceSequence Diagram of ECU 2:
* CPU Load for ECU 2:

We have just one task: (Assume Execution Time)

T1: {Periodicity: 5ms, Execution Timer: 2ms}

Hyperperiod = 5 ms

CPU Load = Ʃ E/H = (2 /5) \*100 = 40%

* CAN Bus Load

1 CAN frame contains around 125 bits.

Assume we are using a 500 kb/s bit rate:

⸫ Bit time = 1 / bit rate => 1 / (500 \* 1000) = 2µs.

This means 1 bit will take 2µs to transfer on the bus.

The approximate time to transfer one frame is 250µs.

The total number of frames = 350 frames every 1000ms.

Bus Load = (((350\*250)/(1000\*100))/100) = 8.75%