

Digital Design and Computer Architecture LU

# Lab Protocol

## Exercise III

Group 6

Thomas Scharinger, Matr. Nr. 11777710

e11777710@student.tuwien.ac.at

Fabian Philipp Posch, Matr. Nr. 01456625

e01456625@student.tuwien.ac.at

Maximilian Engl, Matr. Nr. 11775811

e11775811@student.tuwien.ac.at

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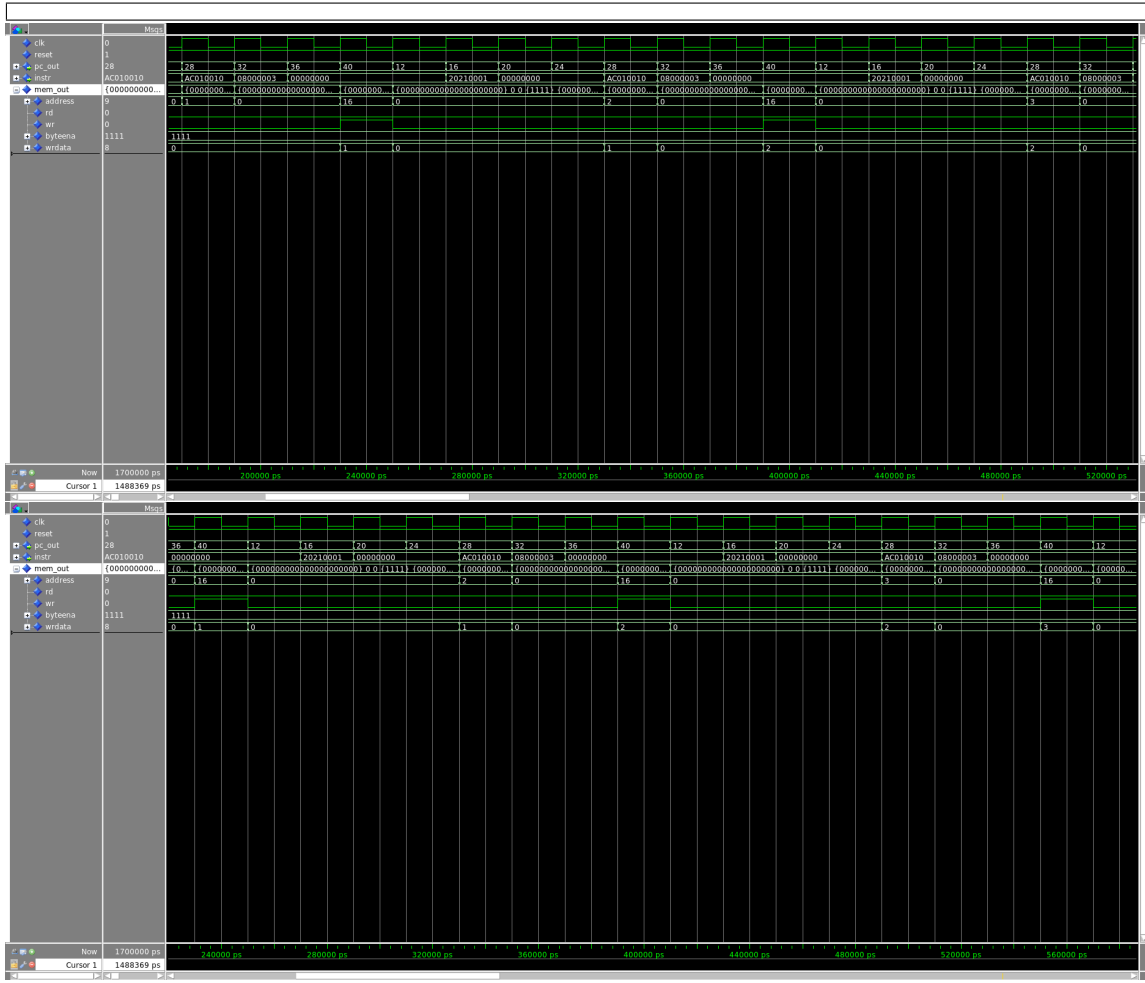


Figure 1: Simulation screenshot for Listing 1.

Make sure the following signals are visible in Figure 1 and the signal values are readable: the program counter in the fetch stage, the instruction being fetched, and the fields address, rd, wr, byteena, and wrdata in the mem\_out signal coming out of the pipeline.

Listing 1: Assembler example without forwarding

```
addi $1, $0, 0
nop
nop
loop:
    addi $1, $1, 1
    nop
    nop
    sw $1, 16($0)
    j loop
    nop
    nop
    nop
```