Digital Design and Computer Architecture LU

Lab Protocol

Exercise IV

Group 6

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Forwarding Simulation

Figure 1: Simulation screenshot for Listing 1.

Make sure that at least the following signals are visible in Figure 1: the program counter in the fetch stage, the instruction being fetched, and the signals `wraddr`, `wrdata`, and `regwrite` of the register file.

Listing 1: Assembler example with forwarding

```
addi $1, $0, 7
addi $2, $0, 5
and $1, $2, $1
nop
nop
```

Branch Hazards Simulation

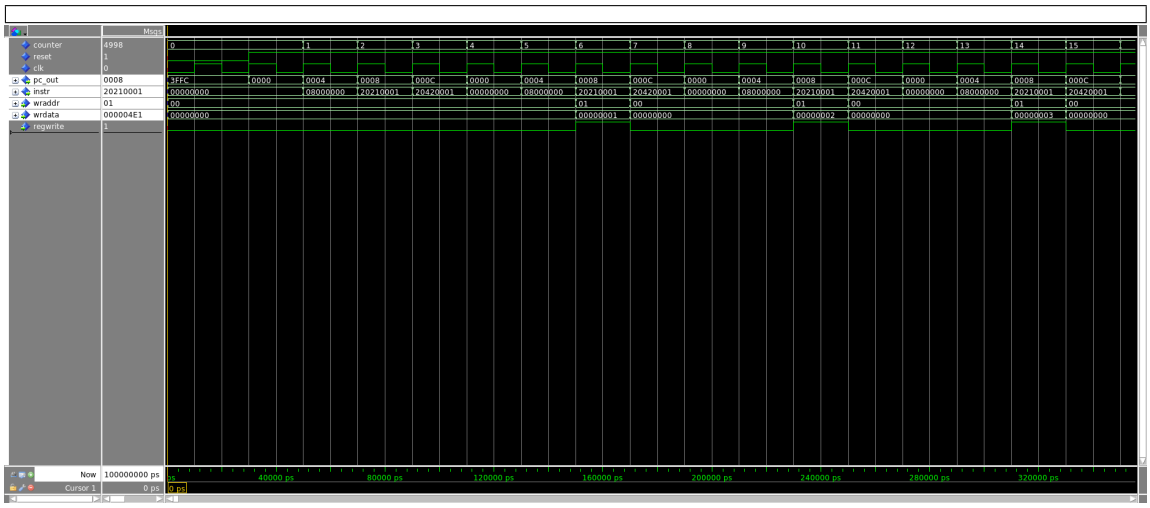

Figure 2: Simulation screenshot for Listing 2.

Make sure that at least the following signals are visible in Figure 2: the program counter in the fetch stage, the instruction being fetched, and the signals `wraddr`, `wrdata`, and `regwrite` of the register file.

Listing 2: Assembler example with branch delay slot

```
loop:   j loop
        addi $1, $1, 1
        addi $2, $2, 1
        nop
```

Synthesis Results

Table 1: Resource usage by entity, including resources used by sub-entities.

	LC Combinationals	LC Registers	Memory Bits
Fetch Stage	61	14	131072
Decode Stage	1659	1080	0
– Register File	1085	1034	0
Execute Stage	1206	172	0
– ALU	444	0	0
Memory Stage	186	115	0
– Jump Unit	4	0	0
– Memory Unit	59	0	0
Write-Back Stage	110	38	0
Forwarding Unit	20	0	0
Control Unit	301	225	0
Sum	3325	1644	131072

Question: What is the maximum frequency of your design?

Answer: 86.89 MHz

Question: Where is the critical path of your design?

Answer: from regfile: rdaddr2_reg to ctrl: npc

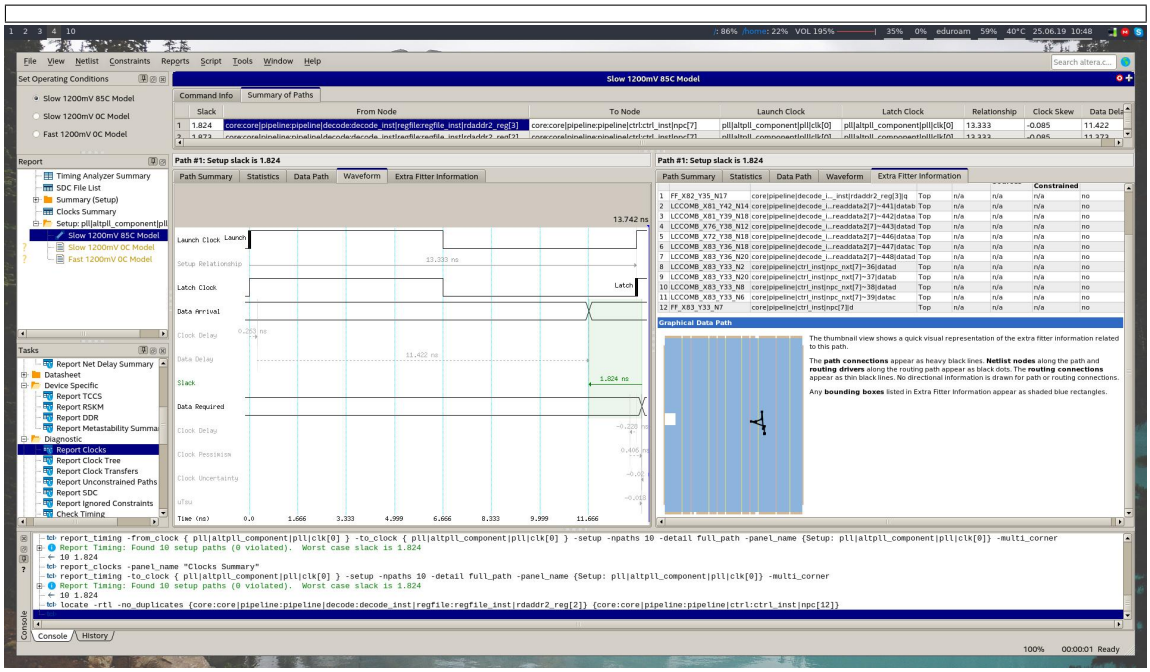

Figure 3: Simulation screenshot for critical path.