Final Lab Project

EE 331 Winter 2015
Prof: Jason Silver
TA: Mark Sugiyama

Jonathan Tompkins, 1227229
Sui Pang, 1361789
Eeshan Londhe, 1227852
Matthew Dentinger, 1167678
Shruti Misra, 1237749

1. Introduction

The purpose for this lab project was to design and build an adjustable AC to DC converter. The lab was broken down into five distinct stages. Overall we were to take an input AC voltage from a lab transformer and through our circuit output a constant DC voltage. This DC voltage signal had to be within 10V to 20V and the magnitude should be adjustable by a single potentiometer. The stages are named as follows, full-wave bridge rectifier, voltage divider, 555 timer, voltage boost, and regulator.

2. Purpose

The first stage was our full-wave bridge rectifier. Here we took a lab transformer as our AC input voltage and put this signal through the full-wave bridge rectifier to output a constant DC voltage of 10 V. We completed this rectifier using four diodes which feeds into two resistors in parallel with an output capacitor. The output capacitor creates the DC voltage used throughout the rest of the circuit. This DC voltage was sent into two of the other stages used in our overall circuit, the voltage divider and voltage boost.

The second stage of our circuit is a voltage divider built simply from two resistors. The input to the voltage divider is the DC voltage received from the rectifier. This voltage divider sends an output voltage of less than 8V to our 555 timer stage.

The third stage of our AC to DC converter was our voltage booster. In this voltage boost stage we received two signals, one from the 555 timer and the other from our full-wave bridge rectifier. This stage we were able to take the input DC voltage from the rectifier and boost it between 10V to 33 V. We were able to achieve this boost through the use of a transistor switched inductor and a catch diode. This is all fed into an output capacitor that ultimately is the output voltage used. This boost stage sent an output voltage to our last stage of the circuit, the regulator.

In the final stage of our circuit we sent our boosted DC voltage to the regulator. Here we had to limit the max output voltage to 20V. In order to achieve this desired output we used two zener diodes to limit the output voltage to 20V. Due to our previous stages designs we were not concerned with having a voltage less than 10V because our voltage boost always outputted at least 10V

3. Circuit Diagrams and Specifications

Hand Drawn Schematic: Figure 1 shows the hand drawn circuit we created in order to build our overall circuit. This includes both the actual circuit diagram and block diagram.

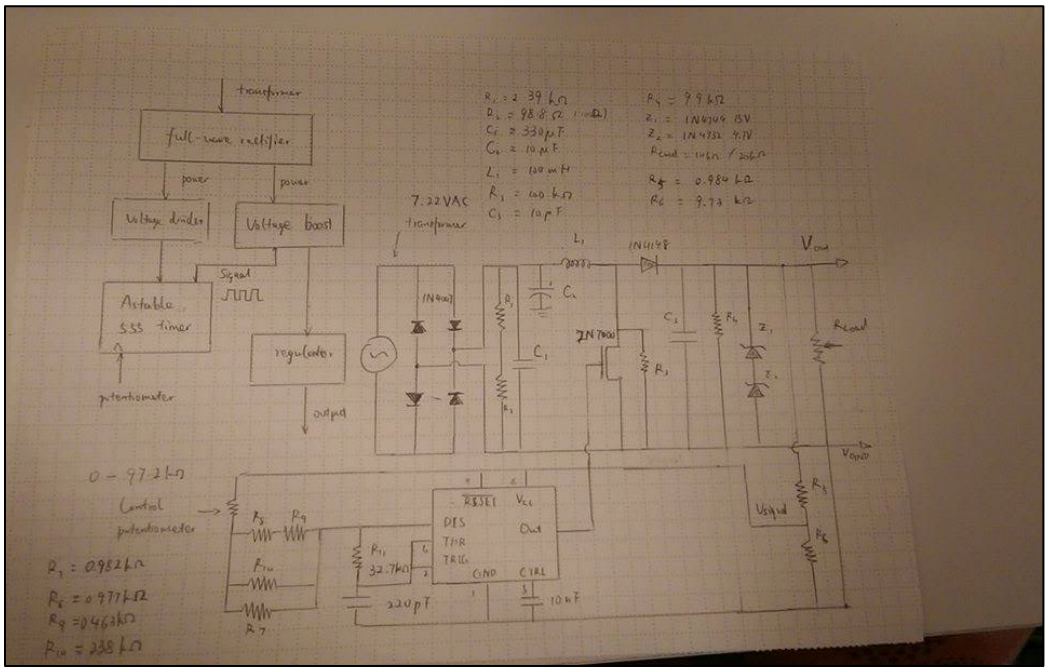


Figure 1: Hand drawn circuit diagram

Block Diagram: Figure 2 is a more detailed version of our block diagram.

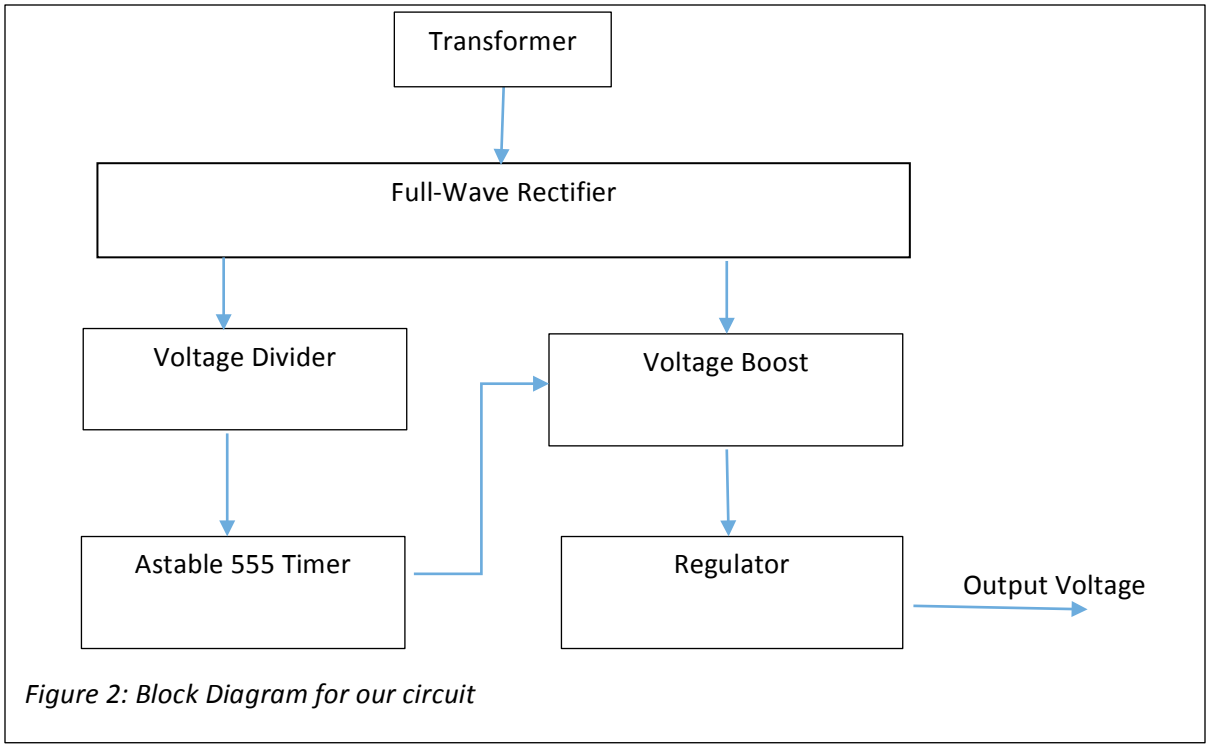


Figure 2: Block Diagram for our circuit

Full-Wave Rectifier: Figure 3 shows the circuit diagram for our full-wave rectifier. D1, D2, D3, and D4 are all 1N4007G diodes. The DC output voltage is stored along C1.

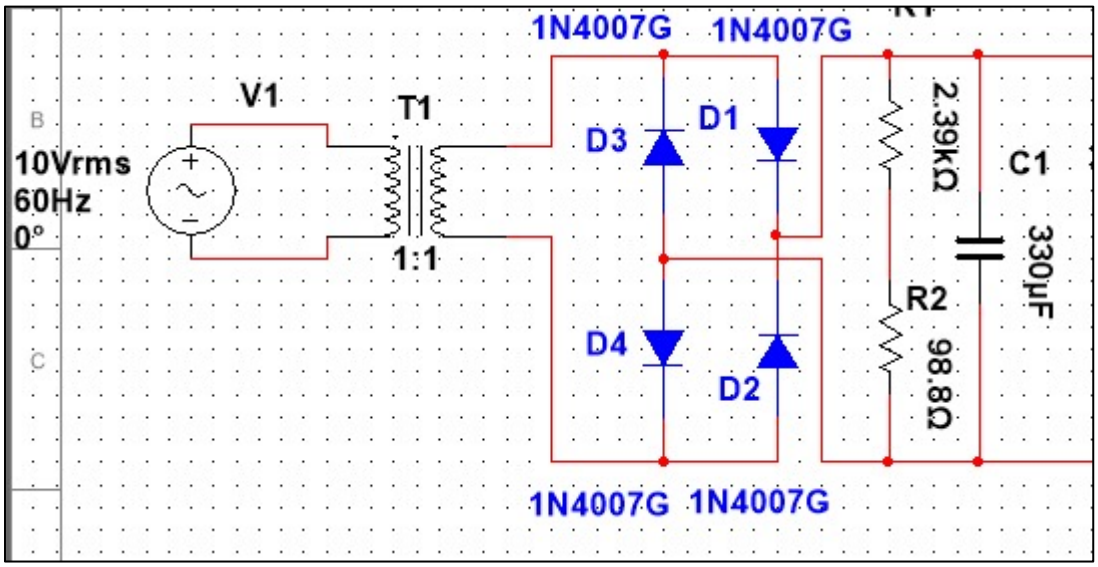


Figure 3: Circuit diagram for our full-wave rectifier

Voltage Boost: Figure 4 below is our voltage boost circuit. The input to the 2N7000 transistor is the output voltage from our 555 timer and voltage divider section. This has an output voltage along R4 that is sent to our regulator.

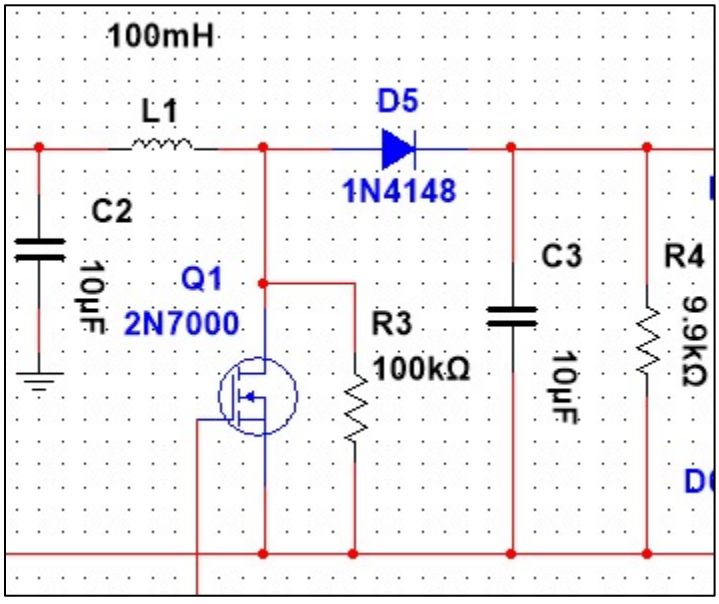


Figure 4: Our voltage boots circuit.

Voltage Divider/555 Timer: Figure 5 contains both the voltage divider and 555 timer. The voltage divider consisting of R7, R9, R8, R12, and R6. This voltage divider outputs a voltage across R6 that is sent to the 555 timer.

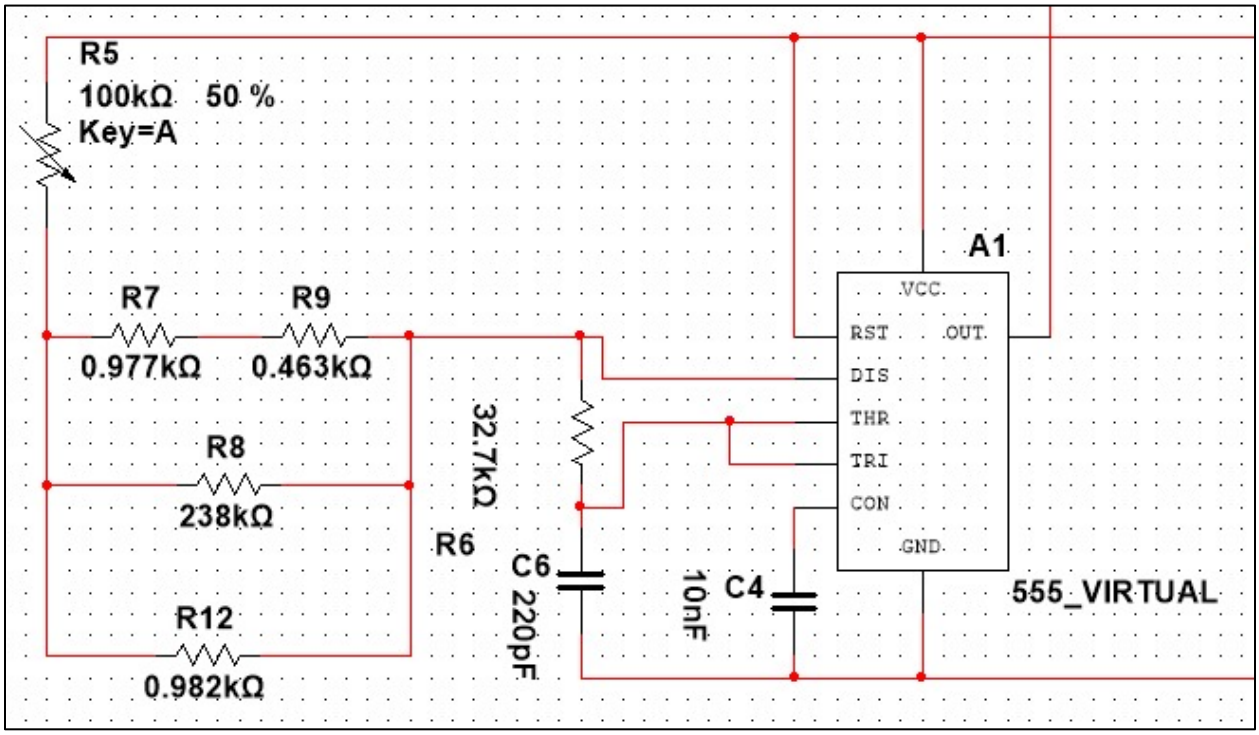
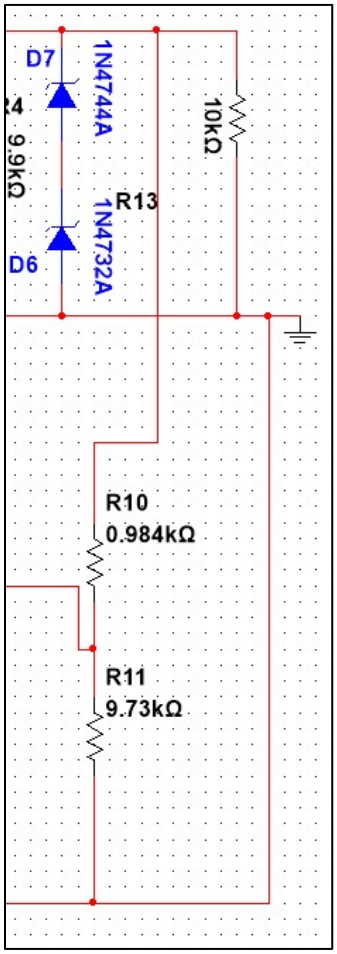


Figure 5: The circuit diagram for our voltage divider and 555 timer

Voltage Regulator: Figure 6 shows our circuits voltage regulator which limited our output voltage to 19.3V.



4. Circuit PSpice Simulation

Parameter	Design Specification	PSpice Simulation
Rectifier Voltage:		
	Full-Wave Bridge	7.417 V
Output:		
	Output voltage w/open circuit	19.719 V
	Output voltage w/10k Load	19.719 V
	Output voltage w/20k Load	19.719 V

5. Demonstration Results

Laboratory Final Design Project

AC to DC Voltage Amplifying Converter

Instructor: Jason Silver

VERIFICATION OF DESIGN TEST RESULTS:

Group Members:	Date Tested:
	TA:

Parameter	Design Specification	Test Results	Points
Input Voltage	±7.5 VAC lab transformer (Yes/No)	7.23 V	/3
Output	Low Voltage Limit =		
	Output voltage w/ open circuit	10.30 V	/3
	Output voltage w/ 10 kΩ load	10.03 V	/3
	Ripple voltage w/ open circuit	62.23 mV	/3
	Ripple voltage w/ 10 kΩ load	88.53 mV	/3
	High Voltage Limit =		
	Output voltage w/ open circuit	19.35 V	/3
	Output voltage w/ 20 kΩ load	19.35 V	/3
	Ripple voltage w/ open circuit	45.25 mV	/3
	Ripple voltage w/ 20 kΩ load	46.39 mV	/3
Voltage Adjust	Single Potentiometer (Yes/No)	YES	/3
Rectifier/Filter	Full –wave, half-wave	Full wave bridge, 7.96V	/5
	Ripple voltage on filter cap	0.28 V	/5
Topology	Boost converter (Yes/No)	YES	/5
Oscillator	Frequency of 10 kHz to 100 kHz	38.4 kHz - 99.1 kHz	/5
Extra Credit			/10
Design Documents			/50
Total Score	**100+10 points max.**		**/100**

6. Conclusion

During this lab we encountered many challenges that we did not expect. When initially designing our circuit our first mock schematic mirrored the circuit diagrams of previous labs. We learned quickly that certain aspects of each lab design needed to be finely tuned not only for each stage of the AC to DC converter, but overall in relation to the entire circuit. This project took a significant amount of both precise calculation and reasoning, balanced with some trial and error. Each individual stage was not difficult to build on their own, but when connecting all of the stages together it was sometimes difficult to reach our desired output. The debugging process was the most challenging part of our lab, for example when building our rectifier we accidently connected our oscilloscope ground to two different parts of the circuit. This lead to major shortages and we ended up blowing three capacitors until we realized our mistake. Designing and building this AC to DC converter circuit was a difficult process, but overall our lab group worked together to overcome all obstacles.