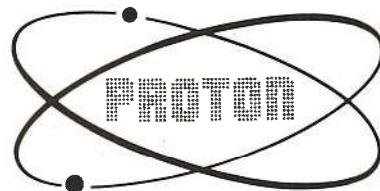
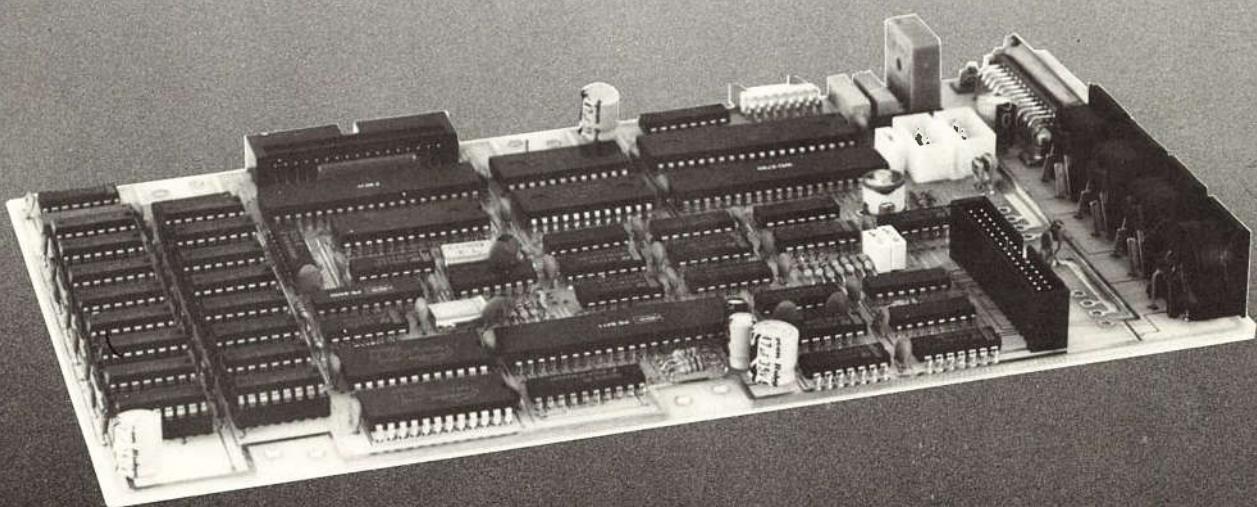
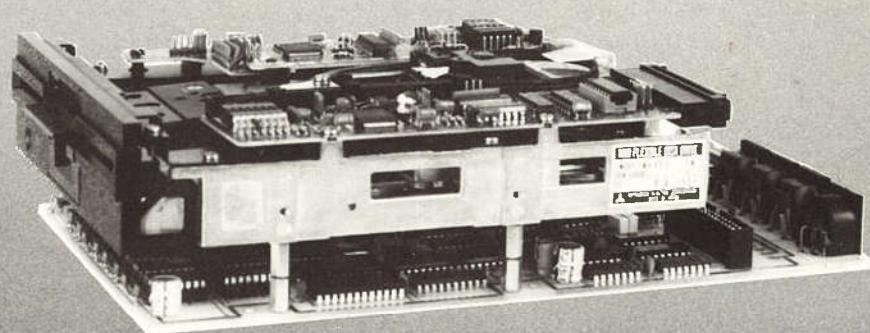


PROTON Electronics
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Telex 73415 pe nl

SERVICE MANUAL



COMPACTBOARD 80



COMPACTBOARD 80 tm

SERVICE MANUAL

Initial Hardware Version

(PE 226)

Note PE 226-1 !

PROTON ELECTRONICS
Energiestraat 36
1411 AT NAARDEN
The NETHERLANDS

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- 3 Memory and I/O addresses
 - 3.1 Memory map and Soft switching
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- 4 Processor operation
 - 4.1 Processor & TCU
 - 4.2 Timing diagrams
- 5 Video Circuit
- 6 Component selection
- 7 Test procedures
 - 7.1 Functional testing
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CHAPTER 1 Introduction

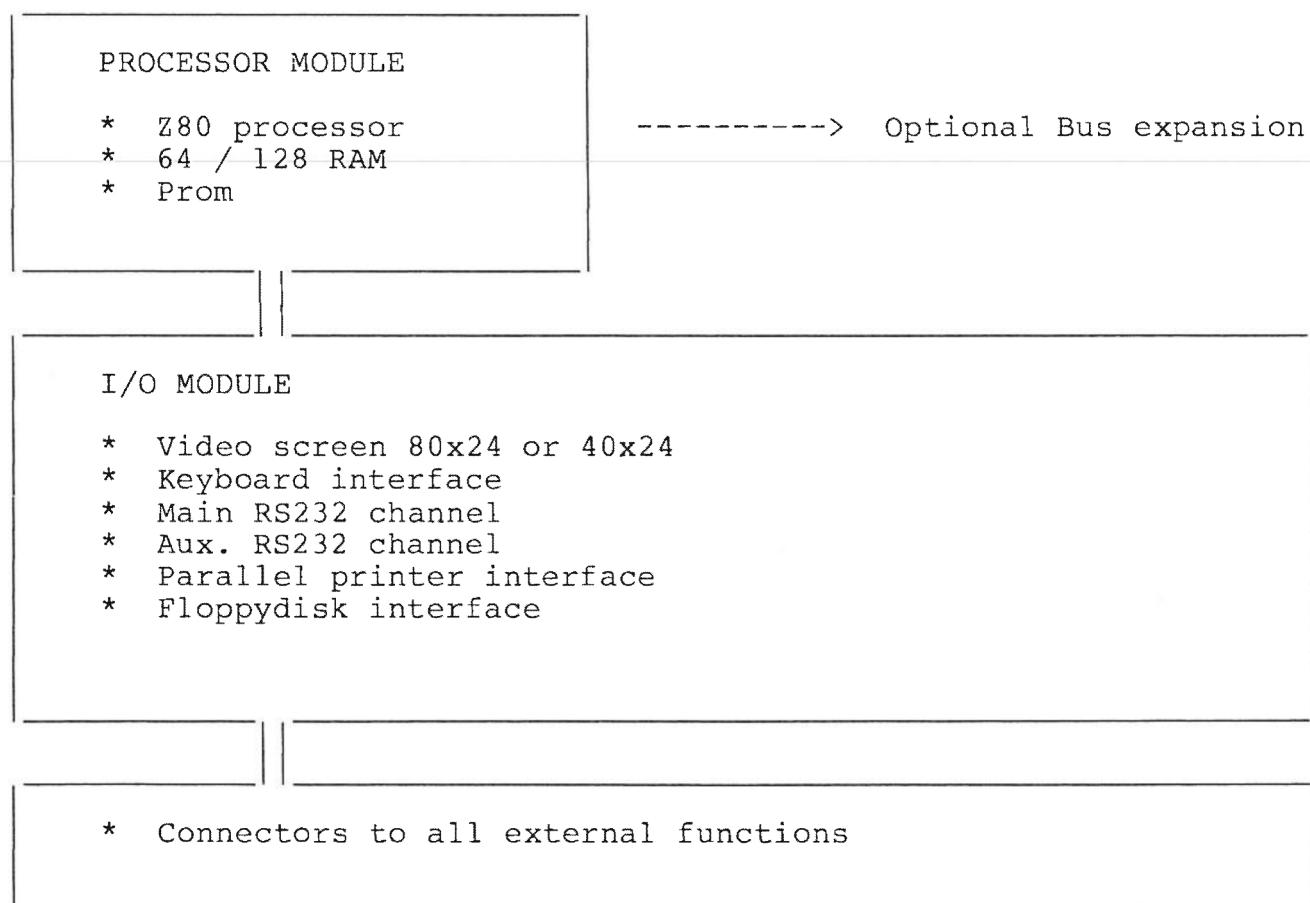
This Manual is a supplement to the Compactboard 80 Documentation. Its goal is to provide an OEM-user with in-depth information about the technical aspects of the Compactboard 80. Together with this manual a diskette with a qualitative test program is supplied. This program facilitates the evaluation of functional correctness of a system and its keyboard, disk(s) and printer.

Functions that are not performed in hardware but in software are normally supported by a BIOS call, the description of their exact operation is the ommitted from this manual.

CHAPTER 2 General hardware structure

The hardware of the compactboard 80 can be divided in two major sections. One section consists of the microprocessor (Z80), RAM and bank-switch logic and the (E)prom. The other section contains all I/O related logic. By nature all I/O logic is connected to the address and databusses. Future expansion therefore, can be added to the compactboard via the busconnector.

A block-diagram of the board is given. The module names will be referred to in the manual.

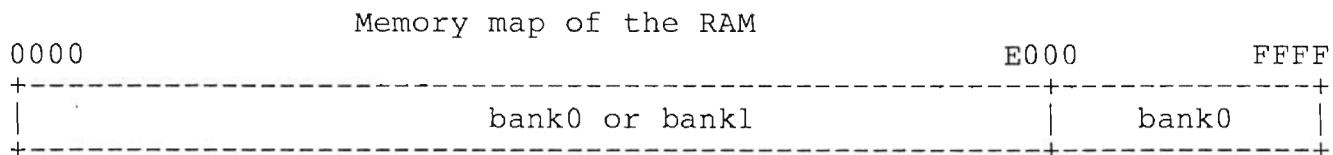


CHAPTER 3 Memory and I/O addresses

3.1 Memory map and Soft switching

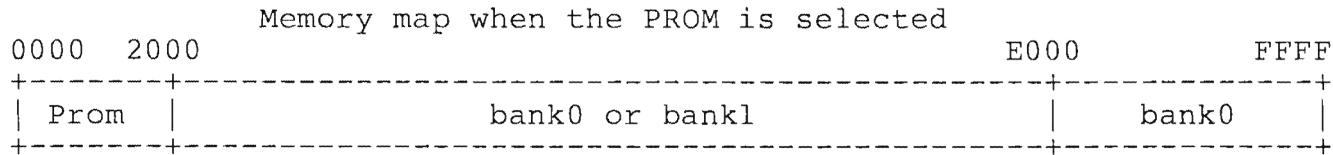
3.1.1 RAM addresses

The Compactboard 80 has an full 64 K (from 0000-FFFF) address space available for transient programs (RAM). For 128 K models a bankswitching is provided. This mechanism replaces the Bank0 ram addresses 0000-DFFF by the ram of Bank1. This method provides a 'common' area of ram (E000-FFFF) which is NOT affected by the bankswitch logic.



3.1.2 PROM addresses

To provide for a 'power-on' program (normally a bootstrap loader) an (E)prom (2732 or 2764) is active from address 0000-1FFF. The prom can be deactivated to supply the full 64 K for RAM use.
See for bankswitching BIOS functions (chapter 6).

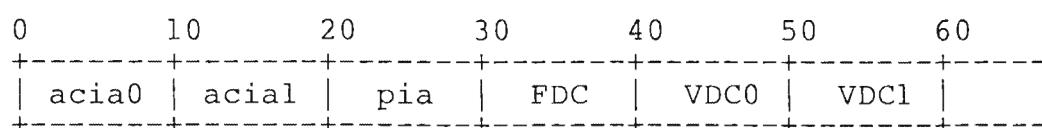


3.2 I/O map

All I/O-devices have read and write registers, so the address map of the input-ports and the address map of the output ports are exactly the same. The following I/O-address table gives the portnumbers of the devices:

device	Output register	Input register	port address (hex)
ACIA 0	Control	Status	00
	Transmit Data	Receive Data	01
ACIA 1	Control	Status	10
	Transmit Data	Receive Data	11
PIA	Data A	Data A	20
	Control A	Control A	21
	Data B	Data B	22
	Control B	Control B	23
FDC	Commands	Status	30
	Track number	Track number	31
	Sector number	Sector number	32
	Data	Data	34
VDCa	Reg0	Reg	40
VDCd	Reg1	Data	50

I/O-map:



3.3 Soft switches

The Compactboard 80 has a number of hardware features that can be controlled by software. The functions are Bank select, Prom enable and floppy disk control.

The functions are controlled by the PIA A-port. The following table shows the bit number and its function.

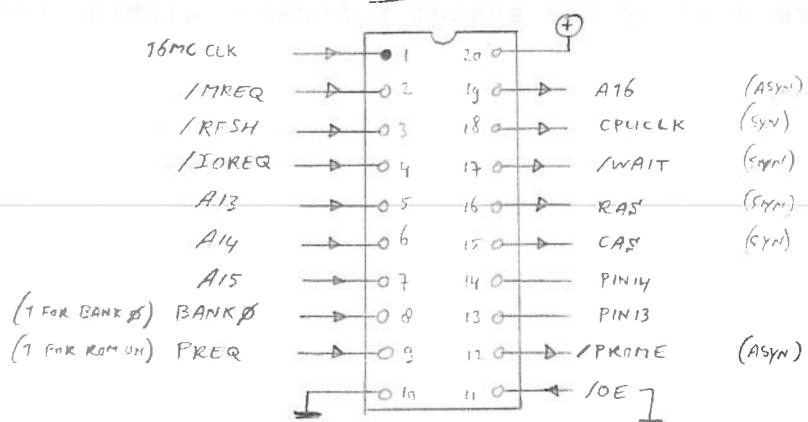
PIA port A (address 20 hex)

bit 0	Drive select 2 ⁰
bit 1	Drive select 2 ¹
bit 2	Drive Side select
bit 3	Enable write precompensation
bit 4	Enable Single density / Buzzer drive
bit 5	Printer BUSY input
bit 6	Memory bank 0 enable
bit 7	Prom enable
CA2	Enable 8" drives
CA1	75 Hz input for realtime clock

All signals names are given in active high logic.

Bits 0,1,2,3,4 and CA2 are used by the system software within the Combidos BIOS.

TCU80



16 [R] 6
X

CHAPTER 4 Processor operation

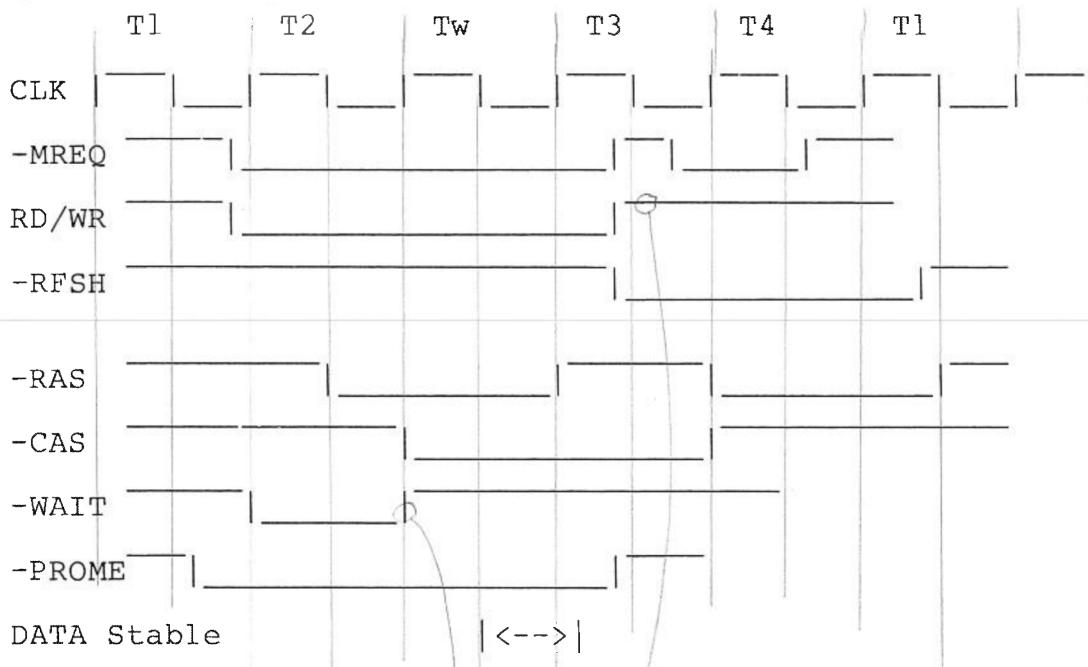
4.1 Processor & TCU

The processor module is build around a Z80 processor, a timing control unit (TCU) 64 or 128 K RAM and the (E)prom. We will describe the system operation of the TCU only, operation of other parts can be found in their own documents.

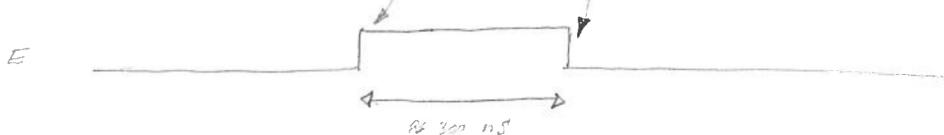
The TCU receives a clocksignal from XT1 (in 6MHz systems from XT2) which is twice the system clock. The TCU divides this signal to obtain the system clock. The -MREQ, -IOREQ, and -RFSH (signals from the processor) are fed into the TCU. From this signals the TCU generates the correct RAS/CAS timing for the DRAM's. The TCU inserts one extra WAIT-cycle in memory and I/O-cycles to provide an optimum device timing.

A separate function of the TCU is the Bank-switch controlling of the RAM Banks and the (E)prom.

4.2 Timing diagrams



Note: For 8 Mhz one clock-cycle is 125 nS.
For 6 MHz one clock-cycle is 166 nS.



CHAPTER 5 Video Circuit

The Compactboard contains the PE8411 video controller chip. This chip was designed for the PROTON Videoterminal chipset that consists of a dedicated standard-cell 8-bit microprocessor (PE8410) and a special high-speed Video Display Processor (PE8411). This combination results in a very low-cost terminal system.

The use of this chip in the Compactboard brings all the features of the terminal chip set to the Compactboard. A description of the chip is given below.

5.1 The video controller

PIN ASSIGNMENT

Vss	1		40	VA0
VOE	2		39	VA1
VWE	3		38	VA2
VAS	4		37	VA3
SYNC	5		36	VA4
	6		35	VA5
BLUE	7		34	VA6
GREEN	8		33	VA7
RED	9		32	VA8
	10	PE	31	VA9
	11	8411	30	VA10
Vclk	12		29	VA11
SynIn	13		28	VA12
ALE	14		27	VA13
EN	15		26	CE
WE	16		25	AD7
ADO	17		24	AD6
AD1	18		23	AD5
AD2	19		22	AD4
Vcc	20		21	AD3

The VDP is a special high-speed videoprocessor in NMOS technology. The circuit contains 5 main blocks:

- Processor DMA interface.
- Command-processor.
- Video-memory interface.
- Video-attribute controller.
- Character-generator (128 char in a 6 x 10 matrix)

The VDP is closely coupled to the Z80 and its firmware to obtain optimal performance and to utilize all features of the VDP.

The VDP is connected to 4 K byte of RAM. This Ram is used to store the characters, attributes and the characters of the line.

Pin description VDP

Vss	1	circuit 0 Volt level.
VOE	2	Output enable of the video-RAM (active low)
VWE	3	Write-control of the video-RAM (active low)
VAS	4	Address-strobe of the video-RAM. The low-byte of the video-address is present at VA0-VA7 on the falling edge of VAS.
Sync	5	TTL-compatible output with the composite sync of the videosignal. The sync-pulses are negative and support egalisation during vertical sync.
BLUE	7	TTL-compatible output of the blue video signal.
GREEN	8	TTL-compatible output of the green video signal.
RED	9	TTL-compatible output of the red video signal.
Vclk	12	TTL-compatible input for the 12Mc video dot-clock.
SynIn	13	TTL-compatible input for external synchronisation
ALE	14	Address latch input.
EN	15	Data transfer clock (active high input).
WE	16	Data transfer direction input.
ADO	17-19,	
-AD7	21-25	Multiplexed data/address lines (D0-D7 & A0-A7).
VA0		
-VA13	40-27	Address lines 0 to 13 for the videomemory. VA0-VA7 are time-multiplexed for data (D0-D7) and address (A0-A7) of the video-ram.
-CE	26	General chipselect (active low).

5.2 External video synchronisation

The PE8411 allows synchronisation to an external video signal by synchronising the Vclk (12Mhz). The Vclk must be generated with a VCO (voltage controlled oscillator) which is controlled by a phase comparator. The PE8411 has an internal phase comparator (output on pin 6) which compares the external sync (on pin 13) to the internally generated sync. The internal phase comparator is a digital comparator. In applications where a very smooth line synchronisation is required, an external phase comparator must be used.

CHAPTER 6 Component selection

The timing of the Compactboard 80 is chosen as loosely as possible to allow component variation. On selecting components however, one must verify that these components fall completely within specification of the compactboard timing. The selection of Dynamic Rams is made easy with the use of the following requirement table.

DRAM maximum allowed times:

READ/WRITE/REFRESH cycle

	at 6 MHz	at 8 MHz	unit
RAS access time	225	160	nS
CAS access time	140	100	nS
RAS hold after CAS	166	125	nS
RAS precharge time	165	125	nS
RAS pulse	250	210	nS

The DRAM's must have 128 refresh cycles and ~~do not need~~ automatic or self-refresh at pin 1 (pin 1 is not connected). *MUST not have*

The timing for the 68xx devices is realised by IC 31 which generates the 'E' signal. The E signal allows sufficient data and address settle time for 68Bxx components (B stands for 2Mhz version).

The timing for the ram of the video controller (IC 48 en 49) is important on the following points:

Cycle time : 450 nS
Read Access : 260 nS
Write pulse width : 100 nS

CHAPTER 7 Test procedures

7.1 Functional testing

To perform a functional test, use the separately supplied test monitor prom. This prom holds the standard Compactboard resident monitor and a test program for:

- Serial port loop-back test (ACIA 0 & 1)
- Parallel line test (printer & floppy lines)
- Ram refresh & access time test.

The tests will start directly after reset. Errors are reported in inversed video and indicate also where errors are detected. To operate these tests, a external circuit is needed. This is connected to the connectors K9 (Floppy disk), K4 (Keyboard), K6 (RS232), K7 (Aux, RS232) and K8 (Printer interface). The video monitor is connected as usual. The schematic diagram of the external circuit is shown in appendix C.

The ramtest stops after approximately 4 minutes. During this time the floppydisk controller adjustments can be done. (See Compactboard manual 'Adjustment').

After this, a floppy disk drive must be connected and the operating system can be read from disk by typing 'A' (boot from drive A).

Now perform the quality tests as described below.

7.2 Quality testing

The program supplied on the is designed to test the Compactboard-80 for functional correctness. The program is called 'CBTEST'. The program is, like all Combidos utilities, fully menu driven. The top of the screen holds a command line on which the test procedures available are listed.

The command line shows:

Test : R)am, K)eyboard, D)isk, P)rinter ctrl/C|<ret>|Q|X to Quit

Testing RAM

The Ram test is started by typing R. The tester will check if the Compactboard holds 64 or 128 K and fill all free memory with 128 byte record. These records contain ramdom data of which a checksum is computed and stored. The tester will sequence through all records, change their contents and recompute the checksum. Errors, when found, are reported.

In case of errors, a defect may be in:

- The power supply voltage. It must be 'ripple free'.
- One of the RAM chips (IC 10..25)
- The Z80 (IC 1)
- The random logic of IC 2, 3, 6, 7, 8, 9 or R4, R5, R6, R7, Cl.

The test is terminated by typing any character onto the keyboard.

Testing the keyboard

The keyboard tester is a simple echo program. All keys are echoed to the screen, followed by a space. Control characters like the return are echoed as an `^` followed by the character and a space. If errors occur they are likely to be of the keyboard since it would hardly be possible to start the tester if the keyboard interface of the compactboard would not function. Although random errors may be caused by:

- Improper baud rate of the keyboard,
- Malfunction of the Compactboard baud rate generator (IC 31, 32, 33, 7, 8 or jumper J1),
- Malfunction of the Serial interface chip IC 34, 37, 38.

The Keyboard test is terminated with ctrl/C.

Testing the Disk

The disk test function has several options, it can test:

- a S)ingle track,
- A)ll tracks sequentially,
- R)ead only,
- read and W)rite.

All options are prompted and must be answered with a character. When a single track must be tested, the track number is prompted and the track number range is shown.

When errors occur, they are shown on the right of the screen. Read errors may be caused by:

- Bad diskette media,
- Bad disk drive,
- Incorrect adjustment of the VCO (C3) or RPW (P1)
- Bad interconnection cables/connectors
- Malfunction of random logic (IC 45, 29, 41, R23, C4, RD2)
- Malfunction of the floppy disk controller (IC 27).

Write errors may be caused by:

- Bad disk drive,
- Bad adjustment of the 'write pre-compensation' (P2). Errors caused by incorrect pre-compensation do occur only when precompensation is enabled in the disk parameter block (see DI description in the Combidos manual) and with tracks higher than 1/2 of the maximum number of cylinders of the drive.
- Malfunction of random logic (IC 45, 29, 41).

For adjustment of the Floppydisk controller (VCO, RPW and WPW) see Chapter 6 of the Compactboard 80 documentation.

The test is terminated by typing any character onto the keyboard.

Testing the printer

The printer tester will write a sequence of all ASCII codes to the printer four times. The user should check visually for correctness, since the computer has no feed back from the printer. The printed pattern is:

```
!"#$%&`()*+,-./0123456789:;<=>?  
@ABCDEFGHIJKLMNPQRSTUVWXYZ[\]^_  
'abcdefghijklmnpqrstuvwxyz{|}~'
```

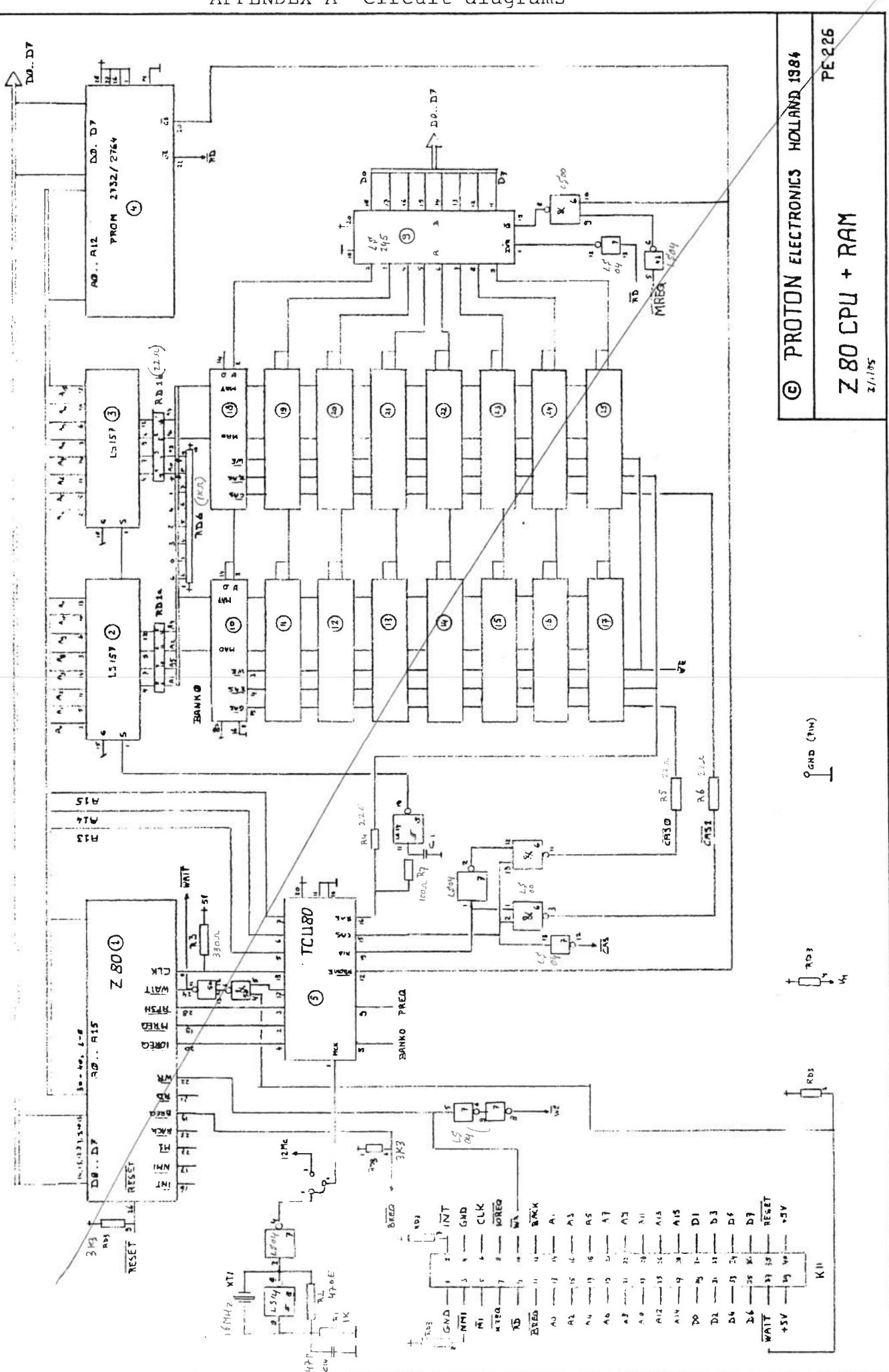
This pattern is printed 4 times.

When the tester 'hangs up', a defect is in the printer, cables or the Compactboard printer interface.

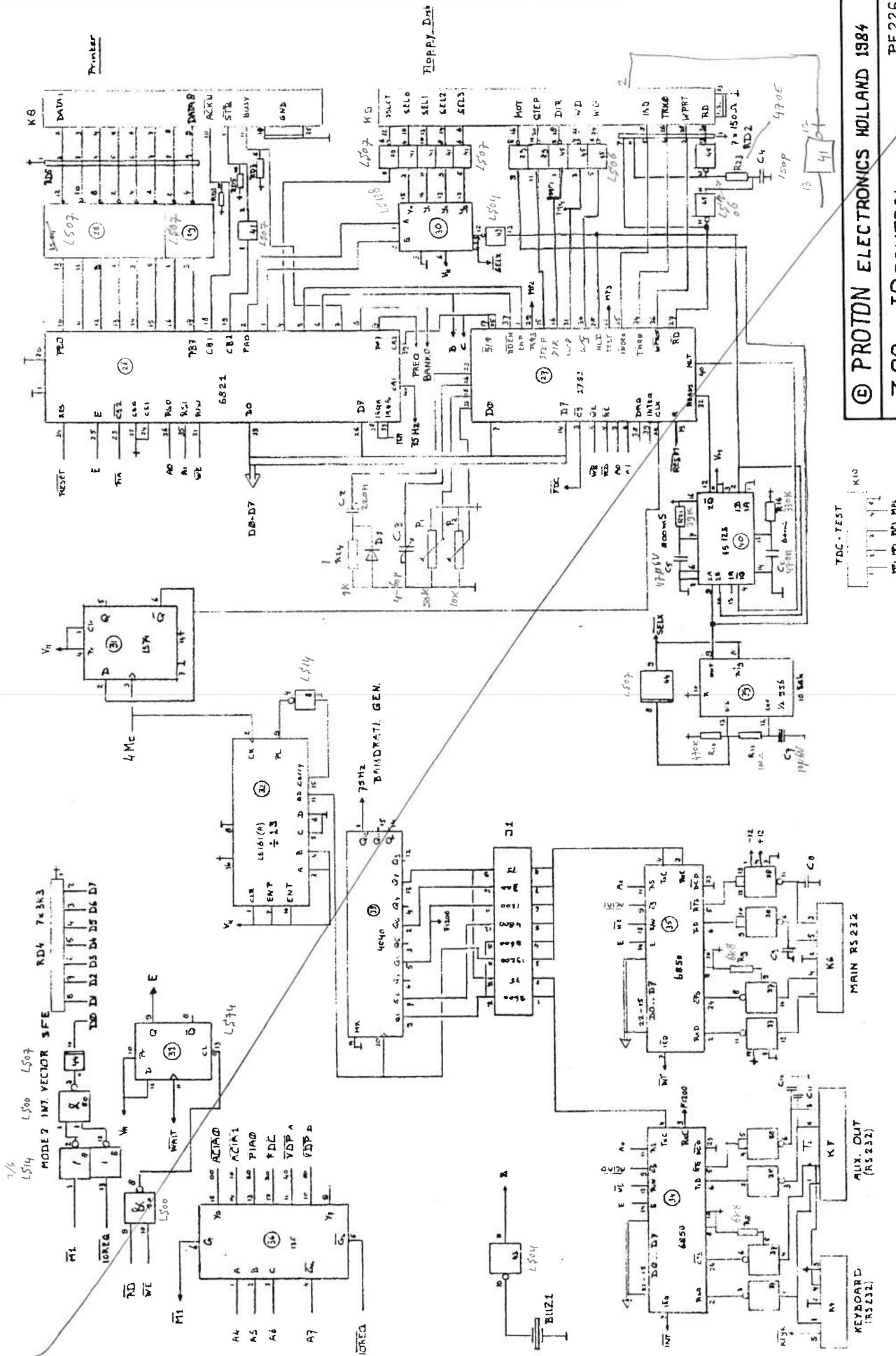
When the printer and the cables have been proved to be ok, the error may be caused by: IC's 28, 29, 41 (interface buffers) and 26 (I/O chip MC68B21).

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APPENDIX A Circuit diagrams



APPENDIX A Circuit diagrams



Service Manual PROTON COMPACTBOARD 80

IC's

=====

1 Z80 B (6Mhz) / H (8MHz)
 2 LS157
 3 LS157
 4 28p socket (2732/2764)
 5 TCU-80
 6 LS00
 7 LS04
 8 LS14
 9 LS245
 10 t/m 17 4164 150 nS Motorola/Nec
 18 t/m 25 4164 (128K version)
 26 MC68B21 (2 MHz)
 27 WD2793 / TMS2793
 28 LS06/16
 29 LS06/16
 30 LS138
 31 LS74
 32 LS161(A)
 33 CD4040
 34 MC68B50 (2 MHz)
 35 MC68B50 (2 MHz)
 36 LS138
 37 XR1489
 38 XR1488
 39 NE556
 40 LS123
 41 LS07/17
 42 LS08
 43 LS04
 44 LS07/17
 45 LS06/16
 46 PE 8411 VDP
 47 LS373
 48 2K x 8 RAM (250ns)
 49 2K x 8 RAM (250ns)
 50 LS00

Decoupling

=====

CO 01 t/m CO 50 10 nF Ker. (29 pcs.)
 CO 51 t/m CO 54 22 uF 6 R
 CO 100 t/m CO 115 100 nF Ker.

Connectors

=====

1 Main power AMP 1-380999-0
 2 Drive A power AMP 350543-1
 3 Drive B power AMP 350543-1
 4 Keyboard DIN 5p
 5 Video DIN 6p
 6 RS232 main DIN 5p
 7 RS232 aux. out DIN 5p
 8 Printer Delta S25
 9 FDC 34p Male recht FC
 10 Test/adjust KK 22-03-1051
 11 Bus exp. 40p Male angle FC
 J1 Baudrate 16 pol. open FC con.

Resistors

=====

1 1 K
 2 470 E
 3 330 E
 4 22 E
 5 22 E
 6 22 E
 7 100 E
 8 6,8 K
 9 6,8 K
 10 470 K
 11 100 E
 12 47 K
 13 100 E
 14 1 K
 15 470 E
 16 330 K
 17 220 E
 18 330 E
 19 120 E
 20 68 E
 21 39 K
 22 --- -
 23 470 E
 24 1 K

Capacitors

=====

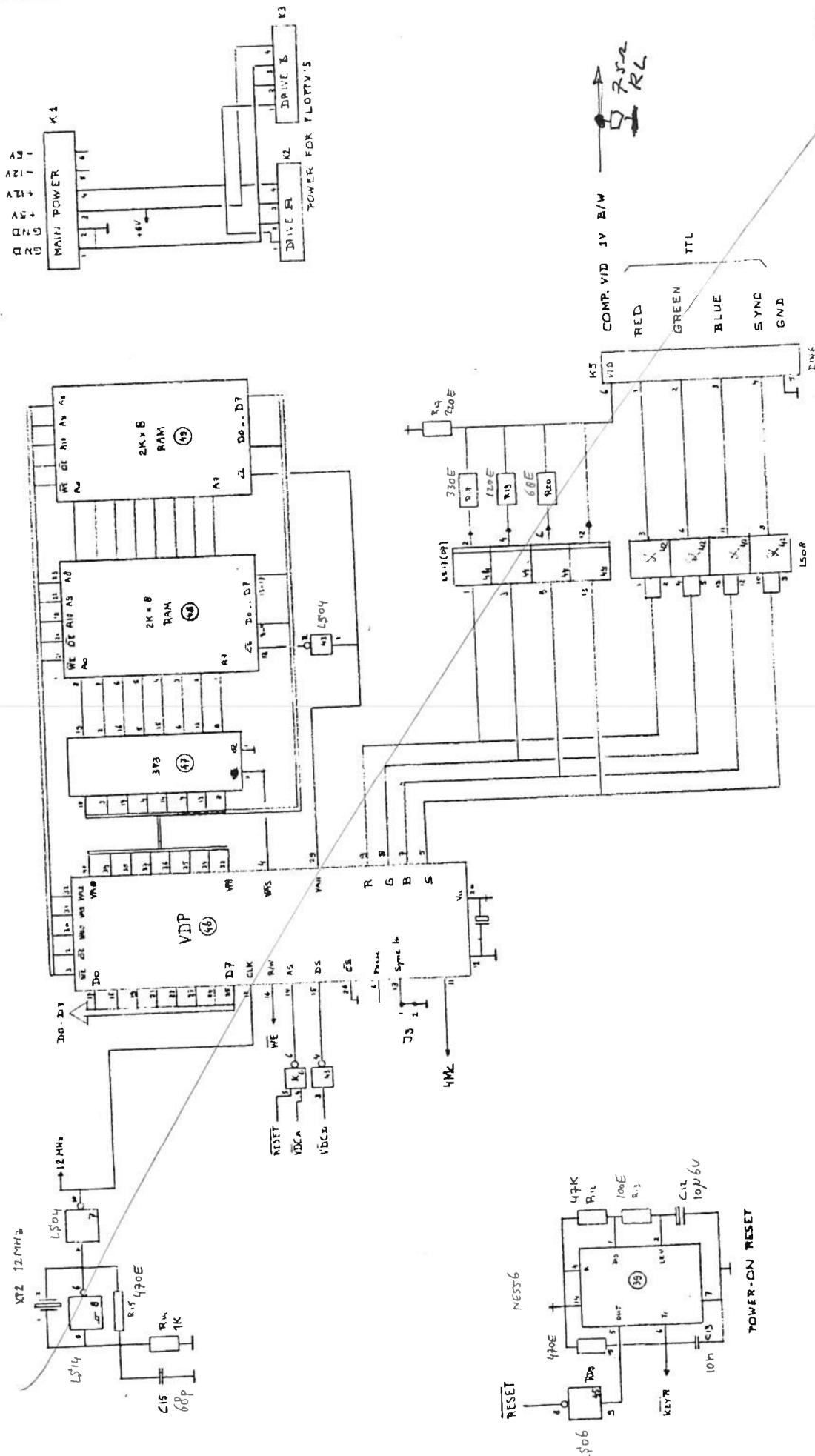
1 22 pF
 2 0,22 uF
 3 trimmer 4-60 pF
 4 150 pF
 5 47 uF/6 R
 6 470 nF
 7 10 uF/6 R
 8 330 pF
 9 330 pF
 10 330 pF
 11 330 pF
 12 10 uF/6 R
 13 10 nF ker
 14 47 pF
 15 68 pF

Others

=====

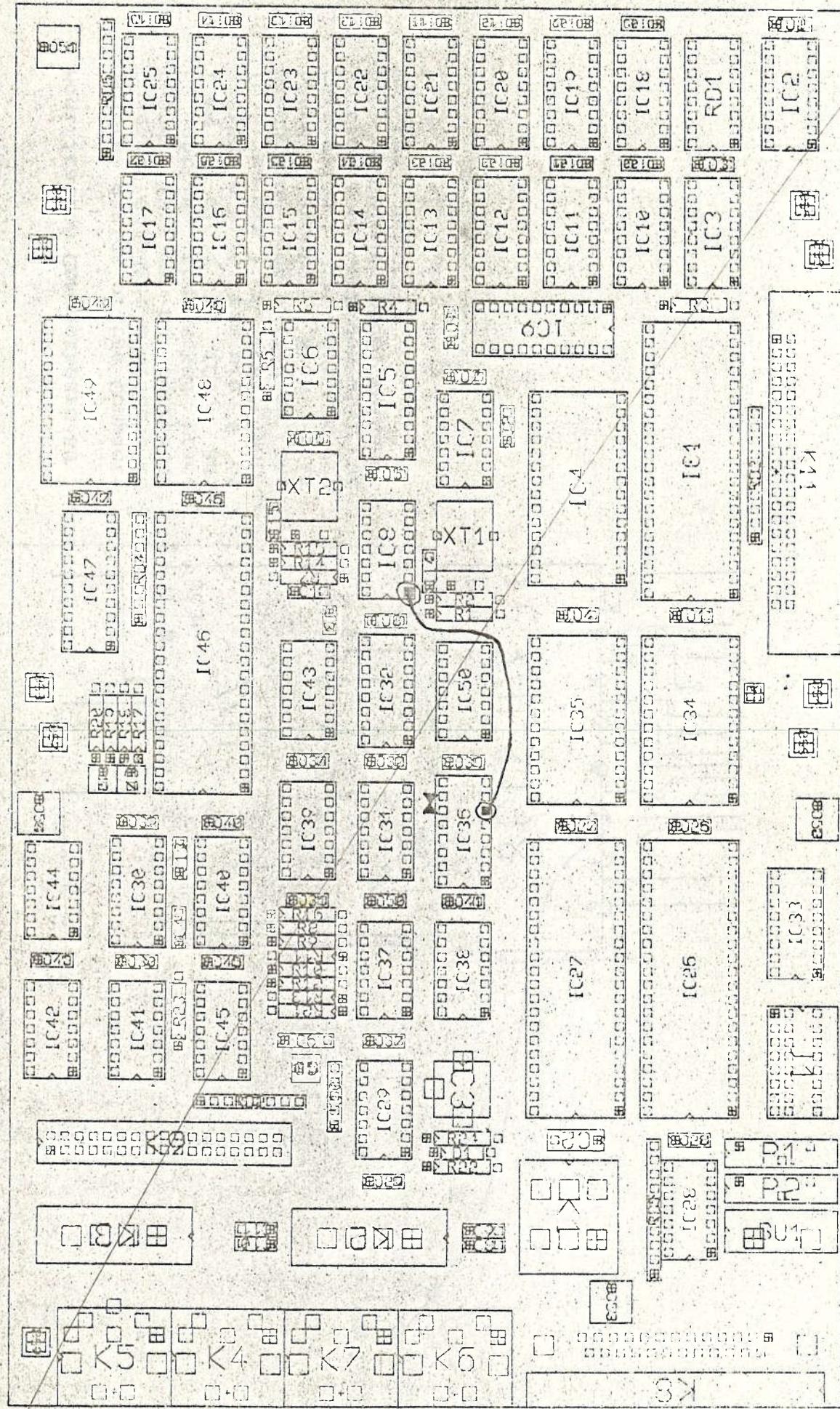
P 1 50 K
 P 2 10 K
 XT1 16 MHz crystal (ser)
 XT2 12 MHz crystal (ser)
 RD1 DIL 8x 22E (sep)
 RD2 SIL 7x150E (comm)
 RD3 SIL 9x3,3K (comm)
 RD4 SIL 7x3,3K (comm)
 RD5 opt. SIL 9x470E (comm)
 RD6 SIL 9x1K (comm)
 D1 1N4148
 PIN1 GND-pin
 BUZ1 Buzzer

APPENDIX A Circuit diagrams



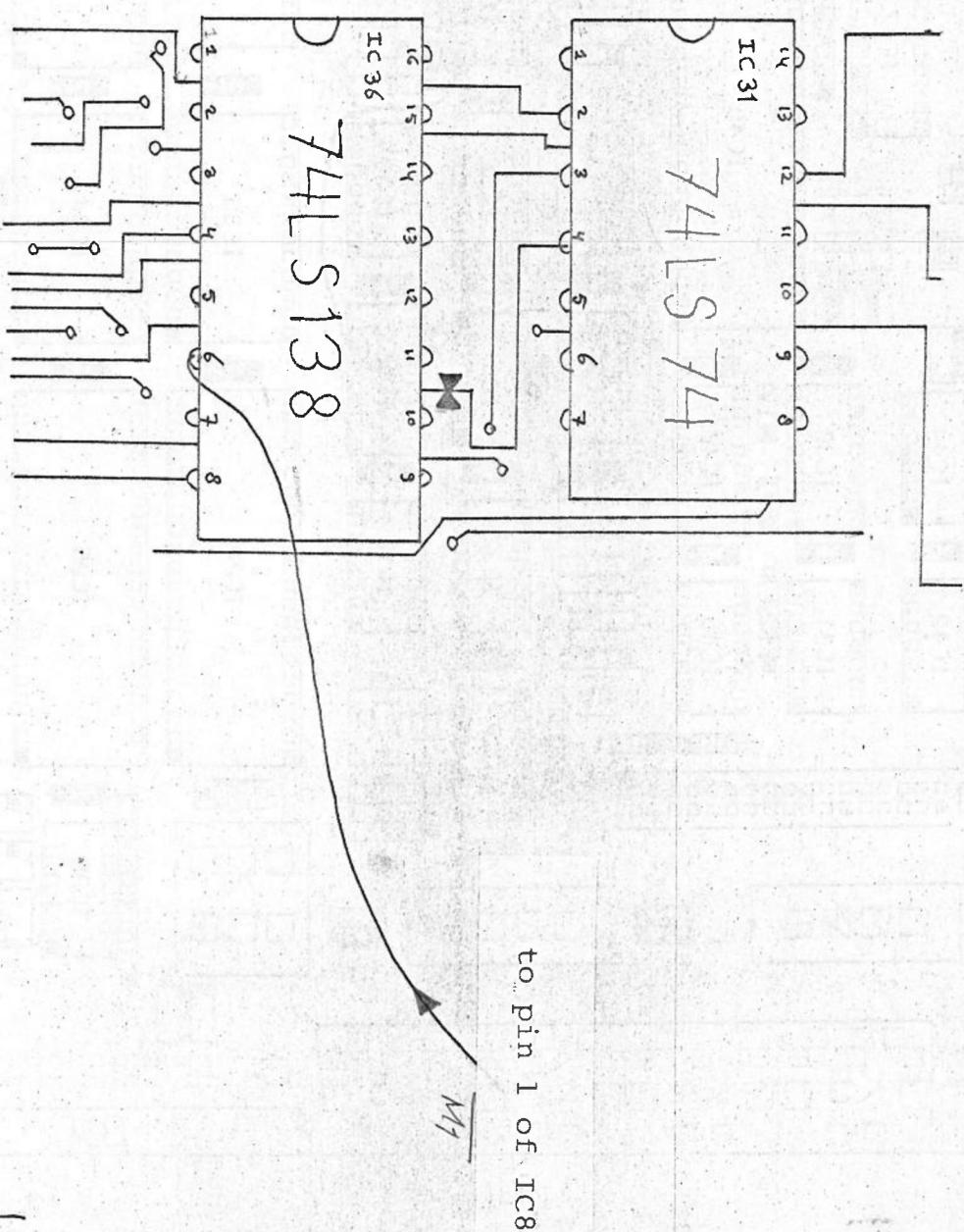
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Z80 VIDEO

PE226
3/1/86



Modification Compactboard-80

In the design of the Compactboard-80 computer a mistake is found. This can be corrected by cutting the marked trace (►) close to IC36 and adding a wire from pin 6 of IC36 to pin 1 of IC8. These pins have been marked on the board layout. When this correction is not made, Version 1 of Combidos will not boot. Previous (pre-) releases may run correctly.



► = cut here.

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