Intel® StrongARM® SA-110 Microprocessor

Brief Datasheet

Product Features

The Intel® StrongARM® SA-110 Microprocessor (SA-110), the first member of the StrongARM® family of high-performance, low-power microprocessors, is optimized for meeting embedded consumer application and portable application requirements. Offering power-saving features, low cost, and high performance and price/performance, the SA-110 is a solution for high-bandwidth network switching, intelligent office machines, storage systems, and internet appliances, as well as digital cameras, bar-code scanners, and other emerging consumer applications. In addition, to delivering performance requirements in a low-power design, the SA-110 offers compatibility with existing ARM™ development tools and operating systems.

- High performance
  - —115 Dhrystone 2.1 MIPS @ 100 MHz
  - —185 Dhrystone 2.1 MIPS @ 160 MHz
  - —192 Dhrystone 2.1 MIPS @ 166 MHz
  - —230 Dhrystone 2.1 MIPS @ 200 MHz
  - —268 Dhrystone 2.1 MIPS @ 233 MHz
- Low power
  - —<300 mW @1.65 V/100 MHz
  - —<450 mW @1.65 V/160 MHz
  - —<700 mW @2.0 V/166 MHz
  - —<900 mW @2.0 V/200 MHz
  - —<1000 mW @2.0 V/233 MHz
- Internal phase-locked loop (PLL)
  - —3.68- or 3.56-MHz oscillator
- Power-management features
  - —Idle (power-down) mode
  - —Sleep (power-down) mode
- Big and little endian operating modes
- 3.3-V I/O interface
- 144-pin thin quad flat pack (TQFP)
- 32-way set-associative caches
  - —16 Kbyte instruction cache
  - —16 Kbyte write-back data cache
- 32-entry MMUs
  - —Maps 4 Kbyte, 64 Kbyte, or 1 Mbyte
- Write buffer
  - —8-entry, 16 bytes each
- Memory bus
  - —Asynchronous or synchronous
  - —0-33 MHz @ 100 MHz
  - —0-53 MHz @ 160 MHz
  - —0-53 MHz @ 166 MHz
  - —0-66 MHz @ 200 MHz
  - —0-66 MHz @ 233 MHz

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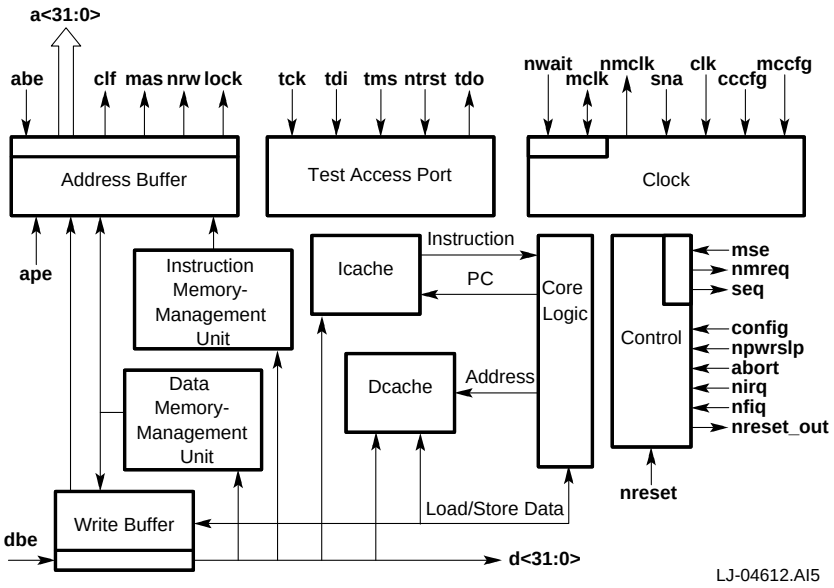
Description

The SA-110 is a general-purpose, 32-bit RISC microprocessor with a 16 Kbyte instruction cache (Icache); a 16 Kbyte write-back data cache (Dcache); a write buffer; and a memory-management unit (MMU) combined in a single component. The five-stage pipeline distributes tasks evenly over time to remove bottlenecks, ensuring high throughput for the core logic. The SA-110 on-chip MMU supports a conventional two-level page-table structure, with a number of extensions. These features result in a high instruction throughput and real-time response for a small and cost-effective microprocessor.

Microarchitecture

The SA-110 CPU implements the ARM™ Version 4 architecture as defined in the *ARM Architecture Reference Manual*. Figure 1 shows a block diagram of the SA-110.

Figure 1. Block Diagram of the SA-110



Bus Interface Logic

The bus interface logic, consisting of the control logic and the address register, controls the bus interface and unplanned events such as interrupts, resets, and aborts. The bus interface logic can also enable or disable wrapping of read transactions and merging of write transactions.

The bus interface can be configured to run synchronously or asynchronously to the core logic. In synchronous mode, the bus interface clock speed is the core clock rate divided by a programmable integer value from 2 to 9 (maximum of 66 MHz).

Write Buffer

The SA-110 has an 8-entry write buffer with each entry able to contain 1 byte to 16 bytes. The write buffer can be enabled or disabled by software. The write buffer is further controlled by a bit in the MMU page tables; so the MMU must be enabled before the write buffer can be used. Software can cause the write buffer to be flushed.

Core Logic

The core logic fetches and executes instructions by using a five-stage pipeline. The five stages are: fetch, decode, arithmetic logic unit (ALU), cache, and write-back. This pipeline arrangement, using the on-chip ALU, distributes tasks evenly in time and, therefore, contributes to the high performance of the core logic.

The ARM™ architecture supports 30 general-purpose registers, one program counter, and six status registers. There are 16 general-purpose registers (including the PC register) and one or two status registers visible at any one time. The processor operating mode determines which registers are visible.

The core logic executes the ARM™ instruction set, which supports straight-forward assembly language code programming. It does not depend upon sophisticated compilers to manage complicated instruction interdependence. The instruction set has eight instruction classes:

- Two instruction classes use the on-chip ALU, barrel shifter, and multiplier to perform high-speed operations on the data in a bank of 16 logical (31 physical) 32-bit registers.
- Three instruction classes control data transfer between memory and the registers. The classes are optimized for flexible addressing, rapid context switching, and swapping data.
- Two instruction classes control execution flow and execution privilege level.
- One instruction class accesses the privileged state of the SA-110.

The core logic implements 32-bit virtual addresses and 32-bit physical addresses. A 12-bit multiplier with early termination performs multiplication. The number of cycles needed to perform a multiplication operation depends on the magnitude of the operands, as shown in Table 1.

Table 1. Core Logic Multiplication Functions

Multiplication Operation (Signed or Unsigned)	Result Size	Operation Duration
32 x 32	32 bits	2–4 cycles
32 x 32 + 32	32 bits	2–4 cycles
32 x 32	64 bits	3–5 cycles
32 x 32 + 64	64 bits	3–5 cycles

Memory-Management Units

The SA-110 has two MMUs: instruction (IMMU) and data (DMMU). Separate translation look-aside buffers (TLBs) are implemented for the instruction and data streams. The TLBs each have 32 entries that can each map a segment, a large page, or a small page. The TLB entry replacement

algorithm is round robin. The data TLB supports both the flush-all and the flush-single-entry function, while the instruction TLB supports only the flush-all function. Memory-management exceptions preserve the base address registers, eliminating the need for “fix-up” code.

Cache

The SA-110 has a 16 Kbyte, 32-way, set-associative Icache with 32-byte blocks and a 16 Kbyte, 32-way, set-associative, write-back Dcache with 32-byte blocks.

Instruction Cache

The Icache supports the flush-all-entry function, and the replacement algorithm is round-robin within a set. The Icache can be enabled or disabled independent of the memory-management function. When memory management is disabled, the Icache control logic considers all memory to be cacheable.

Data Cache

The write-back Dcache supports the flush-all-entry, flush-entry, and copyback-entry functions. The copyback-all function is not provided in hardware but can be provided by software. The Dcache entries are allocated with read transactions and the entry replacement logic uses a round-robin algorithm.

Clocks

The SA-110 receives a 3.68-MHz clock from a crystal-based clock generator. The SA-110 uses an internal PLL to multiply the frequency by a variable multiplier to produce a high-speed clock. The high-speed clock is then divided internally by a configurable ratio to provide a system clock for synchronous operation. The 3.68-MHz oscillator and PLL run constantly in normal and idle mode.

Boundary-Scan Test Logic

The SA-110 boundary-scan interface provides for driving and sampling of all the external pins of the device except **npwrslp**, irrespective of the core logic state. This ability permits testing of:

- SA-110 electrical connections to the circuit board.
- Integrity of connections between devices having a similar interface on the circuit board.

Signal Lines

Figure 2 shows the signal connects to and from the SA-110. The signals are arranged within functional groups.

Figure 2. Functional Group Signal Lines

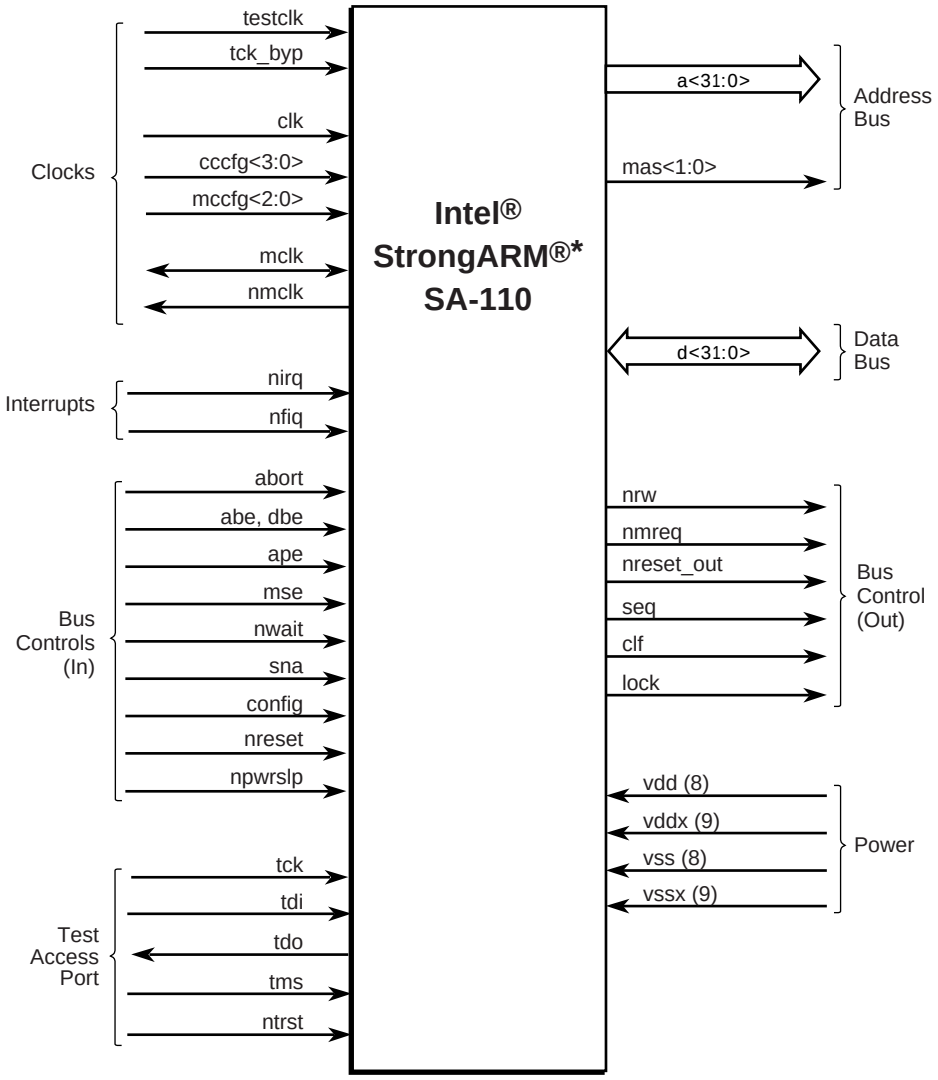


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Table 2. SA-110 Characteristics

	100 MHz	160 MHz	166 MHz	200 MHz	233 MHz	233 MHz
Performance	115 Dhrystone 2.1 MIPS	185 Dhrystone 2.1 MIPS	192 Dhrystone 2.1 MIPS	230 Dhrystone 2.1 MIPS	268 Dhrystone 2.1 MIPS	268 Dhrystone 2.1 MIPS
Core power supply	**Vss** = 0.0 V dc **Vdd** = 1.65 V dc ± 10%	**Vss** = 0.0 V dc **Vdd** = 1.65 V dc ± 10%	**Vss** = 0.0 V dc **Vdd** = 2.0 V dc ± 10%	**Vss** = 0.0 V dc **Vdd** = 2.0 V dc ± 10%	**Vss** = 0.0 V dc **Vdd** = 2.0 V dc ± 5%	**Vss** = 0.0 V dc **Vdd** = 2.0 V dc ± 5%
I/O power supply	**Vssx** = 0.0 V dc **Vddx =** 3.3 V dc ± 10%	**Vssx** = 0.0 V dc **Vddx =** 3.3 V dc ± 10%	**Vssx** = 0.0 V dc **Vddx** = 3.3 V dc ± 10%	**Vss** = 0.0 V dc **Vdd** = 3.3 V dc ± 10%	**Vss** = 0.0 V dc **Vdd** = 3.3 V dc ± 10%	**Vss** = 0.0 V dc **Vdd** = 3.3 V dc ± 10%
Power dissipation	Max. = <300 mW Typical = <110 mW	Max. = <450 mW Typical = <136 mW	Max. = <700 mW	Max. = <900 mW	Max. = <1000 mW	Max. = <1000 mW
Modes	Sleep current = 50 µA Idle power = <20 mW	Sleep current = 50 µA Idle power = <20 mW	—	—	—	—
Maximum junction temperature	Tj = 100°C (212°F)	Tj = 100°C (212°F)	Tj = 100°C (212°F)	Tj = 100°C (212°F)	Tj = 100°C (212°F)	Tj = 100°C (212°F)
Ambiant operating temperature	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 60°C
Storage temperature	–20°C to +125°C (–4°F to +257°F)	–20°C to +125°C (–4°F to +257°F)	–20°C to +125°C (–4°F to +257°F)	–20°C to +125°C (–4°F to +257°F)	–20°C to +125°C (–4°F to +257°F)	–20°C to +125°C (–4°F to +257°F)
Packaging	144-pin TQFP	144-pin TQFP	144-pin TQFP	144-pin TQFP	144-pin TQFP	144-pin TQFP
Process technology	.35 µm, 3-layer metal	.35 µm, 3-layer metal	.35 µm, 3-layer metal	.35 µm, 3-layer metal	.35 µm, 3-layer metal	.35 µm, 3-layer metal
Transistor count	2.1 million	2.1 million	2.1 million	2.1 million	2.1 million	2.1 million
Order number	21281BB	21281AB	21281DB	21281CB	21281EB	21281FB

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