DLD ASSESSMENT 3

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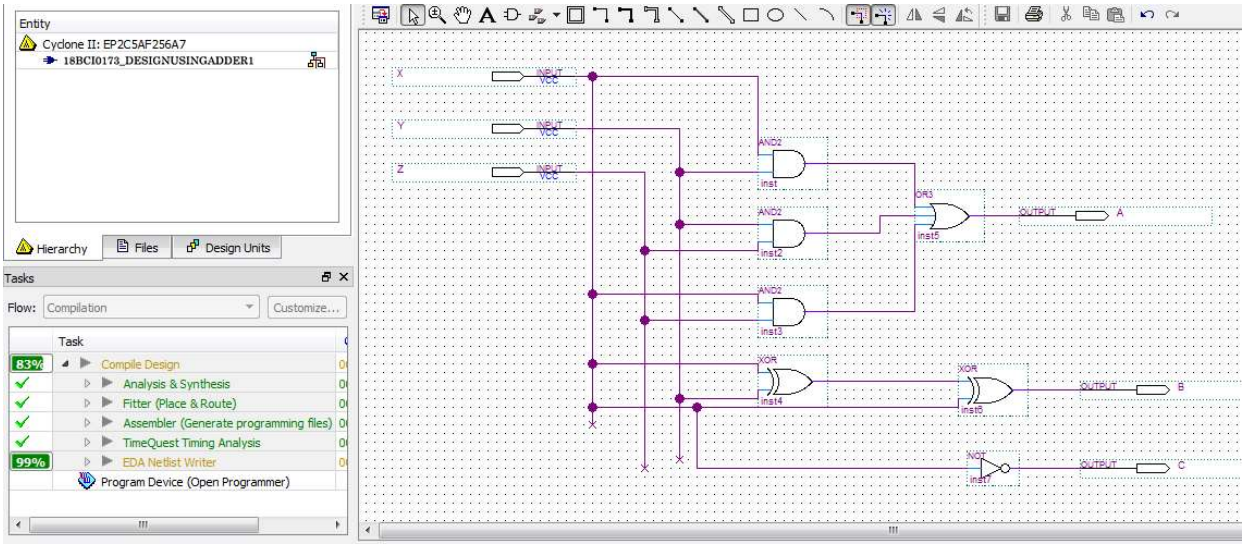
SLOT: L25 + L26

FACULTY: PROF. LIJO VP

QUESTION 1

a. **AIM:** Design a combinational circuit with three inputs x,y and z and three outputs A,B nd C using full adders and an inverter. When the binary input is 0,1,2 or 3 the binary output is one greater than the input. When the binary input is 4,5,6 or 7 the binary output is one less than the input.

CIRCUIT DIAGRAM:



TRUTH TABLE:

X	Y	Z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

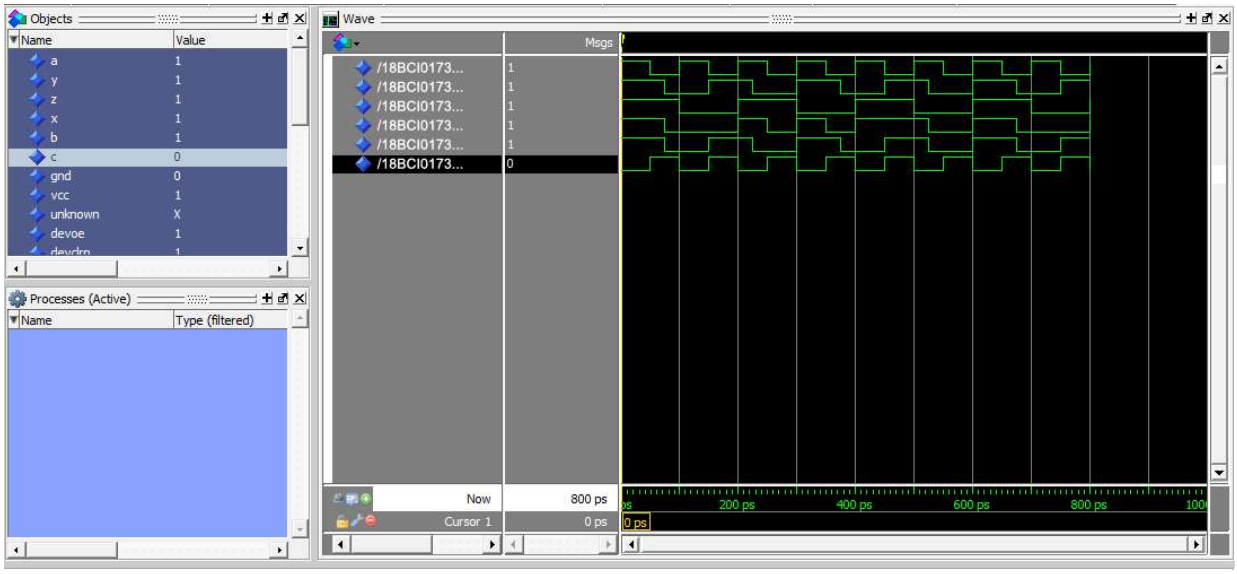
EXPRESSIONS:

A= YZ + XZ + XY

B= X xor Y xor Z

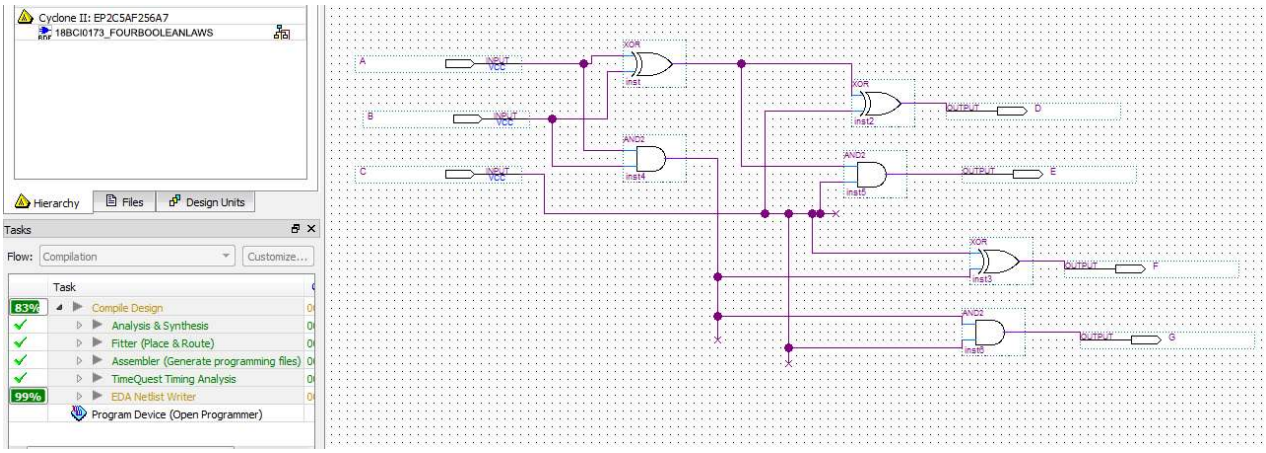
C= Z’

FINAL RESULT:



AIM: implement the four Boolean functions listed using three half adders.

CIRCUIT DIAGRAM:



TRUTH TABLE:

A	B	C	D	E	F	G
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	1	0	0	0
0	1	1	0	1	1	0
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	1	0	1	1

EXPRESSIONS:

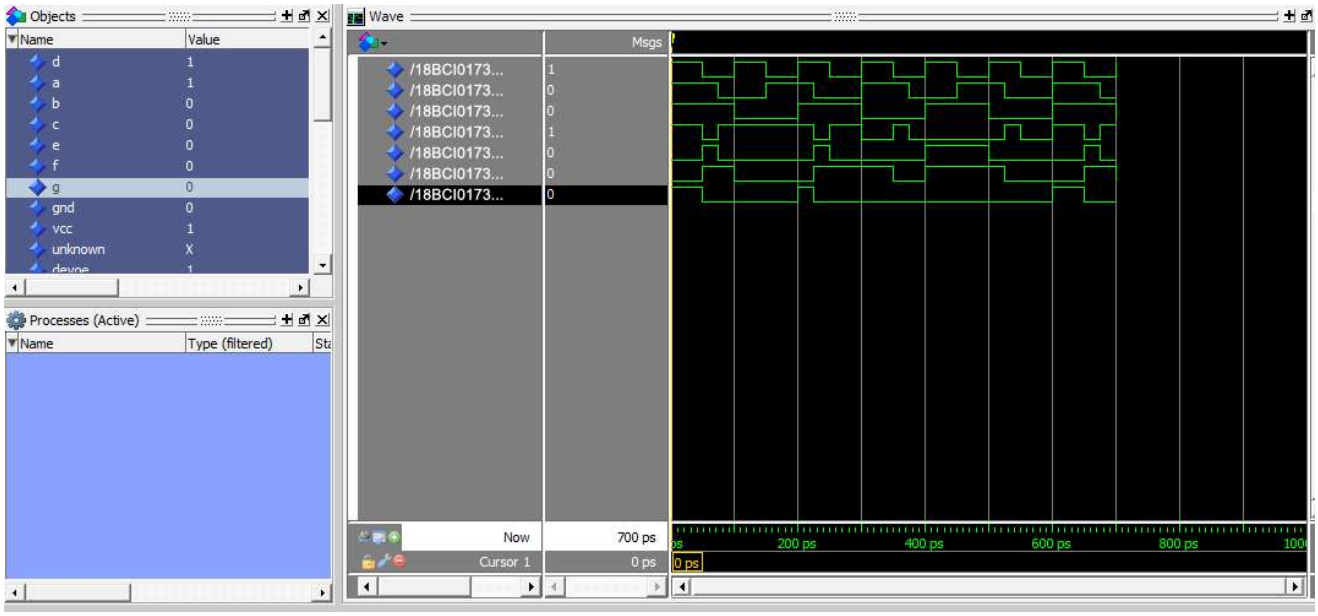
D= A XOR B XOR C

E= A’BC + AB’C

F= ABC’ + (A’ +B)C

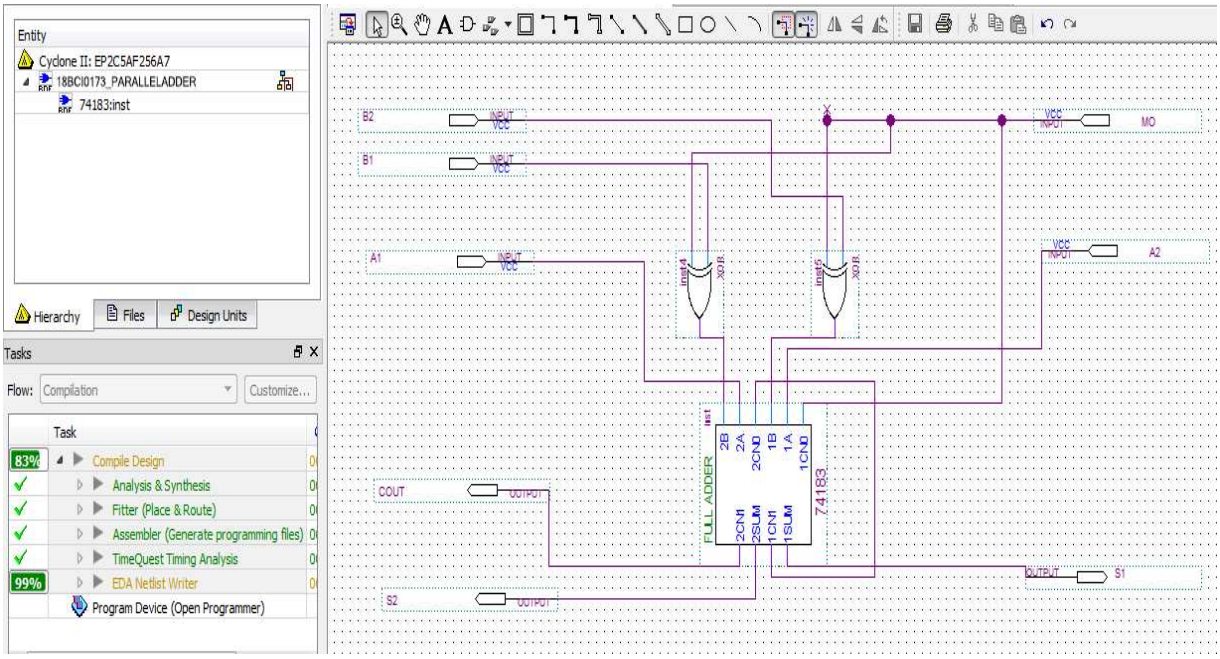
G= G=ABC

FINAL RESULT:



c. **AIM**: design 2-bit parallel adder/subtractor circuit.

CIRCUIT DIAGRAM:

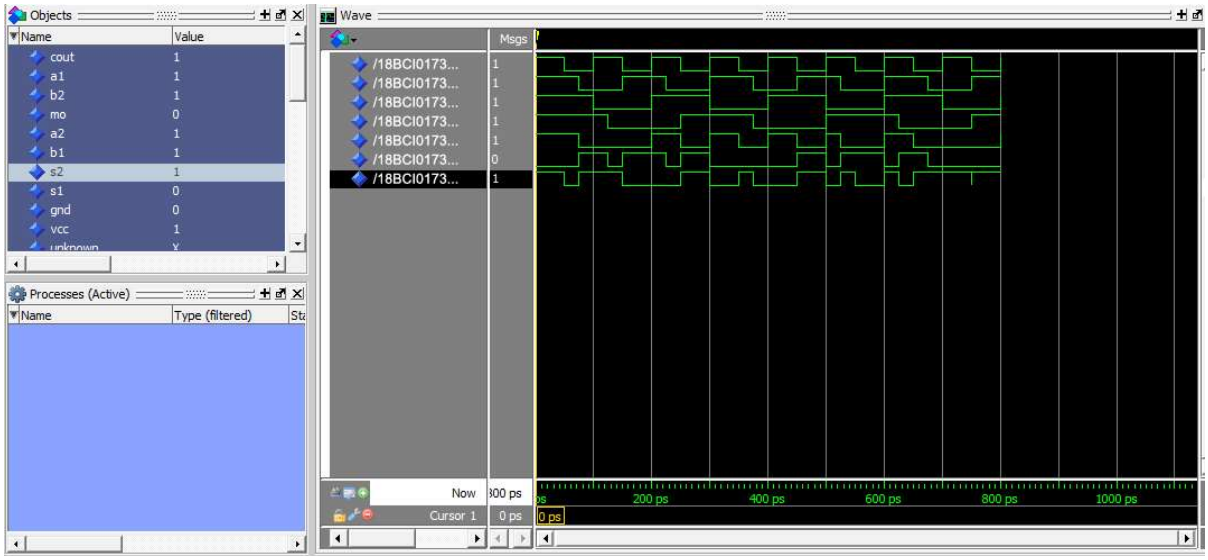


m=0 for addition of numbers a1 a2 and b1 b2

TRUTH TABLE:

A2	A1	B2	B1	C	S1	S2
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

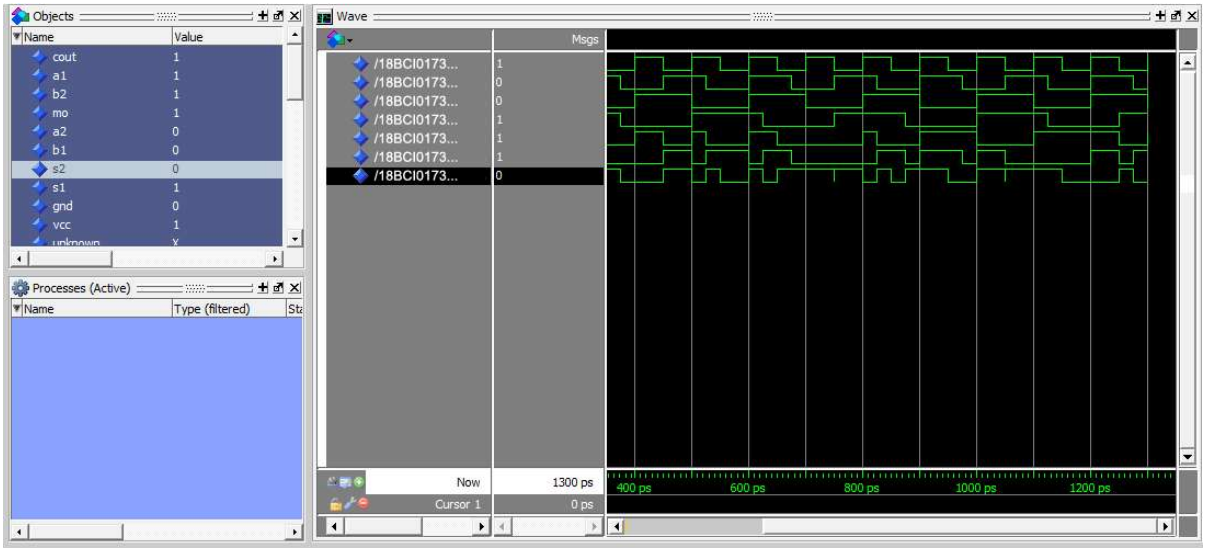
ADDER FINAL RESULT:



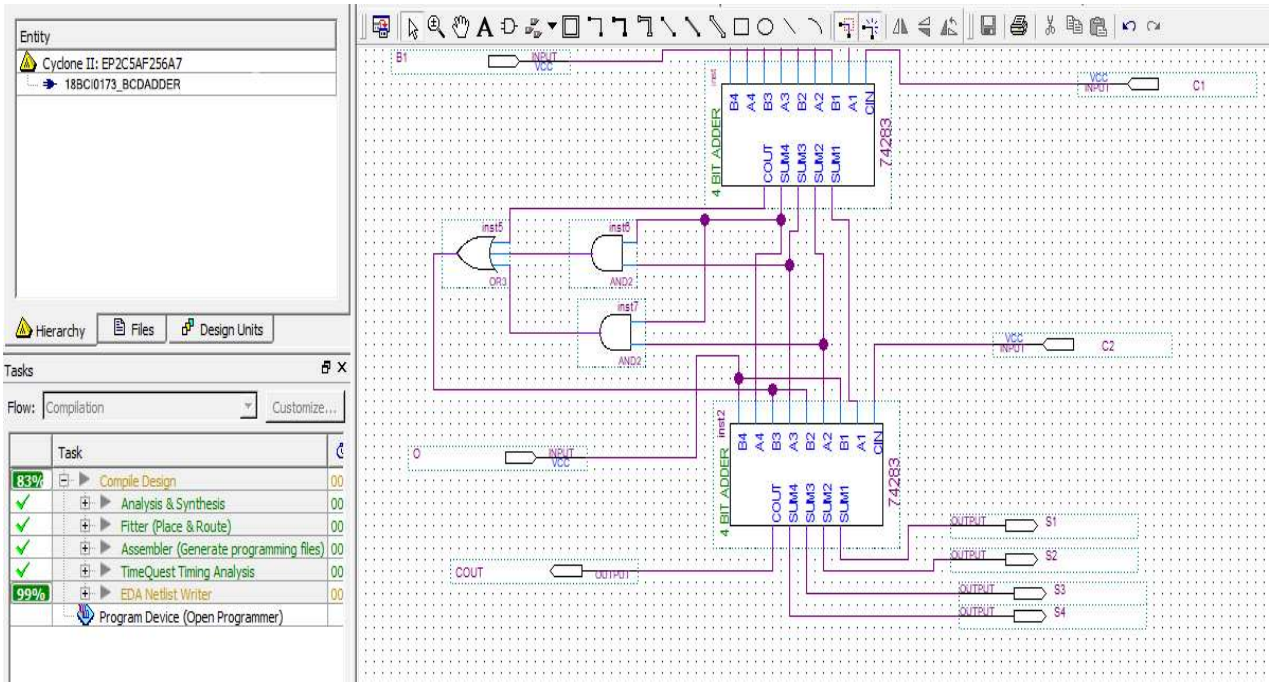
M=1 for subtraction of numbers a1 a2 and b1 b2.

A2	A1	B2	B1	C	S1	S2
0	0	0	0	0	0	0
0	0	0	1	1	1	0
0	0	1	0	1	0	1
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	0	0
0	1	1	0	1	1	0
0	1	1	1	1	0	1
1	0	0	0	0	1	0
1	0	0	1	0	0	1
1	0	1	0	0	0	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	0	1	0
1	1	1	0	0	0	1
1	1	1	1	0	0	0

SUBTRACTOR FINAL RESULT:



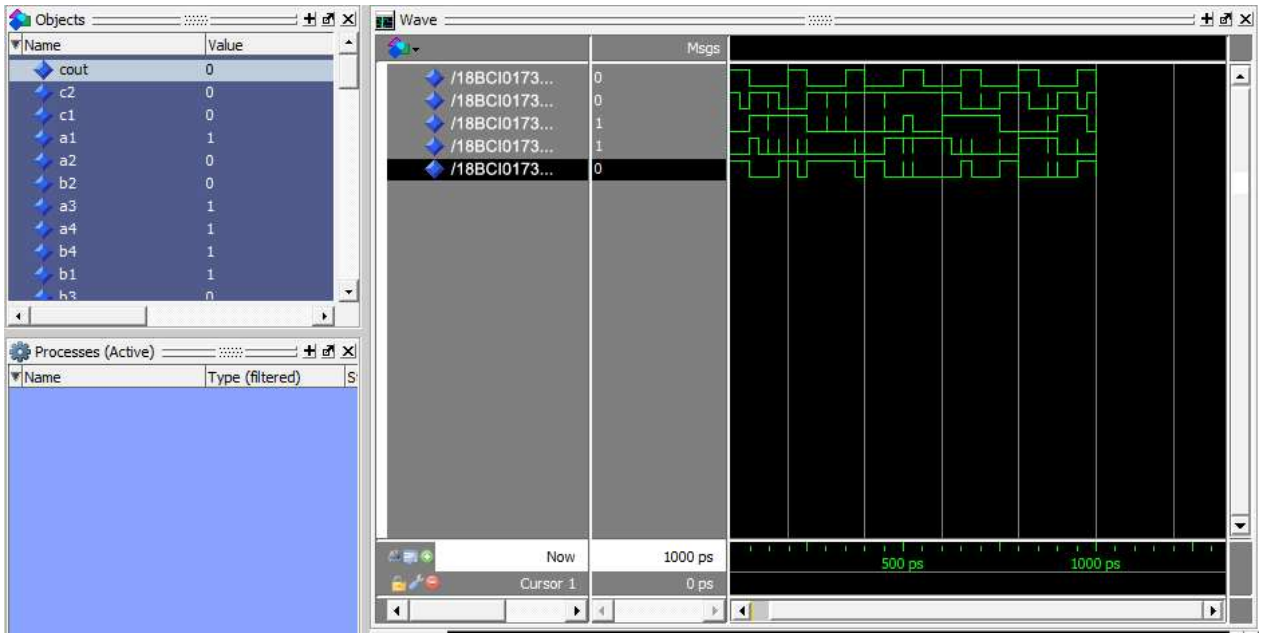
AIM: design a BCD adder using binary parallel adder.



TRUTH TABLE:

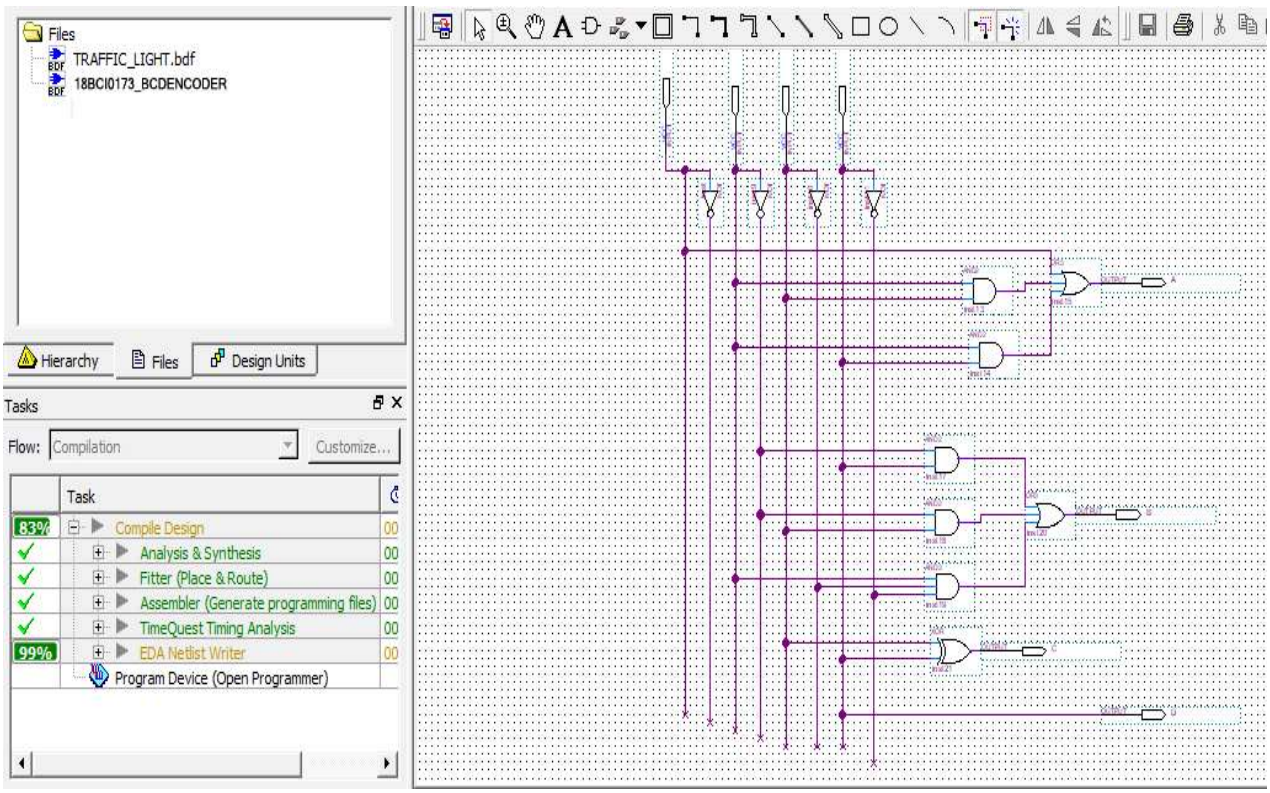
k	8	4	2	1	c	S4	S3	S2	S1	decimal
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	2
0	0	0	1	1	0	0	0	1	1	3
0	0	1	0	0	0	0	1	0	0	4
0	0	1	0	1	0	0	1	0	1	5
0	0	1	1	0	0	0	1	1	0	6
0	0	1	1	1	0	0	1	1	1	7
0	1	0	0	0	0	1	0	0	0	8
0	1	0	0	1	0	1	0	0	1	9
0	1	0	1	0	1	0	0	0	0	10
0	1	0	1	1	1	0	0	0	1	11
0	1	1	0	0	1	0	0	1	0	12
0	1	1	0	1	1	0	0	1	1	13
0	1	1	1	0	1	0	1	0	0	14
0	1	1	1	1	1	0	1	0	1	15
1	0	0	0	0	1	0	1	1	0	16
1	0	0	0	1	1	0	1	1	1	17
1	0	0	1	0	1	1	0	0	0	18
1	0	0	1	1	1	1	0	0	1	19

FINAL RESULT:



QUESTION 2

AIM: design a circuit to convert 2421 to 84-2-1.



TRUTH TABLE:

W	X	Y	Z	A	B	C	D	Decimal digit
0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	1	1
0	0	1	0	0	1	1	0	2
0	0	1	1	0	1	0	1	3
0	1	0	0	0	1	0	0	4
1	0	1	1	1	0	1	1	5
1	1	0	0	1	0	1	0	6
1	1	0	1	1	0	0	1	7
1	1	1	0	1	0	0	0	8
1	1	1	1	1	1	1	1	9

EXPRESSIONS:

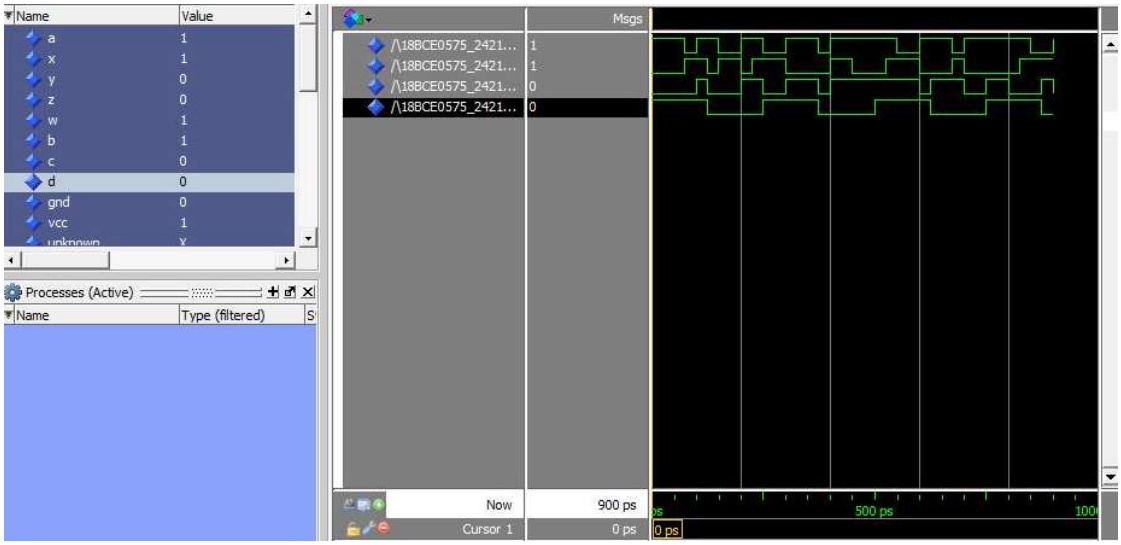
A= WX'YZ + WXY'Z' + WXY'Z + WXYZ' + WXYZ

B= W'X'Y'Z + W'X'YZ' + W'X'YZ+ W'XY'Z' + WXYZ

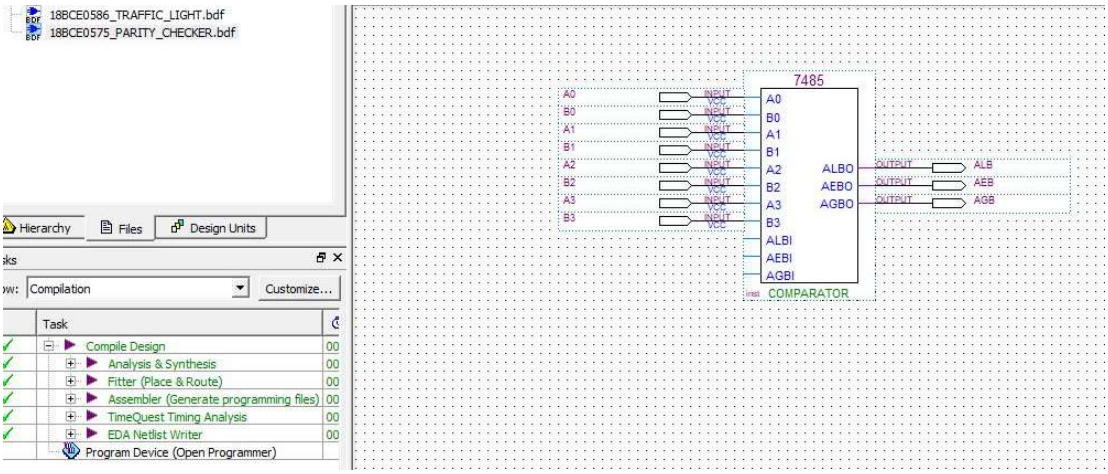
C= W'X'Y'Z + W'X'YZ' + WX'YZ + WXY'Z' + WXYZ

D= W'X'Y'Z + W'X'YZ + WX'YZ + WXY'Z + WXYZ

FINAL RESULT:



AIM: Design a circuit to compare two 4 bit numbers using IC 7485.



TRUTH TABLE:

A	B	A<B	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

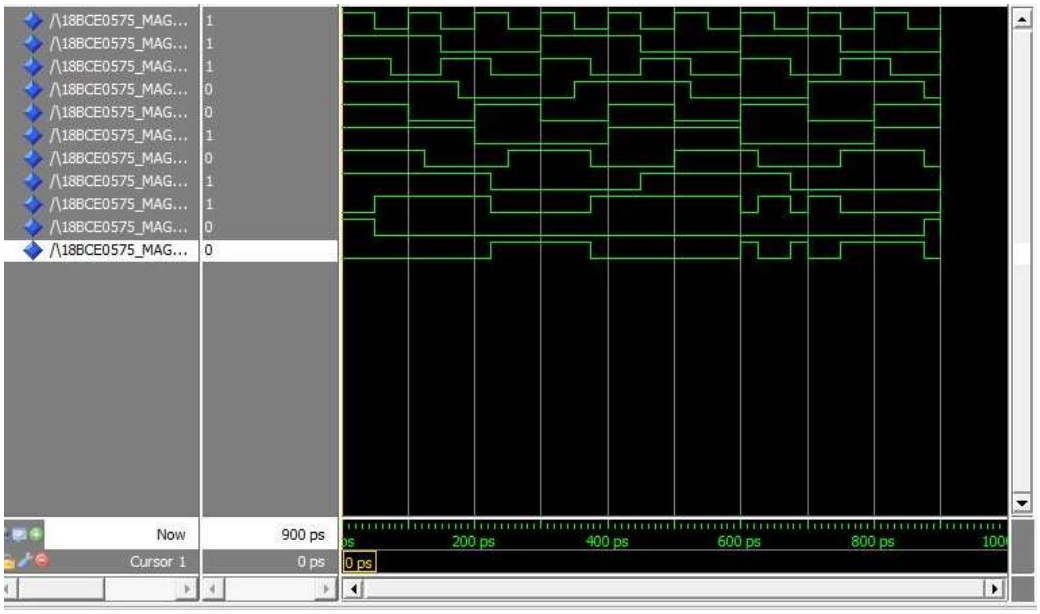
EXPERESSION:

A EQUAL TO B: (A0 XNOR B0)(A1 XNOR B1)(A2 XNOR B2)(A3 XNOR B3).

A GREATER THAN B: A3B3’ + (A3 XNOR B3)A2B2’ +(A3 XNOR B3)(A2 XNOR B2)A1B1’ + (A3 XNOR B3)(A2 XNOR B2)(A1 XNOR B1)A0B0’

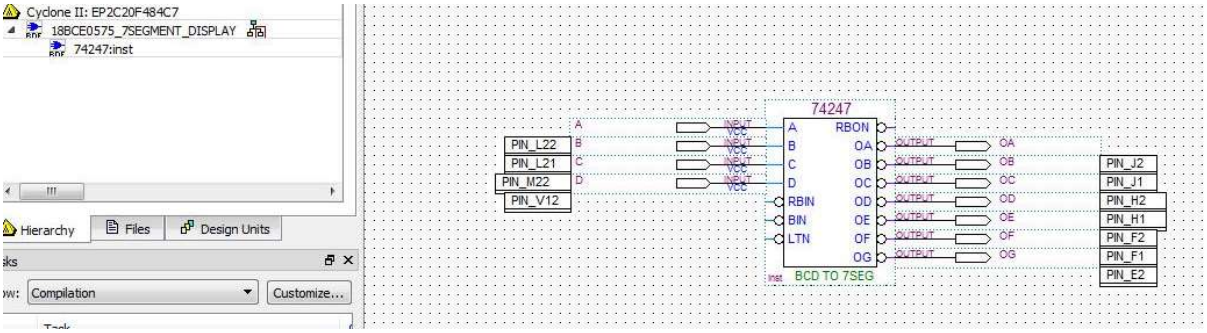
A LESS THAN B: A3’B3 + (A3 XNOR B3)A2’B2 +(A3 XNOR B3)(A2 XNOR B2)A1’B1 +(A3 XNOR B3)(A2 XNOR B2)(A1 XNOR B1)A0’B0

FINAL RESULT:



AIM: To design BCD to seven segment display

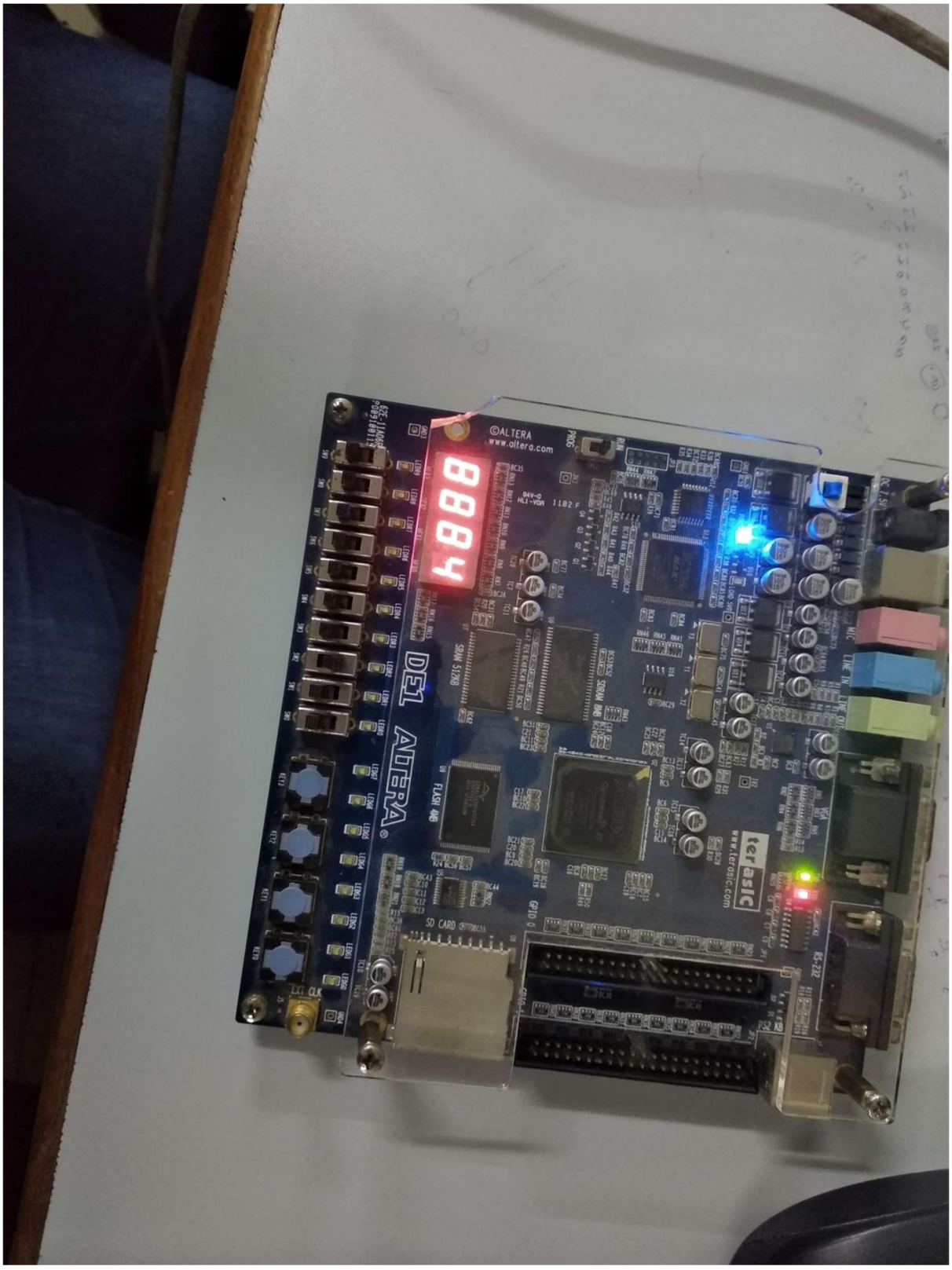
CIRCUIT DIAGRAM:



TRUTH TABLE:

A	B	C	D	OA	OB	OC	OD	OE	OF	OG
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

FINAL RESULT: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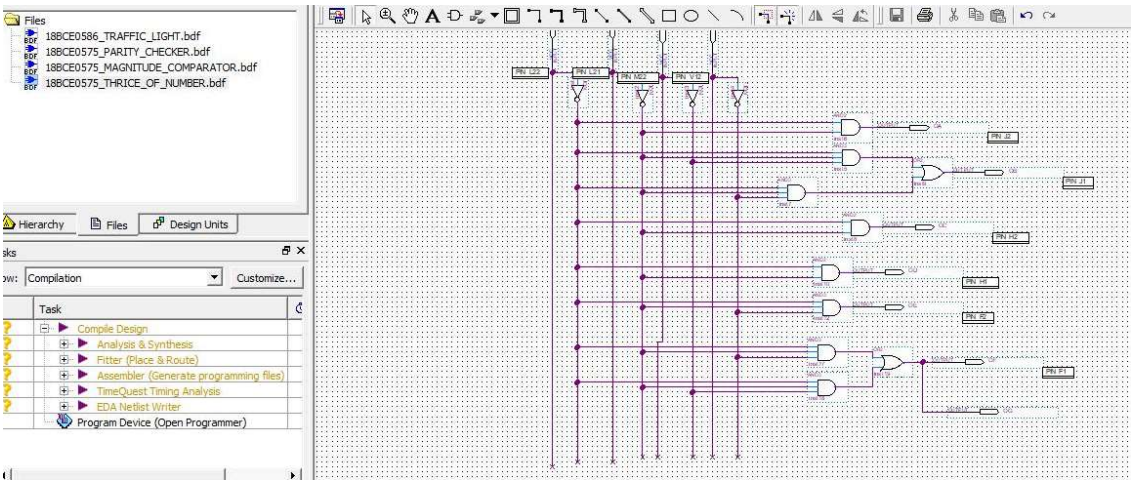
AIM: Design a circuit to display thrice of a number on seven segment display (consider maximum input number to be 2 bit)

CIRCUIT DIAGRAM:



TRUTH TABLE:

A	B	C	D	OA	OB	OC	OD	OE	OF	OG
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	0	0	1
0	0	1	0	1	0	1	1	1	1	1
0	0	1	1	1	1	1	1	0	1	1

EXPRESSIONS:

OA= A'B'

OB=A'B'C' + A'B'D

OC= A'B'

OD= A'B'

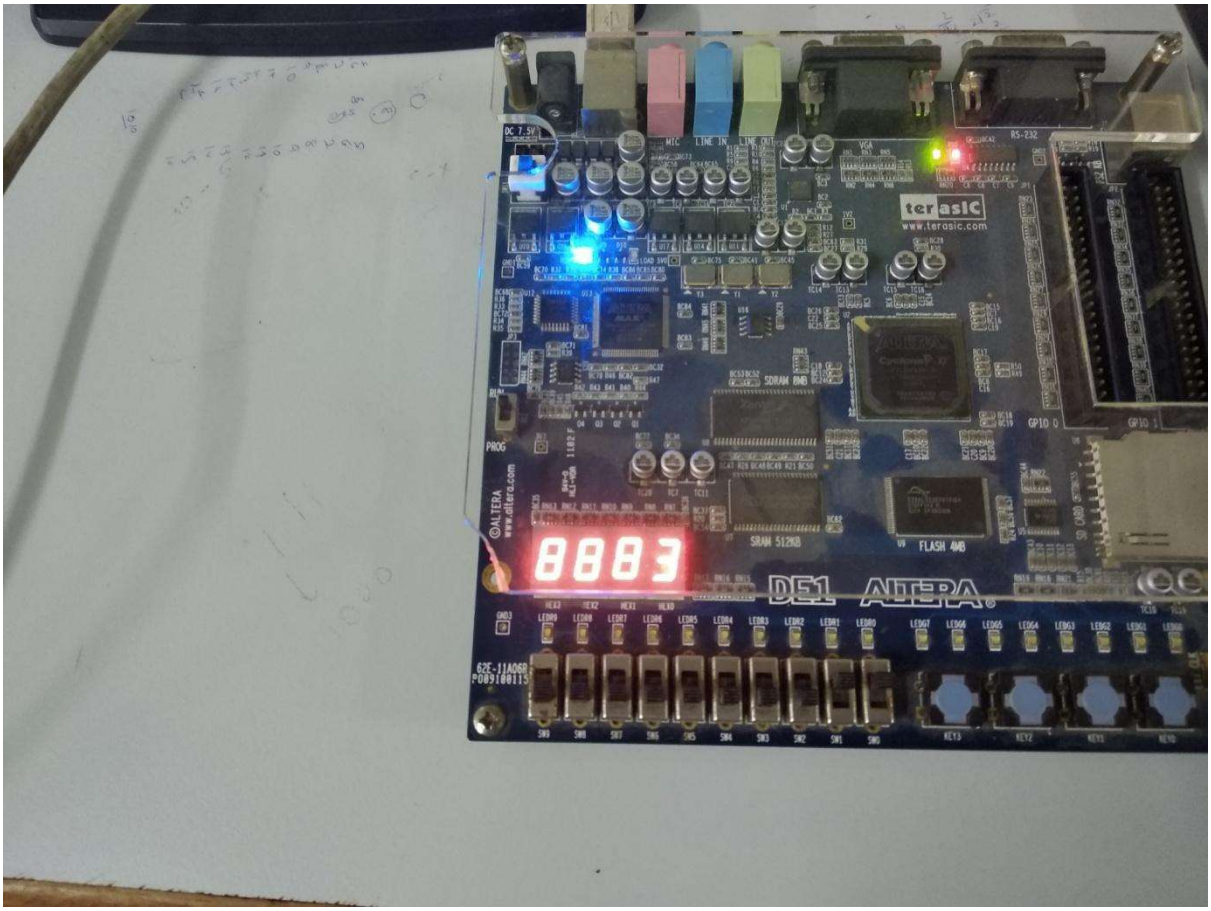
OE = A'B'D'

OF = A'B'D' + A'B'C

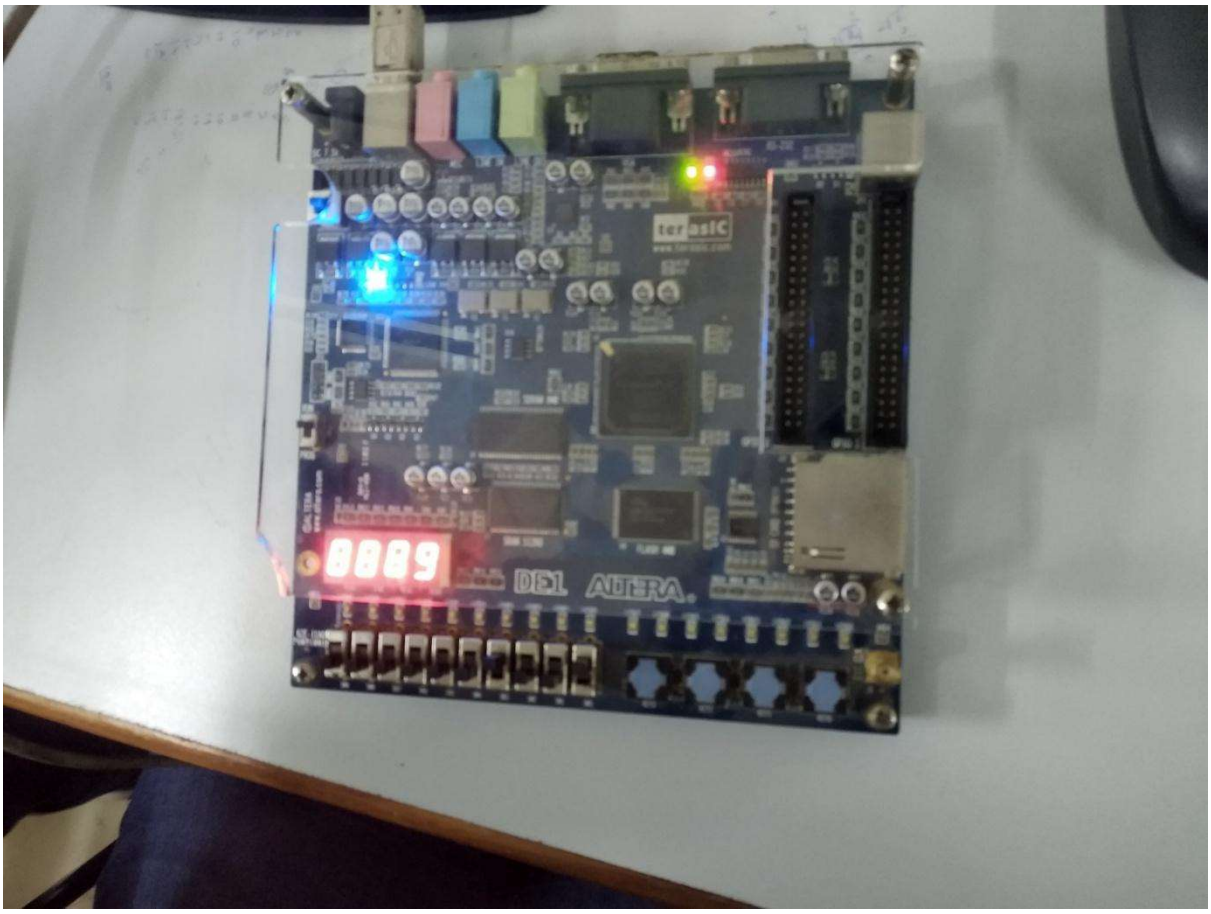
OG = A'B'D +A'B'C

FINAL RESULT:

Thrice of 1



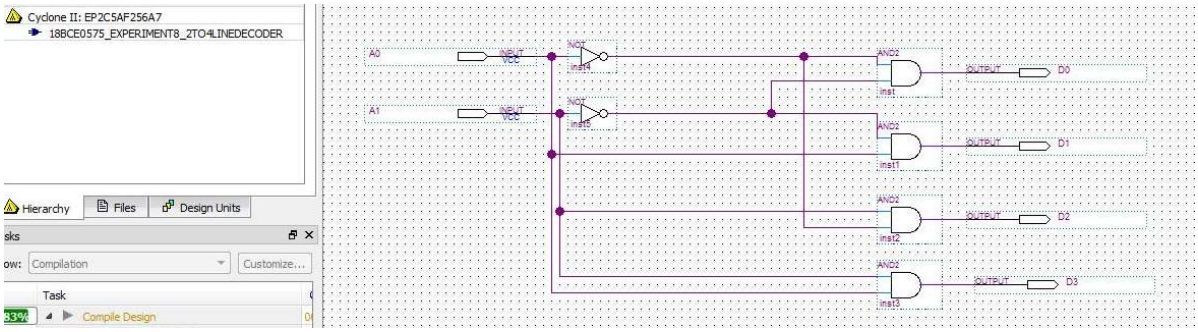
Thrice of 3



QUESTION 3

a. **AIM:** To design a 2 to 4 line decoder.

CIRCUIT DIAGRAM:



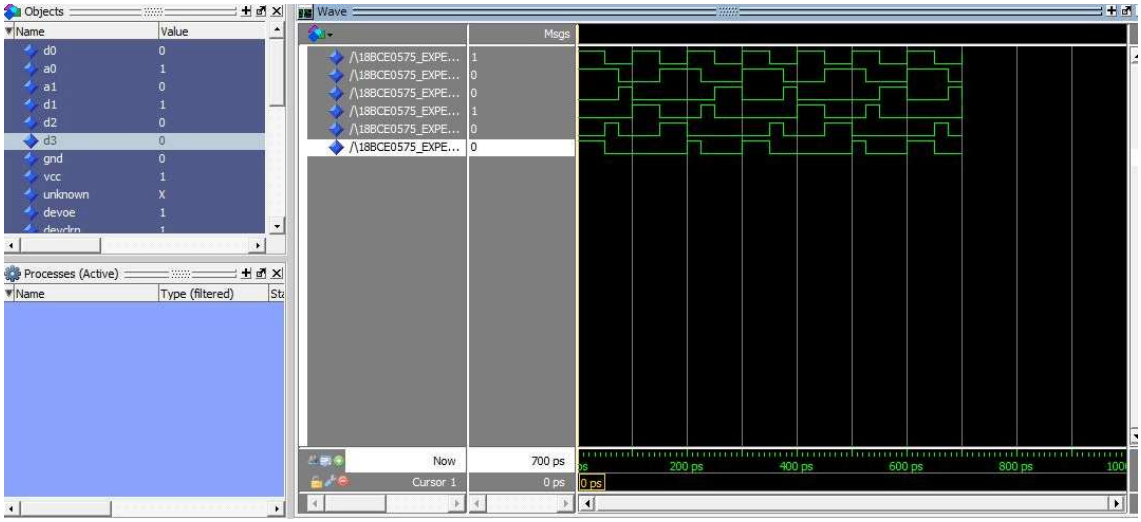
TRUTH TABLE:

A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

EXPERESSIONS:

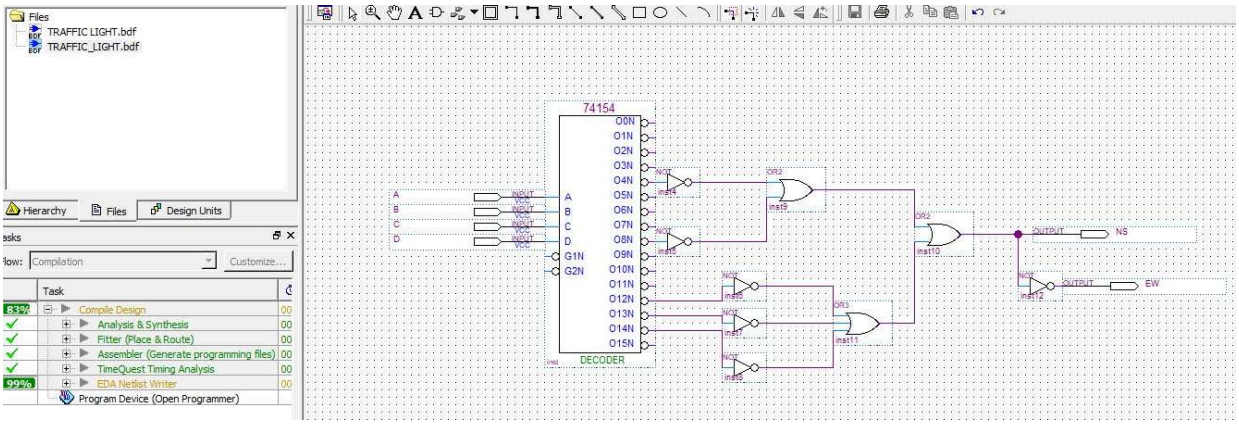
1. D0= A'B'
2. D1=A'B
3. D2=AB'
4. D3=AB

FINAL RESULT:



b. **AIM:** Design a logic circuit to control the traffic light as per the given details. Using the sensor outputs A,B,C and D as inputs, N-S and E-W be two outputs that go high.

CIRCUIT DIAGRAM:



TRUTH TABLE:

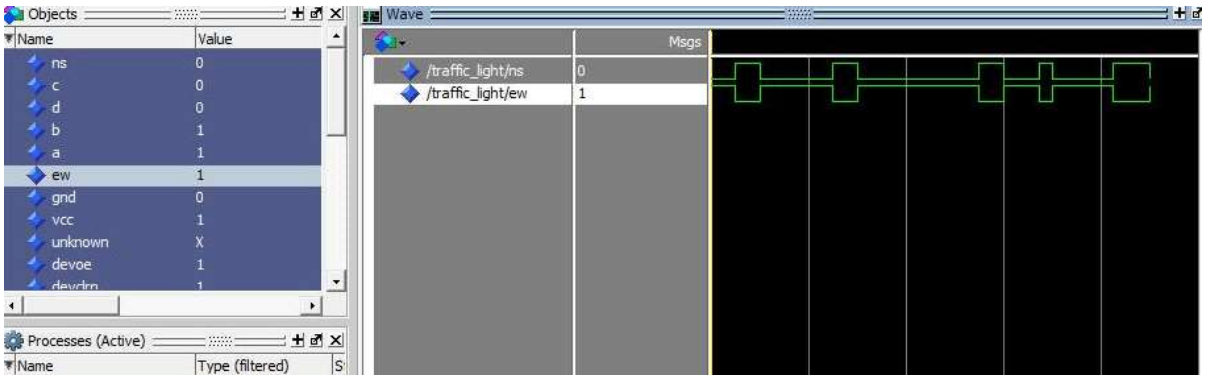
A	B	C	D	EW	NS
0	0	0	0	1	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	1	0

EXPRESSIONS:

NS= A'BC'D' + AB'C'D' + ABC'D' + ABC'D + ABCD'

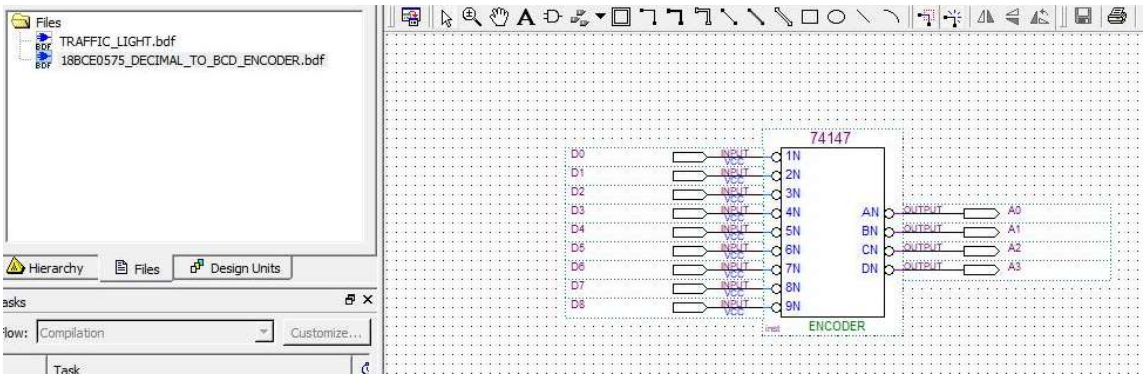
ES= NS'

FINAL RESULT:



c. **AIM**: Design a decimal to BCD encoder.

CIRCUIT DIAGRAM:



TRUTH TABLE:

DECIMAL	A3	A2	A1	A0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

EXPRESSIONS:

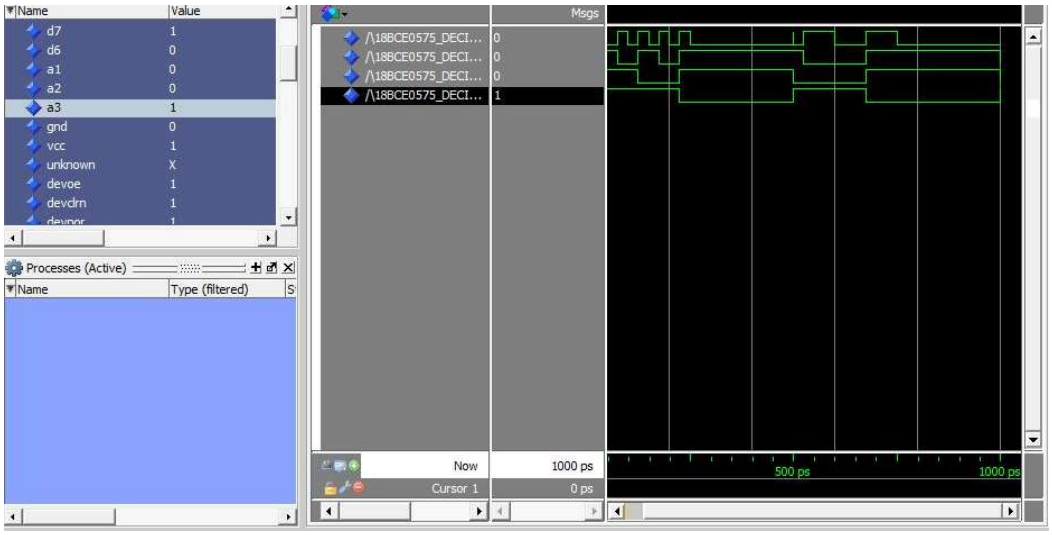
A3=D8+D9

A2=D4+D5+D6+D7

A1=D2+D3+D6+D7

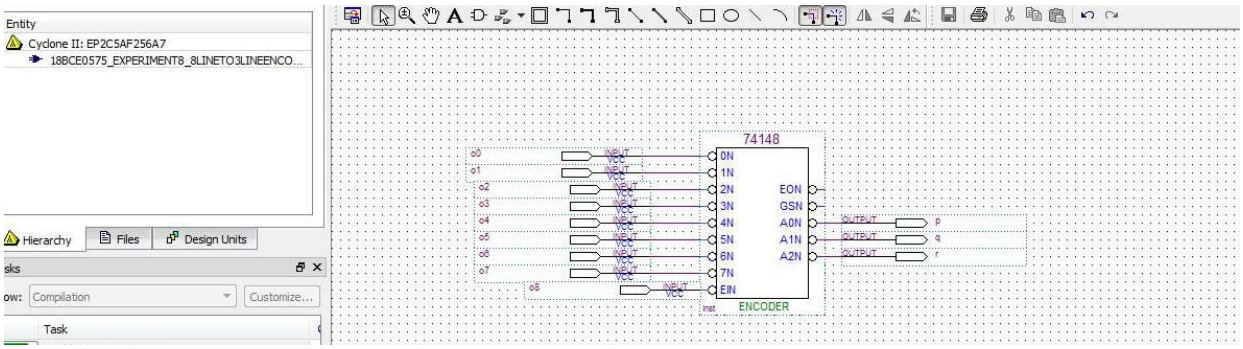
A0=A1+A3+A5+A7+A9

FINAL RESULT:



d. **AIM:** To design a 8 to 3 line priority encoder

CIRCUIT DIAGRAM:



TRUTH TABLE:

O0	O1	O2	O3	O4	O5	O6	O7	P	Q	R
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

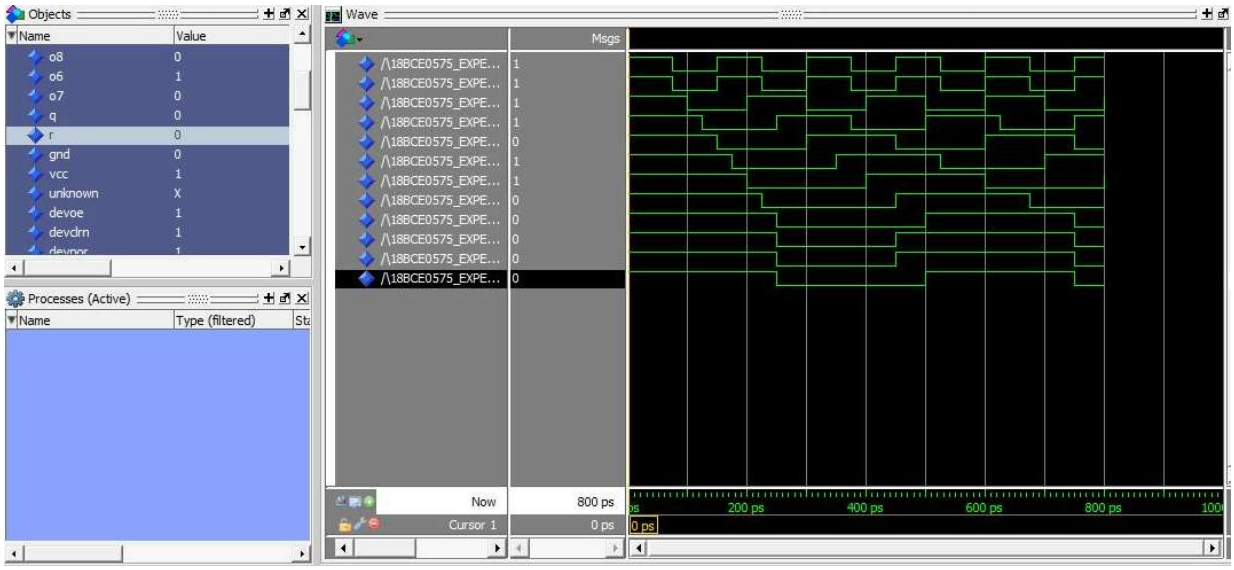
EXPRESSIONS:

P=O4+O5+O6+O7

Q=O2+O3+O6+O7

R=O1+O3+O5+O7

FINAL RESULT:



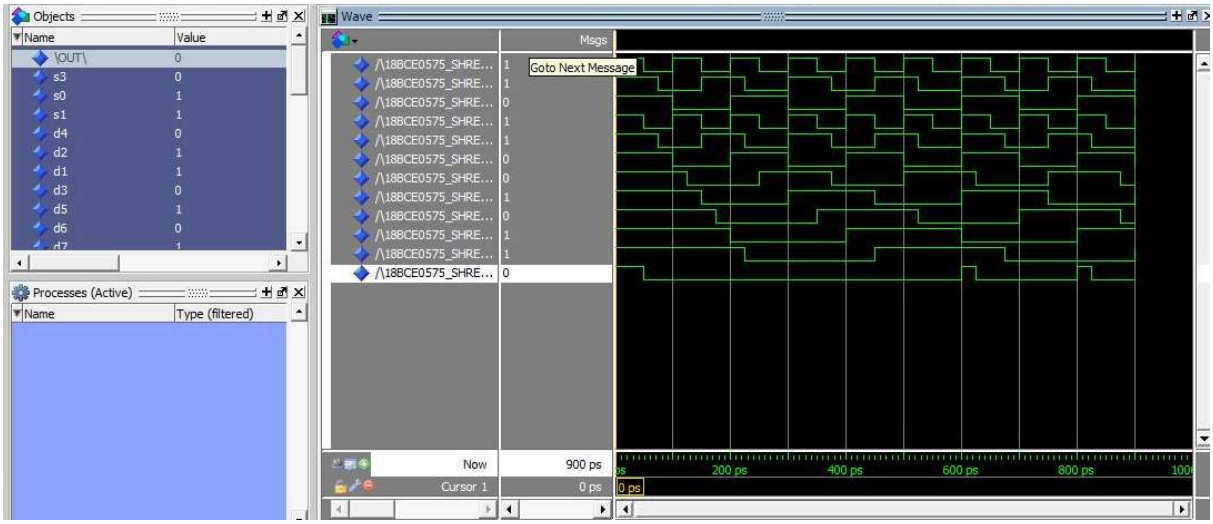
QUESTION 4

a. **AIM:** 8 to 1 mux using two 4 to 1 mux and one 2 to 1 mux.

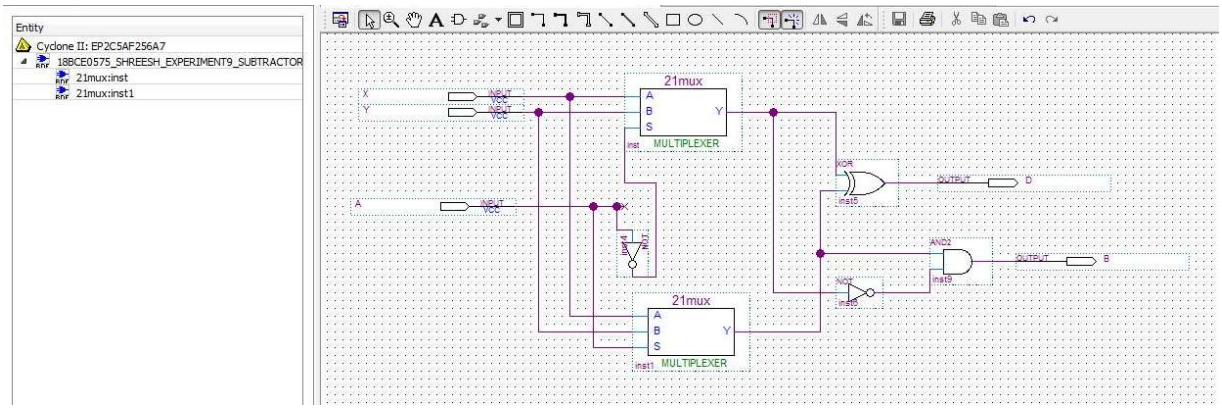
TRUTH TABLE:

S2	S1	S0	OUT
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

FINAL RESULT:



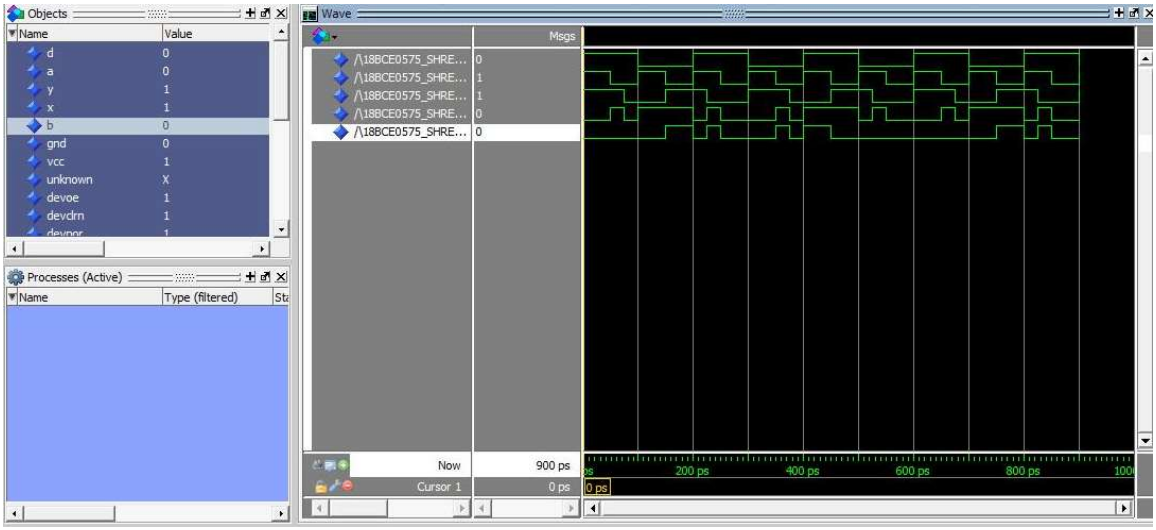
AIM: Design a circuit which perform X-Y if A=1 and Y-X if A=0 .



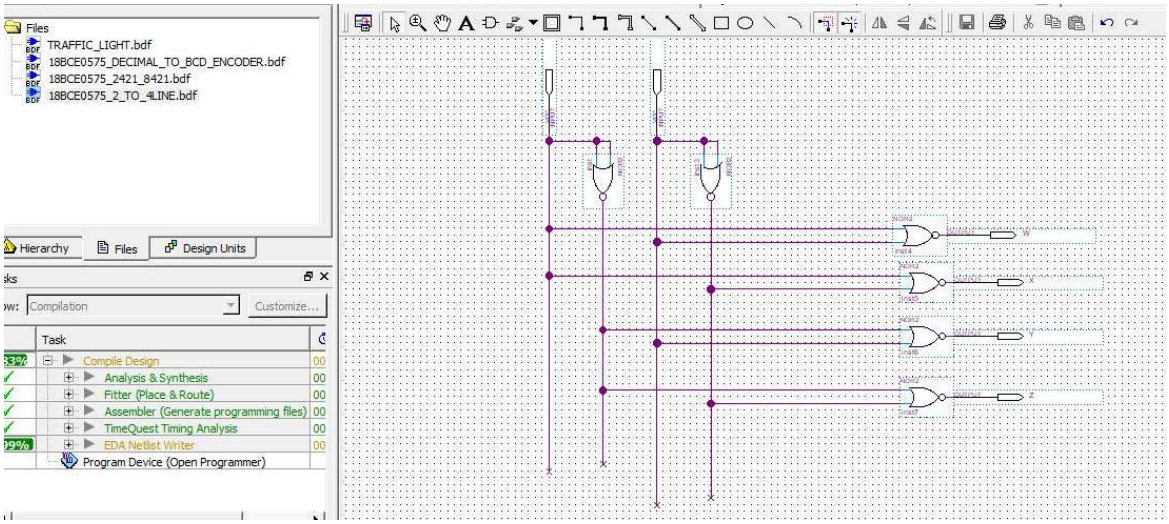
TRUTH TABLE:

A	X	Y	B	D
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1	0	0
1	0	0	0	0
1	0	1	1	1
1	1	0	0	1
1	1	1	0	0

FINAL RESULT:



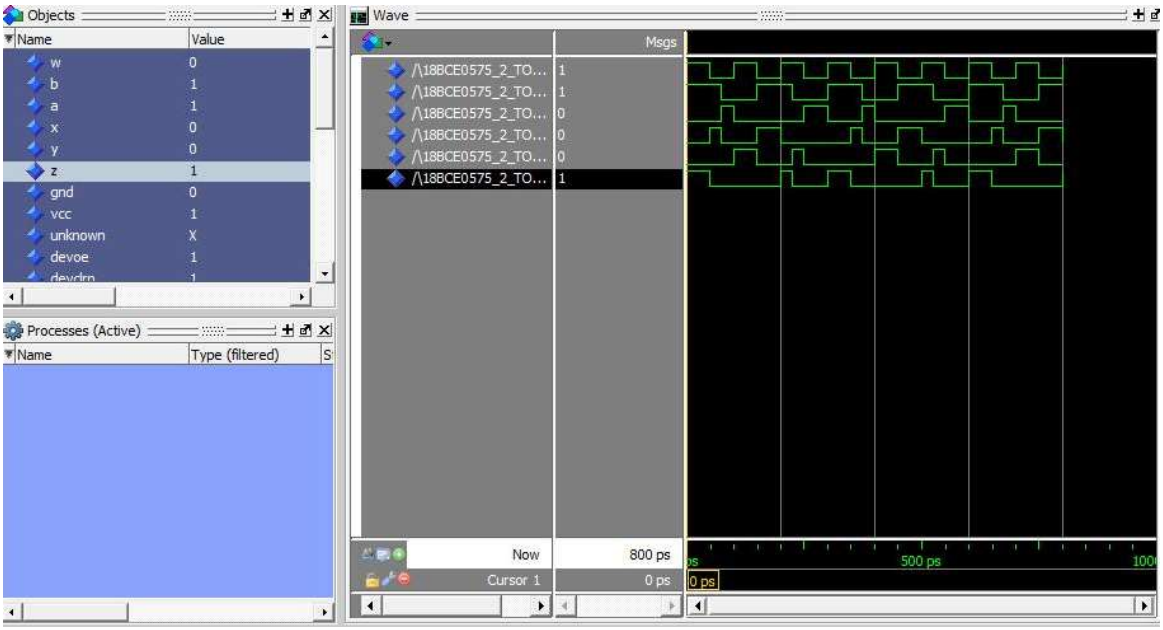
AIM: Design 2 to 4 line demux using NOR gates.



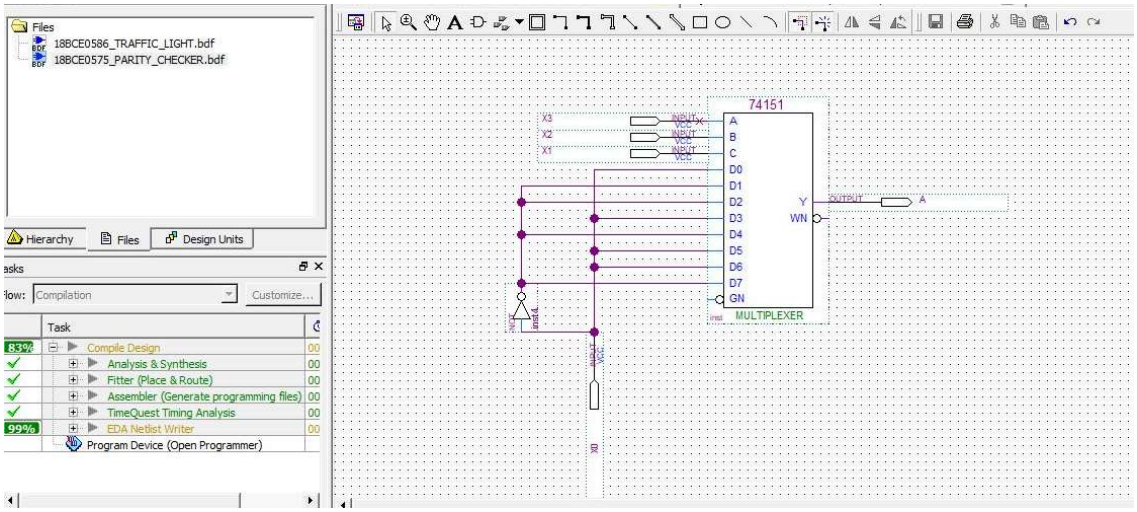
TRUTH TABLE:

A	B	W	X	Y	Z
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

FINAL RESULT:



AIM: Design a 4 bit even parity checker



TRUTH TABLE:

X3	X2	X1	X0	A	
0	0	0	0	0	X0
0	0	0	1	1	X0
0	0	1	0	1	X0’
0	0	1	1	0	X0’
0	1	0	0	1	X0’
0	1	0	1	0	X0’
0	1	1	0	0	X0
0	1	1	1	1	X0
1	0	0	0	1	X0’
1	0	0	1	0	X0’
1	0	1	0	0	X0
1	0	1	1	1	X0
1	1	0	0	0	X0
1	1	0	1	1	X0
1	1	1	0	1	X0’
1	1	1	1	0	X0’

FINAL RESULT: