DIGITAL LOGIC AND DESIGN LAB

EXPERIMENT-5

- **NAME: ANSHIL SETH**
- **REG NO.: 18BCI0173**
- **SLOT: L25+26**
- **SESSION: WINTER SEMESTER 2018-19**
- **FACULTY: PROF. LIJO V.P**

DATE: - 29Th March 2019

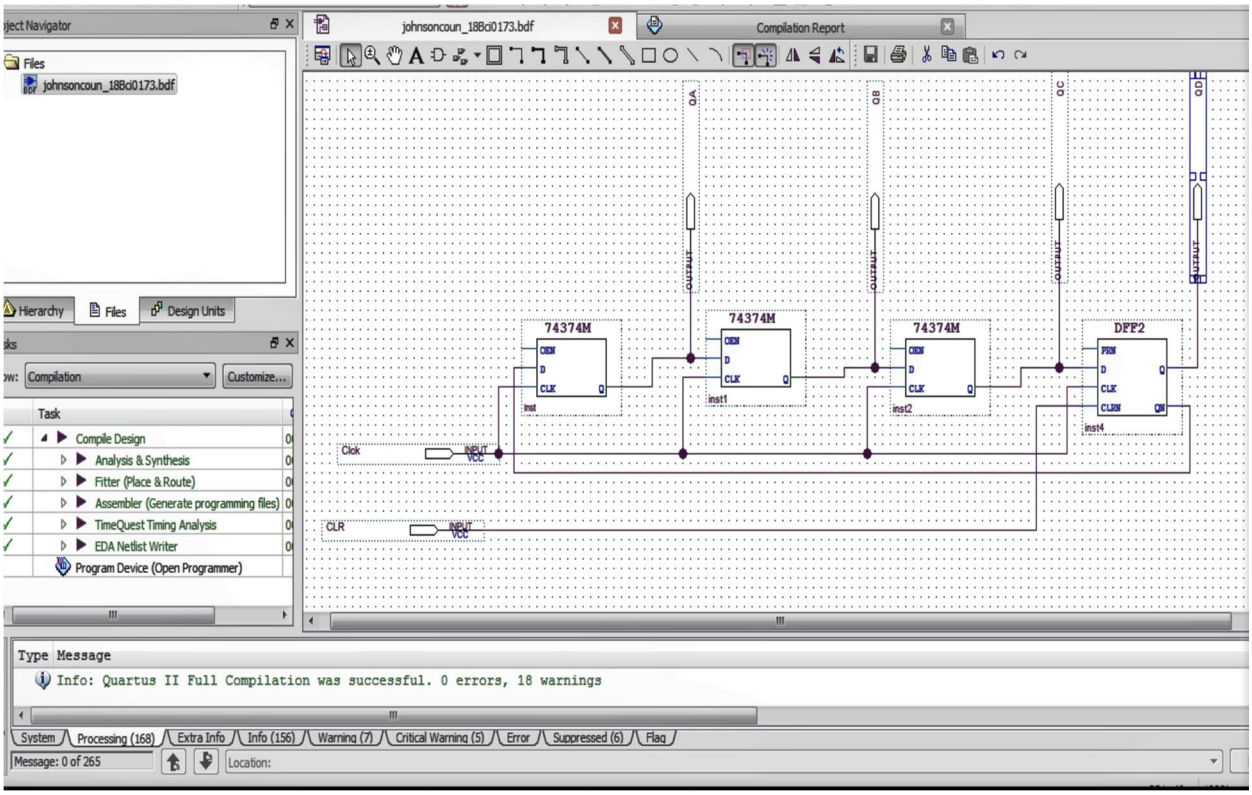
2.

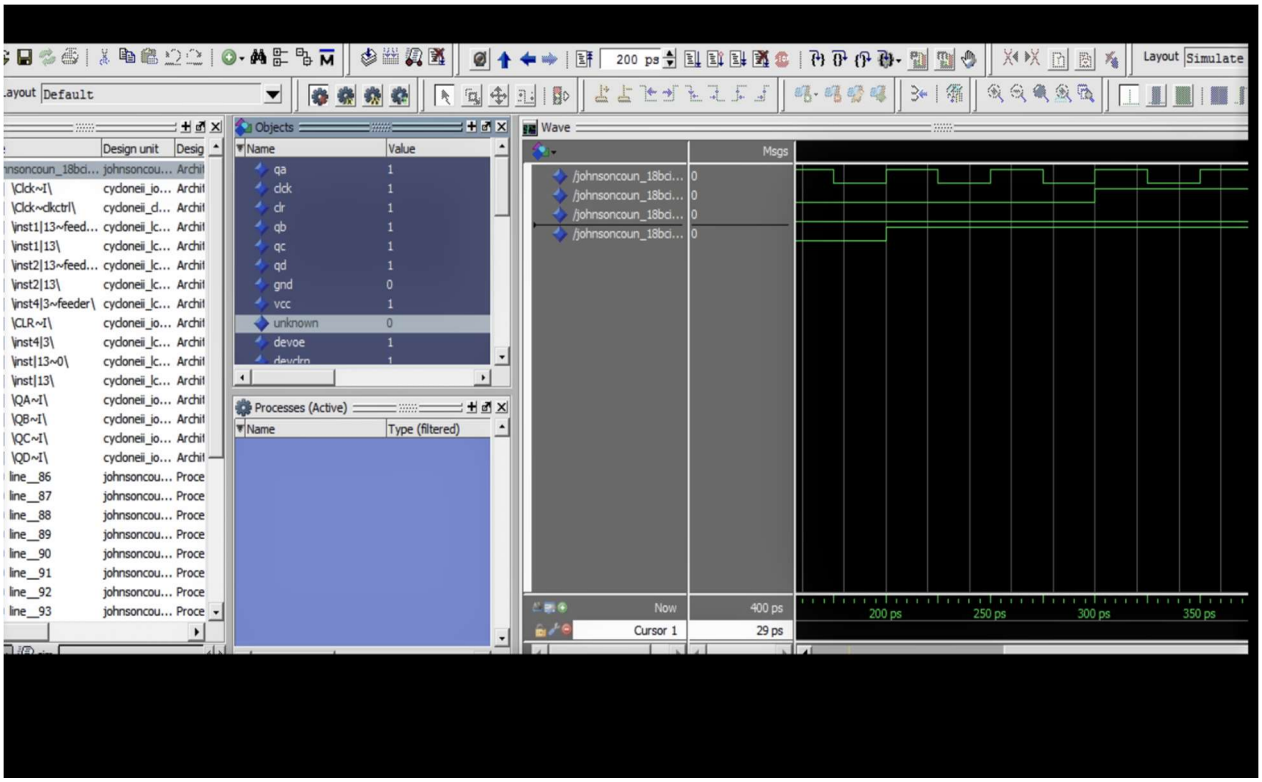
A. ***Design and implement four bit Johnson counter***

TRUTH TABLE: -

CLOCK NO.	FFA	FFB	FFC	FFD
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

CIRCUIT AND WAVEFORM: -





3.

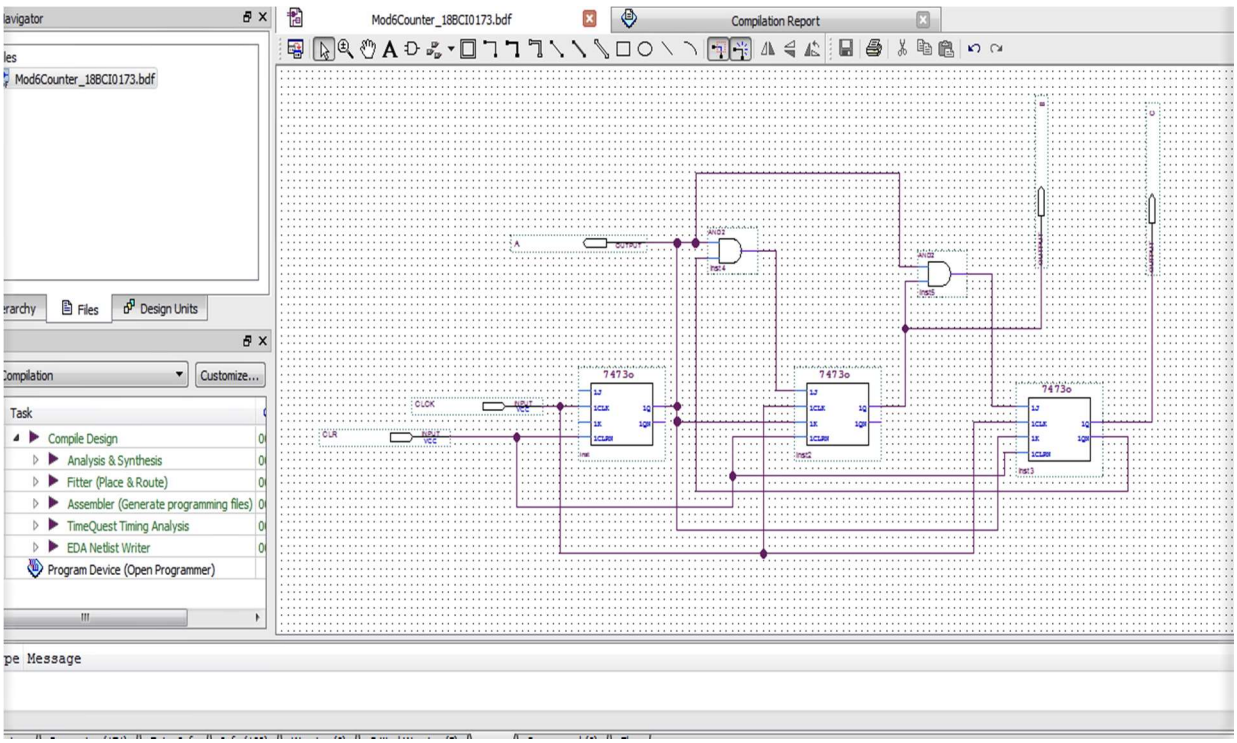
A. *Design a Mod-6 ripple counter.*

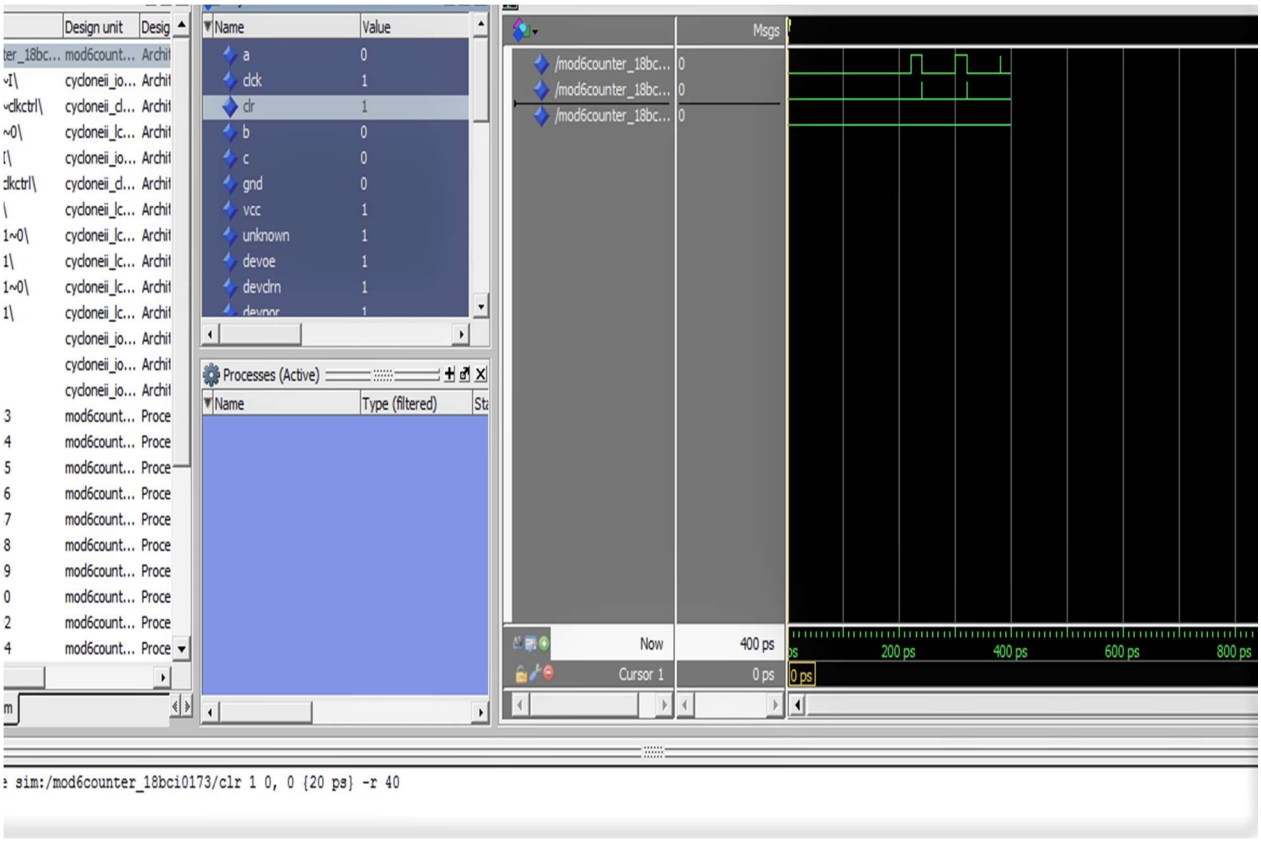
TRUTH TABLE: -

Q_C	Q_B	Q_A	Reset logic
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Fig1. Truth table of MOD 6 asynchronous counter

CIRCUIT AND WAVEFORM: -





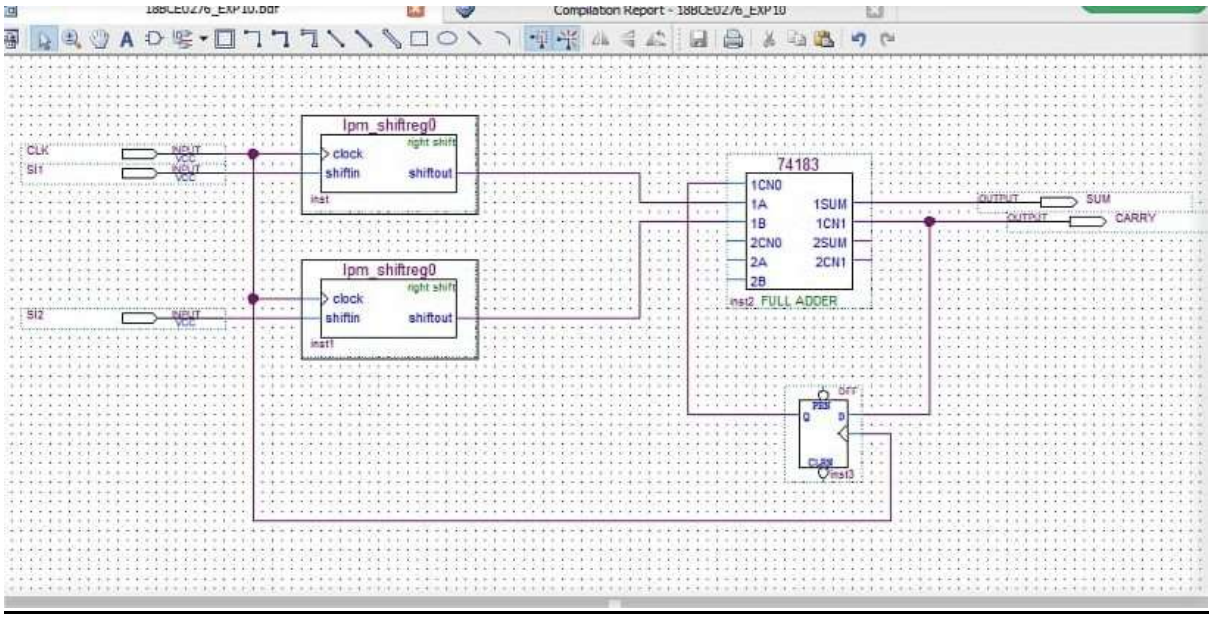
1.

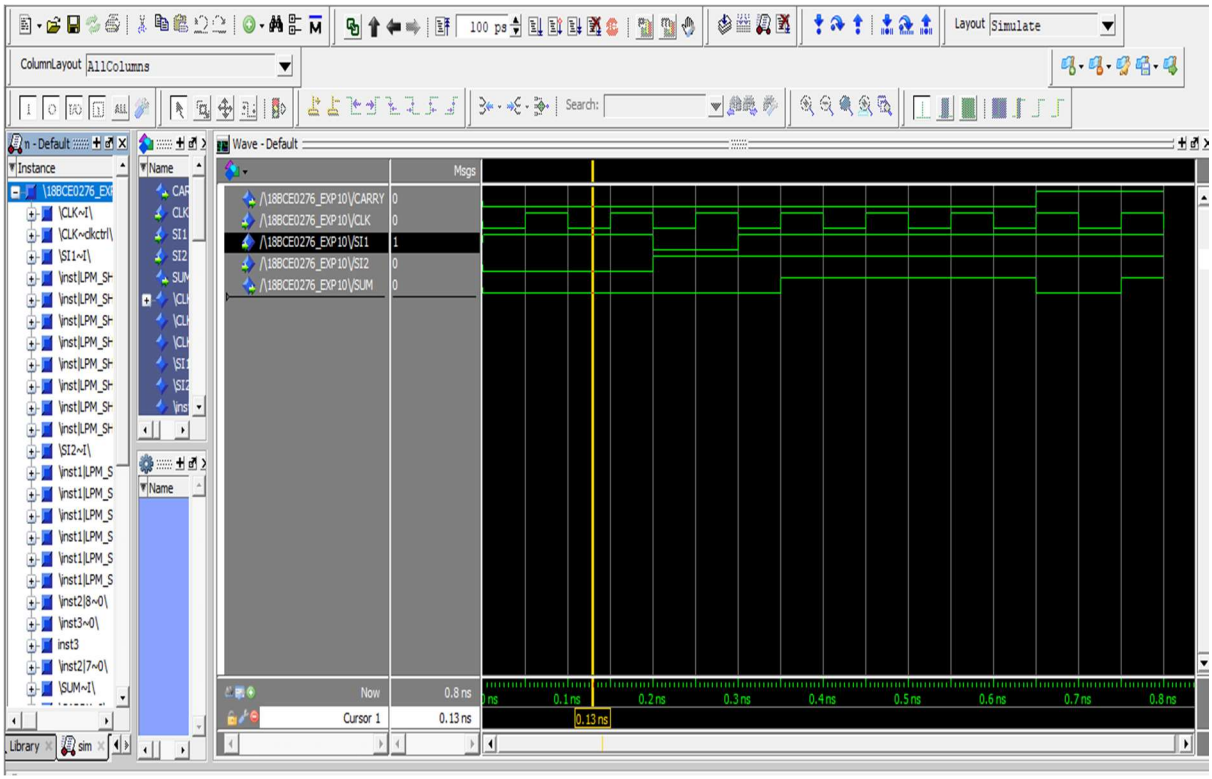
B. Implement a four bit serial adder using shift register

TRUTH TABLE: -

A	*B*	*S*	s_i	c_{i+1}
1011	0011	0000	0	1
0101	0001	1000	1	1
0010	0000	1100	1	0
0001	0000	1110	1	0

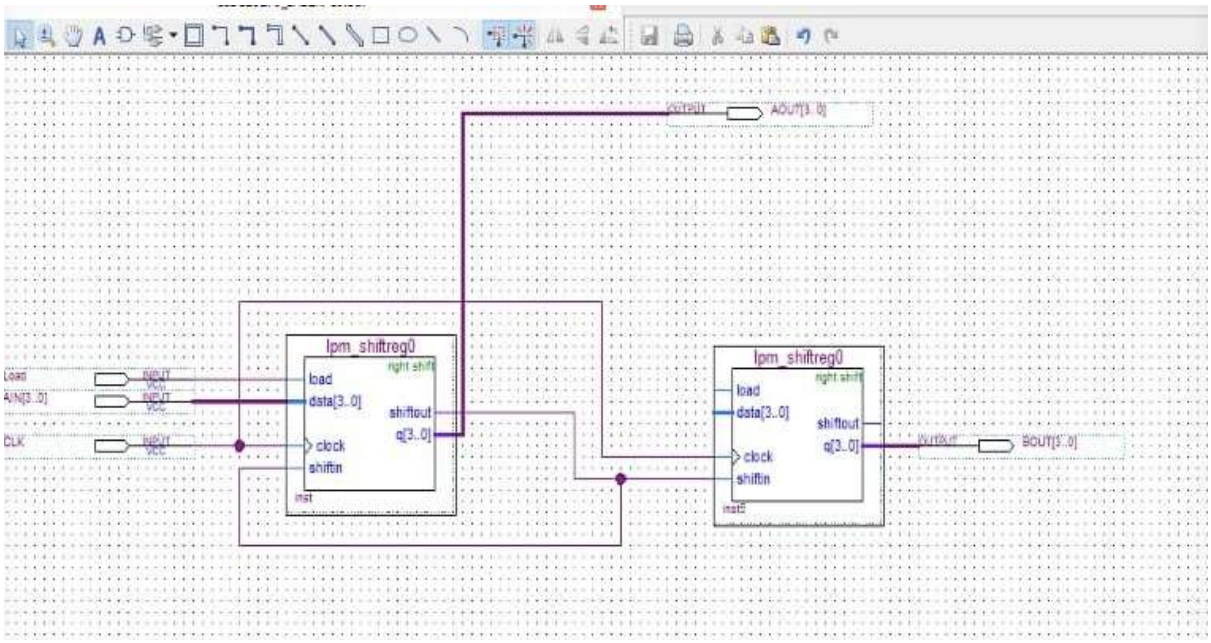
CIRCUIT AND WAVE DIAGRAM: -

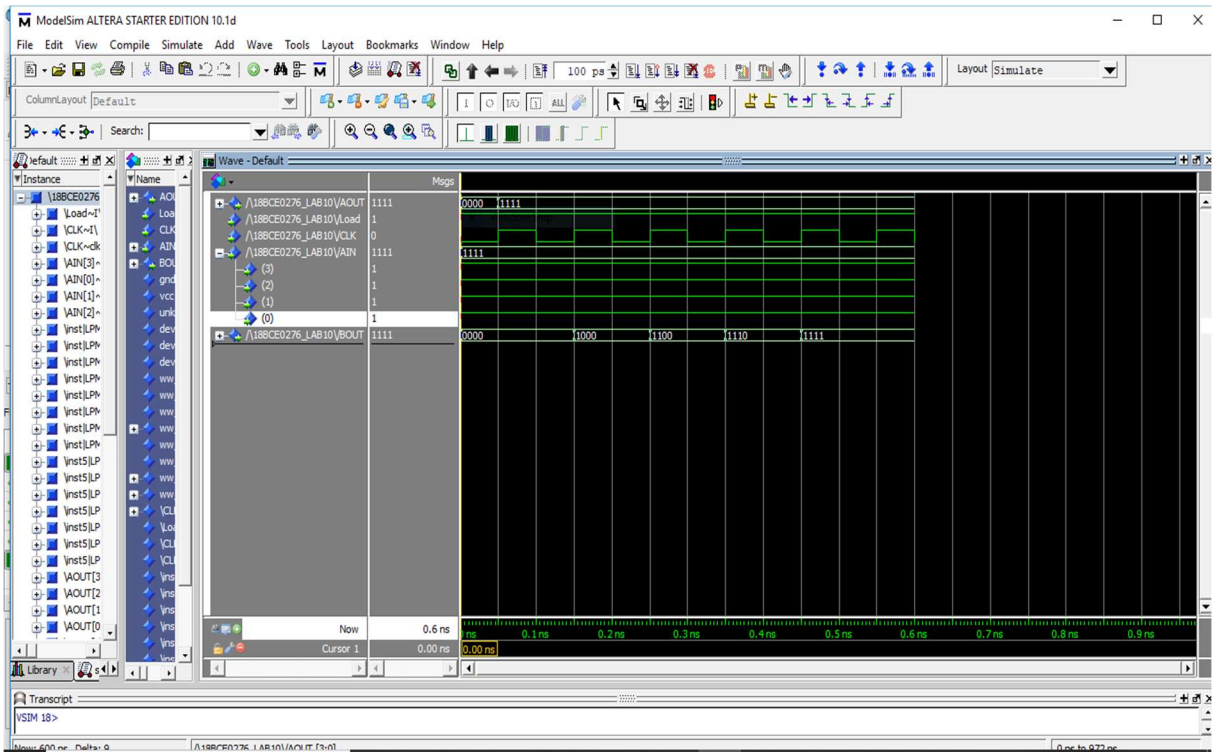




A. Transfer the contents of register 'A' to register 'B' in a serial manner using shift registers. The contents of the register 'A' need to be retained.

CIRCUIT AND DIAGRAM: -





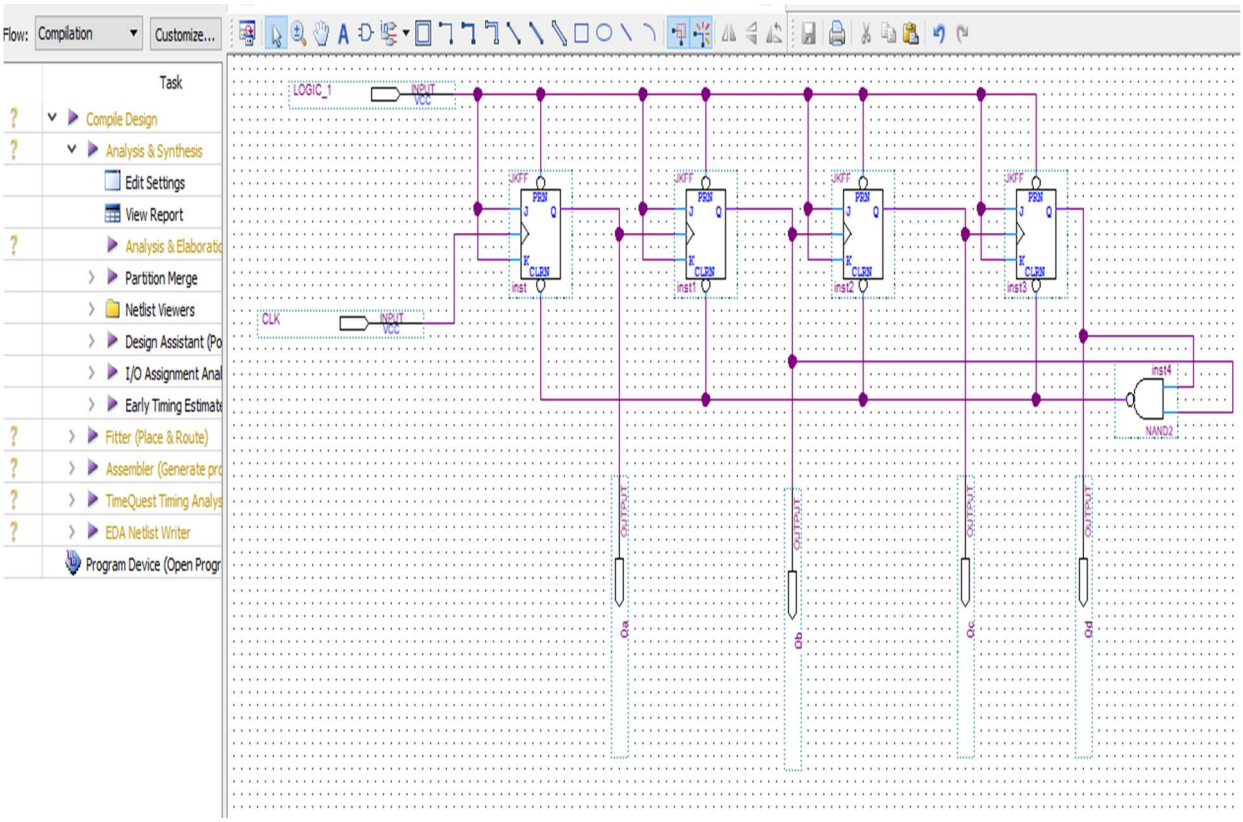
TRUTH TABLE: -

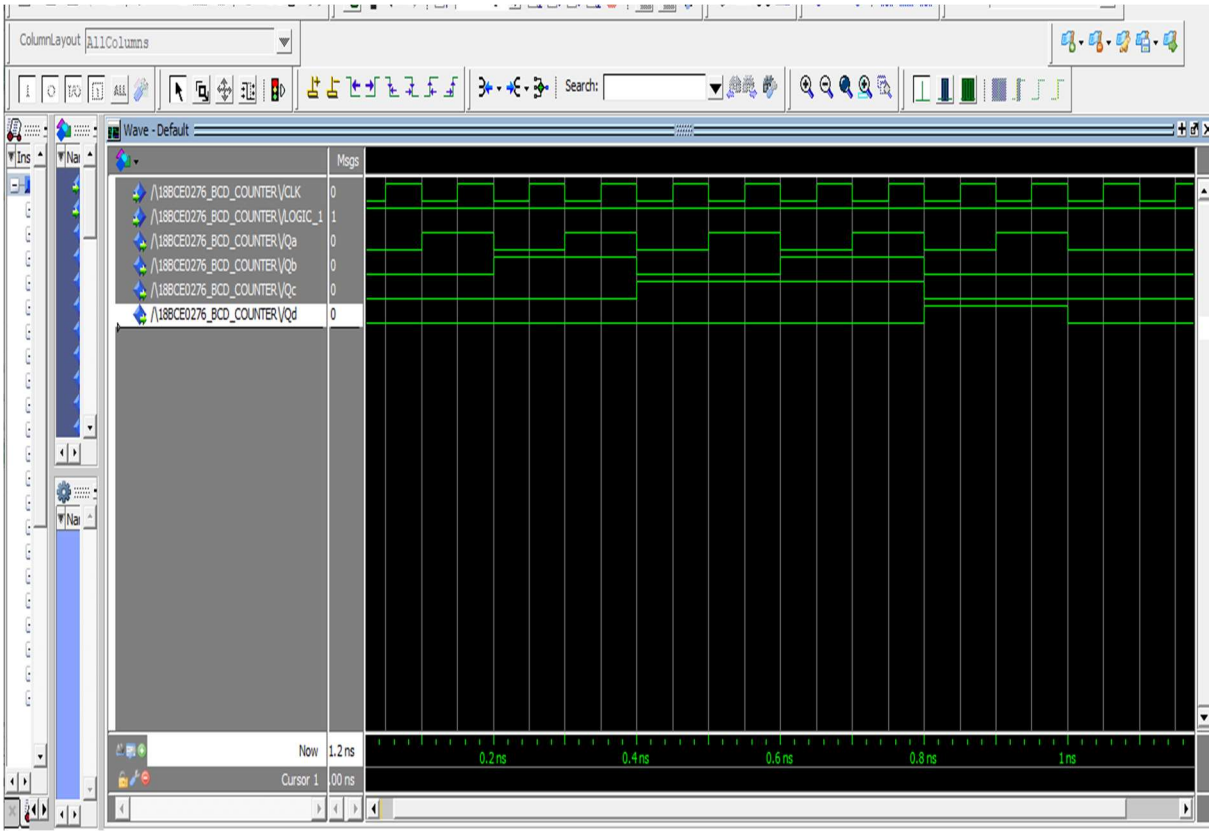
Clock Cycle	Data in	Q_1	Q_2	Q_3 = Data out
1	1	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	1	0	0
5	0	0	1	0
6	0	0	0	1

3.

B. ***Design and implement asynchronous BCD counter***

CIRCUIT AND WAVE DIAGRAM*: -*





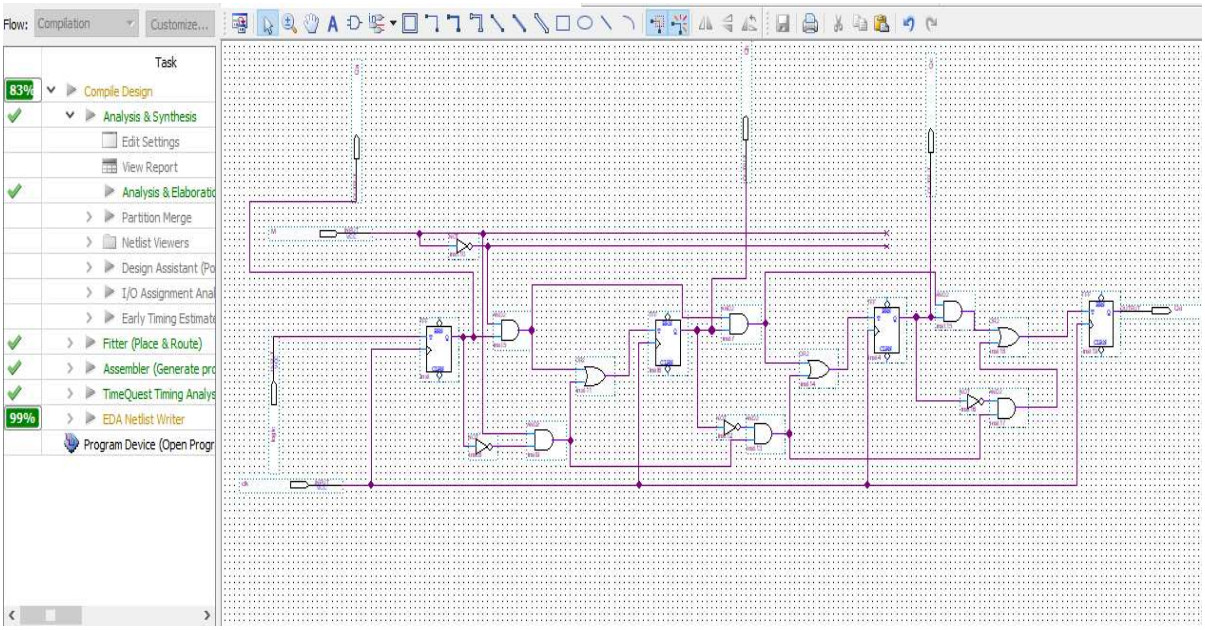
TRUTH TABLE: -

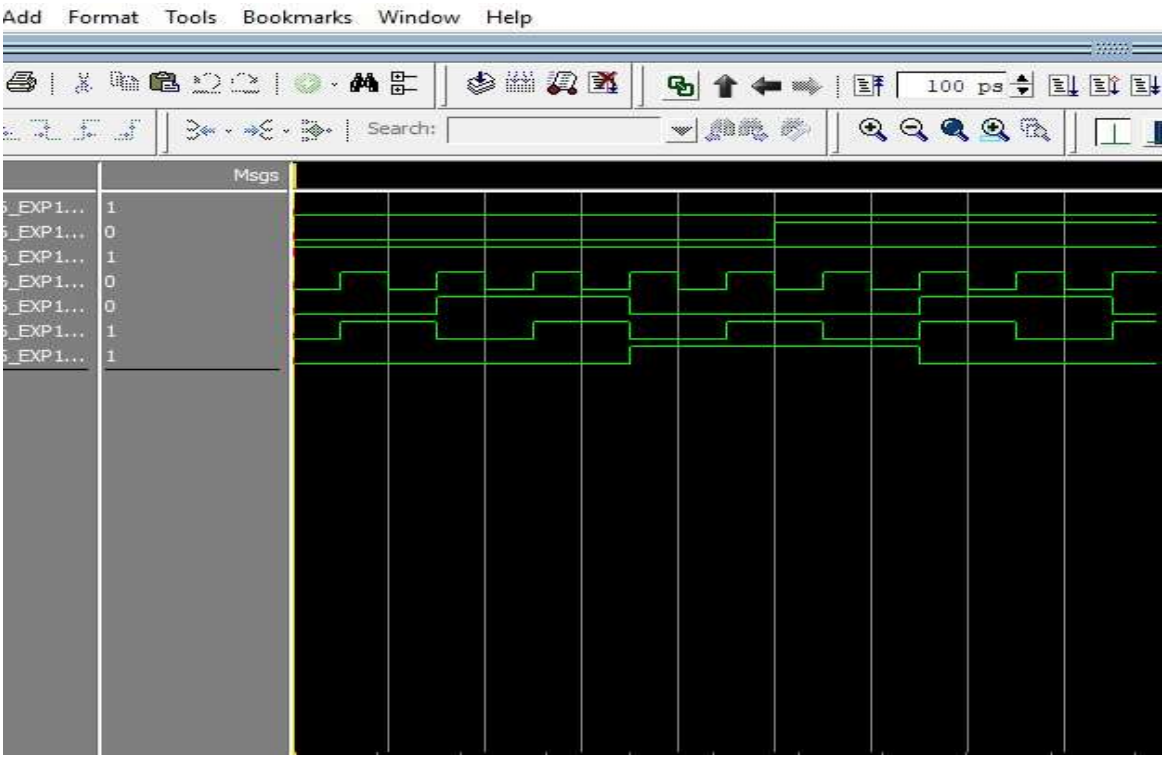
Clock Pulse	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

2.

B. Design and implement four bit synchronous up – down binary counter.

CIRCUIT AND WAVE DIAGRAM: -





TRUTH TABLE: -

Table 5.6.2								
CK	Q_3	Q_2	Q_1	Q_0	$\overline{Q_3}$	$\overline{Q_2}$	$\overline{Q_1}$	$\overline{Q_0}$
0	0	0	0	0	1	1	1	1
1	0	0	0	1	1	1	1	0
2	0	0	1	0	1	1	0	1
3	0	0	1	1	1	1	0	0
4	0	1	0	0	1	0	1	1
5	0	1	0	1	1	0	1	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	0	0
8	1	0	0	0	0	1	1	1
9	1	0	0	1	0	1	1	0
10	1	0	1	0	0	1	0	1
11	1	0	1	1	0	1	0	0
12	1	1	0	0	0	0	1	1
13	1	1	0	1	0	0	1	0
14	1	1	1	0	0	0	0	1
15	1	1	1	1	0	0	0	0

RESULT: -

Hence the above circuits are verified by the truth table and the wave diagram.

----------THANK YOU----------