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Version	1

Abstract

Simulating photovoltaic modules in a laboratory environment currently requires expensive and complex equipment, restricting research into this area to parties with substantial financial backing. In order to facilitate access to this area of research, a lower cost alternative to the existing expensive equipment is needed.

This report details our efforts in developing and building a device for this purpose. Its design is based around a microcontroller which handles IO tasks and implements two control loops for operating a pre-existing step-down converter in either constant current or constant voltage mode to generate an output voltage matching a dynamically programmable IV characteristics curve. The mathematics used to model the underlying physical behaviour allows emulation of multiple series-connected cells to generate more complicated solar panel behaviours.

Unfortunately, the device is not operational at this point as the step-down converter keeps being damaged with the current design.

TODO: Insert suspicions about causes

With more time available, we are confident that the cause of our issue would be found and fixed, and the device made operational as originally specified.

Contents

Versionsgeschichte

10th Oct 2015: `Version 0.1:` Einleitung & Disposition
2nd Jan 2015: `Version 0.2:` Translation to English

1 Introduction

Verifying the correct operation of equipment used for testing solar arrays is currently difficult in a controlled laboratory environment, as no affordable solutions for this exist on the open market. To address this issue, the aim of this project was the development of a device capable of emulating the behavior of a photovoltaic module. With this device, test equipment for photovoltaic modules can be verified to function as specified in a laboratory conveniently and affordably.

The primary characteristics of our device should be compactness (usable in a standard laboratory environment), the capability to emulate varying solar irradiation levels, being able to be used in series with other emulators, effiency with regards to power consumption and losses, and to emulate the characteristic curve of an actual PV module. A more detailed list of the technical requirements can be found in the specifications (see appendix `XXX (link to Lastenheft)`).

A microcontroller and a constant-current, constant-voltage step-down converter constitute the core of our device. The microcontroller performs IO operations and implements the regulation loop used to control the step-down converter, whereas the step-down converter generates the output voltage and output current corresponding to the desired operating point from a DC power supply. The entire design is based around a custom PCB, enabling us to optimise impedances of connections between critical components. Additionally, we can get very close in behavior to a potentially mass-produced product since trace lenghts, routing and component placement are crucial (see also section 6, beginning on page 20).

The device has a simple yet powerful user interface which can be controlled by a push-twist button and a modern OLED display. The device can also be remotely monitored and controlled from a PC via USB interface and custom software built on the Qt application framework and is compatible with all major operating systems [6]. Our device can emulate fairly complex configurations of cells thanks to an efficient use of computation resources and its powerful microprocessor.

Section 2 (p. 2ff) of this reports deal with the basic concept behind our solution. Component selection and PCB design are documented in sections 3 (p. 5ff) and 4 (p. 16ff), respectively, while section 5 is concerned with software (p. 18ff). Lastly, section 6 (p. 20ff) deals with testing the device including error analysis, and the conclusion can be found in section 7 on page 24.

2 Basic Concept

Underpinning our device is a microcontroller which is primarily responsible for handling I/O tasks (such as user interaction and the display) and controlling the step-down converter. Power delivery is realised with a prebuilt DC power supply unit.

With an eye towards potential serial production, we developed our own PCB. This allows tight control over impedances in the connections between critical components and brings the behavior of the prototype device much closer to a mass produced version than a breadboard solution could. This is because trace routing lengths and component placement are crucial factors, as is discussed in section 6 (p. 20ff), *Verification*.

Users can interact with our device either through a push-twist button and a display on the device itself or from a PC connected by USB using our software *Smooth* (section 5.6, p. 19ff).

2.1 Concept of Regulation Circuit

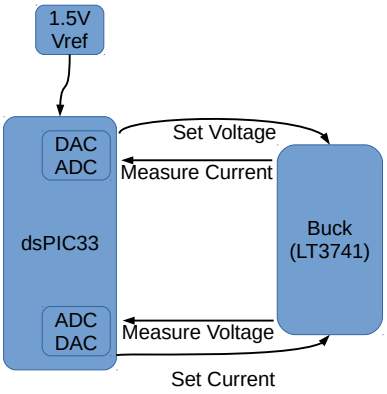

Figure 1: Block diagram of control circuit

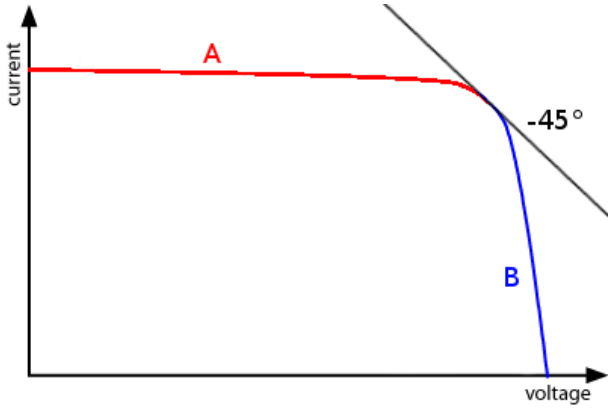

Figure 2: VI-Curve with −45° slope indicated

Emulation of the IV characteristic curve is achieved accurately by measuring both output voltage and output current. If the operating point is above the −45° slope ("A" in figure 2) then it is more accurate to operate the regulator in constant current mode. In contrast, if the operating point is below the −45° slope ("B" in figure 2) then it is more accurate to operate the regulator in constant voltage mode. A more detailed explanation can be found in section 5.4 on page 18.

2.2 Goals of the model

Our aim is to have a simple model, as usability is more important than accuracy. In other words, our model should have a small set of parameters, which can be easily determined by the user. Further it must respect solar irradiation, as we want to model how clouded skies or a partially covered module affects its output.

2.3 Model for one solar cell

make references work

As Basis for our model serves the single diode model of the ideal PV cell from [4] . The I-V characteristic of this circuit is

$$I = I_{pv} - I_o \left[\exp\left(\frac{V}{V_T}\right) - 1 \right] \tag{1}$$

where I_{pv} is the generated current, I_o is the diode current and V_T is the thermal voltage. All of these three parameters are dependent on the junction temperature, however to simplify our

model we assume that the temperature is equal to the nominal temperature $T_n = 298.15K$. The thermal voltage is defined with

$$V_T = akT/q \tag{2}$$

where T is the junction Temperature, k is the boltzman-constant, q is the electron charge constant and a is the diode ideality factor, which lies usually around 1.2 for silicium substrates. This gives us $V_T \approx 30.8mV$ for one cell. The current generated by the cell is defined as

$$I_{pv} = (I_n + K_I \Delta_T) \frac{G}{G_n} \tag{3}$$

with I_n being the nominal Current and G and G_n being the actual respectively the nominal solar irradiation. For our model we will set $I_n \approx I_{sc}$ and again assume that $T = T_n$ giving us $\Delta_T = 0$ which simplifies this formula to

$$I_{pv} = I_{sc} \frac{G}{G_n} \tag{4}$$

Finally, the diode leakage current at the nominal temperature [I] is

$$I_o = \frac{I_{sc}}{e^{V_{oc}/V_T} - 1} \tag{5}$$

If we put (5) and (4) back in (1) we get

$$I = I_{sc} \left(\frac{G}{G_n} - \frac{e^{\frac{V}{V_T}} - 1}{e^{\frac{V_{oc}}{V_T}} - 1} \right) \tag{6}$$

If we now assume $V_{oc} > 5 * V_T$ we can say that $e^{\frac{V_{oc}}{V_T}} - 1 \approx e^{\frac{V_{oc}}{V_T}}$ and our final formula becomes

$$I = I_{sc} \left(\frac{G}{G_n} - e^{\frac{V - V_{oc}}{V_T}} \right) \tag{7}$$

2.4 Model for multiple Cells in Series

If the solar irradiation is the same for every cell in series, then the whole array can also be simulated with (7), but V_{oc} and V_T get multiplied by the number of cells.

If the irradiation isn't the same for all cells, for instance because one cell is shaded, a more complex model must be used.

Figure 3 shows how varied the characteristics of a shaded PV-module can be and how bypass diodes affect them. In our model we can imitate the I-V curve of an array with a shaded cell and no bypass diode by setting $V_T = V_{oc}$.

The "stairway" characteristic shown in figure 4 emerges when two or more modules, which are exposed to different irradiation, get connected in series with bypass diodes. To simulate this behaviour, we take a number of curves with decreasing short circuit current and increasing open circuit voltage and determine which curve is applicable by checking what curve returns the maximum current for the given voltage.

fix

[I] For other temperatures please see [4]

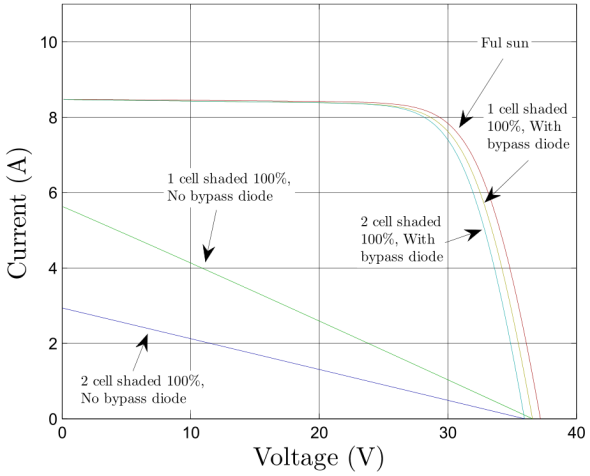

Figure 3: I-V curves for different configurations and shaded cells [**?**]

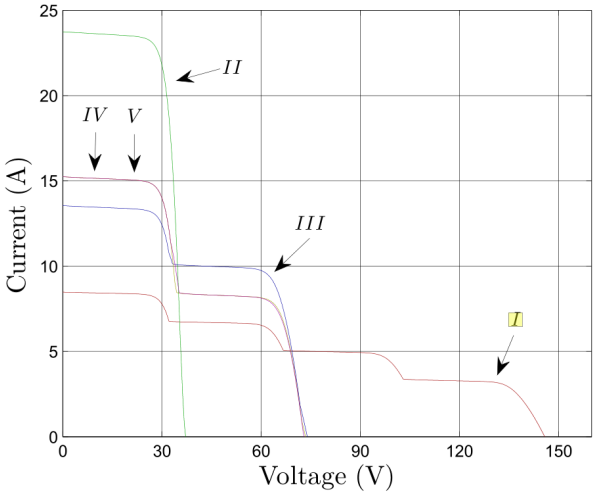

Figure 4: The typical characteristic of modules connected in series or in parallel

3 Component Selection

In this section, the selection of critical components is discussed in detail. Mainly, this concerns the microcontroller, the power delivery (both external and internal) and the circuitry used in conjunction with the step-down converter. A more comprehensive list of components can be found in appendix `TODO` on page `TODO`.

- Was sind die Anforderungen an die Stromversorgung?
- Weshalb wird der dsPIC33EP-Chip verwendet?
- Weshalb wird der LT3741 verwendet?
- Wie erfolgt die Ansteuerung des LT3741?
- Weshalb wurde das verwendete LCD gewählt?
- Wie wird die serielle Schnittstelle realisiert?

3.1 Microcontroller

The choice for our miroprocessor was comparatively straight-forward. Microchip was chosen as manufacturer because one of our team members was already familiar with their products. This enabled us to more quickly start becoming productive instead of the entire team needing to familiarise itself with the tools and architecture of the microcontroller from scratch.

Additionally, Microchip provides good developer tools for free. For selecting a specific model, the following criteria eventually lead us to the `dsPIC33EP16GS506`:

- 120 MHz clock (60 MIPS): High enough to allow a fast control loop.
- 2 ADCs and 2 DACs with external voltage reference: Required by the control model we use (see section `TODO`.
- PGA (Programmable Gain Amplifier) (64 × analog pre-amplifier): Allows measuring the small differential voltages which occur in our device and are used in regulating the step-down converter.
- Low cost of 4 CHF

3.2 36V Power Supply and Mains Input

The maximum required output power of our device was roughly calulated as $24\,\mathrm{V} \cdot 3\,\mathrm{A} = 72\,\mathrm{W}$. Assuming an efficiency of $\eta \approx 90\,\%$ an 80 W power supply is required.

The design and construction of a custom power supply would have consumed too much time and resources. Instead, we opted for an external power supply which can be mounted inside the housing. The selected power supply is capable of supplying 28 V at 75 W and can be seen in figure 5.

The device can be plugged into a power outlet by means of an IEC 60320 C13 socket seen in figure 6. The socket has a built-in fuse as well as a built-in mains filter, which will reduce high frequency coupling from the device back into the mains.

A rocker switch (figure 7) is connected in series with the socket and the power supply, allowing for the end user to cut power at any time.

TODO: Show photo of wiring in housing

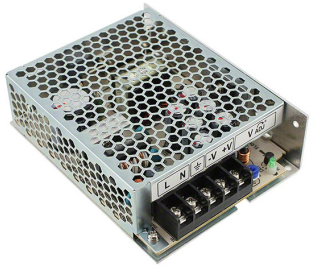

Figure 5: External PSU

Figure 6: Power Entry Module

Figure 7: Rocker Switch

3.3 Voltage Rails

In order to power the components used in this design, hree different voltage levels (known as voltage *rails*), which are 28 V, 5 V and 3.3 V respecitvely. Each rail has different requirements concerning noise, power and efficiency.

First and foremost, the maximum current of each voltage rail must be approximately determined. This information is crucial for selecting appropriate voltage regulators.

The most power-hungry component on the 3.3 V rail is clearly the dsPIC33 microcontroller and LEDs. According to the datasheet, the microcontroller will consume $0.5\,\text{mA}\,\text{MHz}^{-1}$. Since the microcontroller will be clocked at 120 MHz, the minimum current can be calculated with the following equation.

$$I_{dsPIC} = 0.5\,\text{mA}\,\text{MHz}^{-1} \cdot 120\,\text{MHz} = 60\,\text{mA} \tag{8}$$

The other significant power-hungry components are the four LEDs connected to the dsPIC33 microcontroller. Each consume 15 mA. The total current consumption of the 3.3 V rail is therefore roughly:

$$I_{3.3\,\text{V}} = I_{dsPIC} + 4 \cdot 15\,\text{mA} = 120\,\text{mA} \tag{9}$$

The 3.3 V rail derives it's voltage from the 5 V rail. Additionally, the OLED display is powered by the 5 V rail, which, according to the datasheet, draws a maximum current of 135 mA. The total current consumption of the 5 V rail will approximately be:

$$I_{5\,\text{V}} = I_{3.3\,\text{V}} + 135\,\text{mA} = 255\,\text{mA} \tag{10}$$

A decision for each voltage rail must be made. Do we use a switch-mode power regulator or a linear regulator? The general trade-off is that swith-mode regulators have a very high efficiency, but due to the nature of how they transform voltages, they produce a lot more jitter on the output. In contrast, a linear regulator produces almost no jitter – in fact, it even dampens incoming jitter by a substantial amount – however, the linear regulator has very poor efficiency since it just "burns" the excess voltage and produces a lot of heat, making it a poor candidate for transforming between larger voltage differences.

The 28 V rail is already taken care of, since that's precisely the voltage the external power supply provides.

Seeing as there is a very large voltage difference between 28 V and the next lower rail, 5 V, a switch-mode regulator is clearly the only sane choice to be made for powering the 5 V rail due

to efficiency reasons. The diagram of this circuit is illustrated in figure 8. There is little reason to discuss the selection of components of this circuit in great detail; It's using a standard configuration according to the datasheet. The regulator was chosen based on the current requirement $I_{5\,\mathrm{V}}$ and is capable of supplying a maximum current of 750 mA.

All digital circuitry, such as the micro controller, operates at 3.3 V. It is particularly important for the 3.3 V rail to have as little noise/jitter as possible. This requirement stems from the fact that the analog-to-digital (ADC) conversions and digital-to-analog (DAC) conversions derive their reference voltage from the 3.3 V rail. Any noise on this rail could impact the accuracy of these conversions and could result in lower accuracy of the final, regulated output voltage of the device itself. For this reason we opted for a linear regulator to power the 3.3 V off of the 5 V rail. The circuit is illustrated in figure 8. This regulator was also chosen based on the current requirement $I_{3.3\,\mathrm{V}}$ and is capable of supplying a maximum current of 1 A.

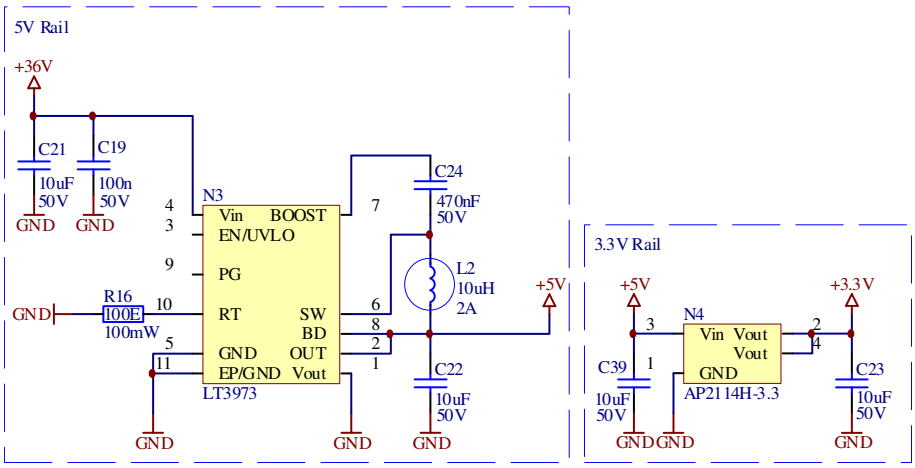

Figure 8: Speisung für 5V mittels Abwertswandler (links) und Speisung für 3.3V mittels Linearregler (rechts)

3.4 LT3741

There are many reasons why the LT3741 was chosen to regulate the output voltage of this device. The most important reasons are listed here.

- **Re-inventing the wheel.** Switch-mode regulators aren't new technology. They've been studied and perfected over decades by many engineers. For this reason we decided against building a regulator descretely and instead opted to use an existing regulator if available.
- **Voltage and current requirements.** The device is specified to output voltage levels between 0 V and 24 V and current levels between 0 A and 3.5 A. Further, the ripple voltage is specified to be ≤ 300 mV and the ripple current is specified to be ≤ 100 mA. The LT3741 fulfills all of these requirements.
- **The importance of power absorption.** Most switch-mode regulators are only able to *supply* power, but are incapable of *absorbing* power. Because our device may be connected in series (or parallel) with other power supplies, it must have the ability to absorb power too (which is the case if, say, it were connected to a voltage source outputting a higher voltage level than our own). A so-called *synchronous converter* possesses this property and the LT3741 is one of them.
- **Control inputs.** The LT3741 was chosen because it has dedicated input control pins for directly manipulating the regulated output current. This makes the design a lot simpler, because no complicated additional circuitry is required.

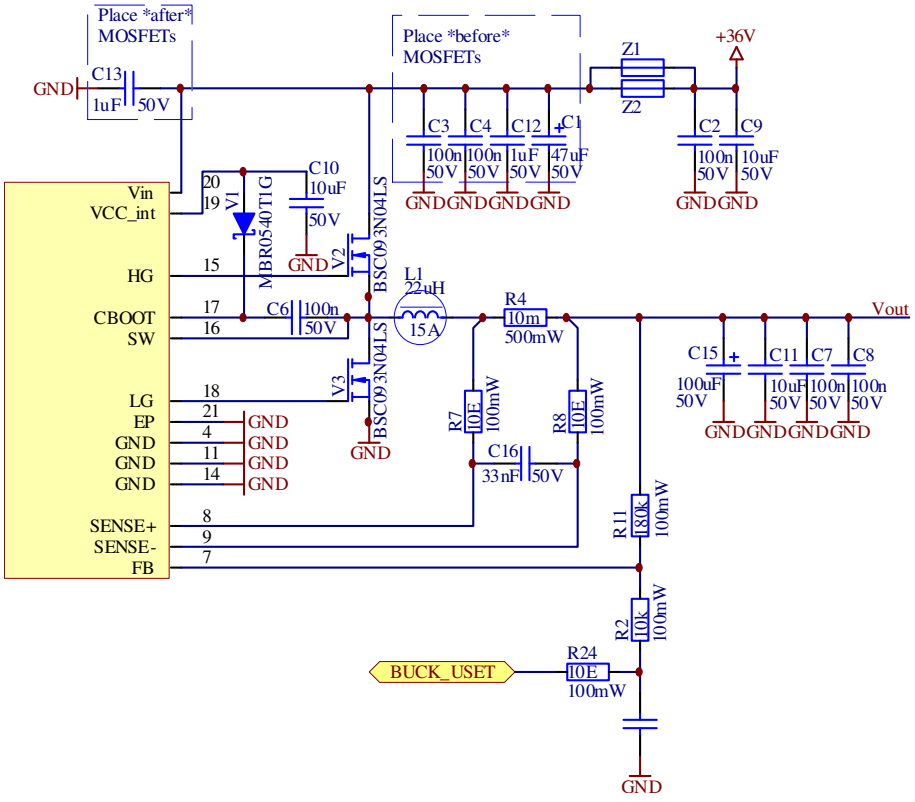

Figure 9: Herzstück des Projektes: Aufbau des LT3741 CVCC Synchronwandler

With the LT3741 selected, the selection of components required to control the LT3741 are discussed next.

3.4.1 Bypass Capacitors

The LT3741 is powered by the 28 V rail, which can be seen in figure 9 in the top right. Because the LT3741 consumes high amounts of power in very high frequent, short intervals (caused by the switching of the MOSFETs), the LT3741 is keen to feed high frequency disturbance back into the 28 V rail, which, if not handled correctly, could cause disturbances in the rest of the circuit. As a countermeasure we used a multitude of different ceramic and electrolytic bypass capacitors in parallel to help reduce EMI. Additionally, we used ferrite beads placed in series with the supply, which will absorb any high frequency feedback.

3.4.2 Switching Frequency

There is a tradeoff when selecting the switching frequency f_S. The higher f_S is selected, the lower the output ripple voltage will be, but the higher the power consumption will be (caused by switching losses). Generally, one will want to maximise f_S.

Due to all of the factors depending on f_S, it is only possible to determine this value imperically. We found a value of $f_S \approx 800\,\text{kHz}$ to be best suitable. In the rest of the calculations, f_S is assumed to be 1 MHz to allow for some leeway.

The switching frequency f_S is programmed by using a specific resistor on one of the inputs of the LT3741.

3.4.3 Inductor Selection

The size of the inductor L_1, as illustrated in figure 9, was calculated using formula 11

$$L_1 = \left(\frac{V_{in} \cdot V_{out} - V_{out}^2}{0.3 \cdot f_S \cdot I_O \cdot V_{in}} \right) = 6\,\mu\text{H} \tag{11}$$

where V_{in} is the input voltage 28 V, V_{out} is the output voltage at peak power (which exists at $V_{out} = 14\,\text{V}$), f_S is the switching frequency 1 MHz and I_O is the maximum output current, assumed to be $I_O = 5\,\text{A}$ for some additional leeway.

We ended up selecting a larger inductor of $L_1 = 22\,\mu\text{H}$ to further decrease ripple current.

In addition to the value of the inductor, the maximum current rating, DCR, and saturation current are also important factors to consider. The maximum current of the inductor is calculated using formula 12

$$I_{L_{1_{peak}}} = I_O + \left(\frac{V_{in} \cdot V_{out} - V_{out}^2}{2 \cdot f_S \cdot L_1 \cdot V_{in}} \right) = 5.2\,\text{A} \tag{12}$$

Where L_1 is the value of the selected inductor, 22 µH. The saturation current of the inductor was sized factor 1.2 higher than the peak current.

$$I_{L_{1_{saturation}}} = 1.2 \cdot I_{L_{1_{peak}}} \tag{13}$$

A list of candidates matching the above parameters are listed in table 1.

Table 1

Digikey	Price (CHF)	Inductance (µH)	DCR (Ω)	Ohmic Loss (W)
732-4237-1-ND	8.03	22	0.007	0.175
732-2179-1-ND	6.4	47	0.0335	0.8375
732-2177-1-ND	6.4	22	0.0146	0.365

It is clear that the one with the lowest DCR will be the most optimal. The one highlighted in grey is the one we chose.

3.4.4 MOSFET selection

In contrast to a non-synchronous regulator, this design uses two complementary MOSFETs V_2 and V_3, where V_3 acts as an active replacement for the free wheeling diode typically found in non-synchronous designs. As mentioned earlier, a crucial feature of this device is the ability to *absorb* power. V_3 makes this possible because it is able to regulate current in the opposite direction through the inductor L_1.

When selecting switching MOSFETs, the following parameters are critical in determining the best devices for a given application: Q_G (Total Gate Charge), $R_{DS_{(on)}}$ (On-Resistance), Q_{GD} (Gate to Drain Charge), Q_{GS} (Gate to Source Charge), R_G (Gate Resistance), V_{GS} (gate-to-source voltage), V_{DS} (drain-to-source-voltage), $I_{D_{max}}$ (peak drain current) and $V_{GS_{THR}}$ (gate threshold voltage).

The maximum drain current is equal to the previously calculated peak inductor current $I_{L_{1_{peak}}}$ in equation 12.

$$I_{D_{max}} = I_{L_{1_{peak}}} = I_O + \left(\frac{V_{in} \cdot V_{out} - V_{out}^2}{2 \cdot f_S \cdot L_1 \cdot V_{in}} \right) = 5.2\,\text{A} \tag{14}$$

where V_{in} is the input voltage 28 V, V_{out} is the output voltage at peak power (which exists at $V_{out} = 14\,\text{V}$), f_S is the switching frequency 1 MHz, L_1 is the value of the selected inductor (22 µH) and I_O is the maximum output current, assumed to be $I_O = 5\,\text{A}$.

The maximum drain-to-source voltage V_{DS} must be greater than the input voltage $V_{in} = 28\,\text{V}$, including transients. We selected MOSFETs with $V_{DS} = 40\,\text{V}$.

The signals driving the gates of the MOSFETs have a maximum voltage of 5 V with respect to the source. During start-up and recovery conditions, the gate drive signals may be as low as 3 V. To ensure that the LT3741 recovers properly, the maximum gate threshold voltage should be less than 2 V. For a robust design, the maximum gate-to-source voltage V_{GS} should be greater than 7 V.

Power losses in the MOSFETs are related to the on-resistance $R_{DS(on)}$; the transition losses related to the gate resistance R_G; gate-to-drain capacitance Q_{GD} and gate-to-source capacitance Q_{GS}. Power loss to the on-resistance is an Ohmic loss, $I^2 R_{DS_{(on)}}$. The power loss in the high side MOSFET V_2 can be approximated with formula 15.

$$\begin{aligned} P_{LOSS} &= (\text{ohmic loss}) + (\text{transission loss}) \\ &\approx \left(I_O^2 \cdot R_{DS_{(on)}} \cdot \rho_T\right) + \left(\frac{V_{in} \cdot I_O}{5\,\text{V}} \cdot (Q_{GD} + Q_{GS}) \cdot (2 \cdot R_G + R_{PU} + R_{PD}) \cdot f_S\right) \end{aligned} \tag{15}$$

where ρ_T is a temperature-dependant term of the MOSFET's on-resistance. Using 70 °C as the maximum operating temperature, ρ_T is roughly equal to 1.3. R_{PD} and R_{PU} are the LT3741 high side gate driver output empedance, 1.3 Ω and 2.3 Ω respectively.

Another power loss related to switching MOSFET selection is the power lost to driving the gates. The total gate charge, Q_G, must be charged and discharged each switching cycle. The power is lost to the internal LDO within the LT3741. the power lost to the charging of the gates is:

$$P_{LOSS\_LDO} \approx ((V_{in} - 5\,\text{V}) \cdot (Q_{GLG} + Q_{GHG}) \cdot f_S \tag{16}$$

where G_{GLG} is the low side gate charge and Q_{GHG} is the high side gate charge.

In the table 2 are various candidates that meet the above constraints. For each candidate the power losses P_{LOSS} and P_{LOSS_LDO} were calculated.

Table 2

$R_{DS_{(on)}}$	Q_{GD}	Q_{GS}	R_G	$V_{GS_{THR}}$	Ohmic Loss	Transision Loss	Total Loss	Drive Loss
0.0032	4	2.5	0.4	2.5	0.104	1.0296	1.1336	0.806
0.0039	7	9	2.4	3.3	0.12675	4.8384	4.96515	1.984
0.0042	7	9	2.4	3.3	0.1365	4.8384	4.9749	1.984
0.008	2	4.5	3	2	0.26	2.2464	2.5064	0.558
0.0067	5.3	3.9	1.5	1	0.21775	2.18592	2.40367	0.7998
0.0093	2	4.9	1	2	0.30225	1.39104	1.69329	1.488
0.019	8	4	1.3	2	0.6175	2.6784	3.2959	1.798
0.0095	7.5	6	1	3	0.30875	2.7216	3.03035	1.736

The MOSFET highlighted in grey is the one we selected. In this case, it is only the second best candidate that fits the required parameters, but it is a lot cheaper than the best fit and has better documentation.

The same device is used for both the high-side and low-side switch.

3.4.5 Measurement of Output Voltage and Output Current

The LT3741 is both voltage regulated and current regulated. The voltage divider $R_{11} \parallel R_2$ (see figure 9 on page 8 and figure 10 on page 11) allows for the measurement of the output voltage, and a shunt resistor R_4 allows for the exact monitoring of the current going through coil L_1. The value for resistor R_4 was chosen so that the maximum outoing current can be 5 A.

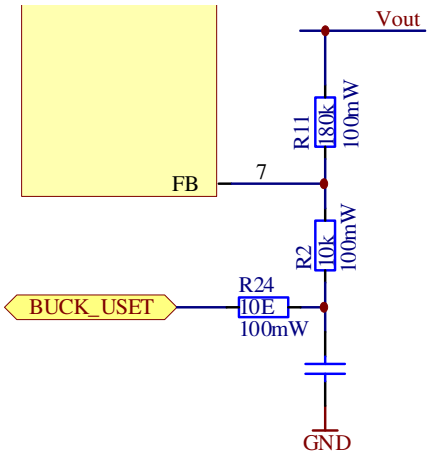

Figure 10: regulation of output voltage by changing the reference voltage in the feedback loop via an analog reference voltage between 0 V and 1.21 V

Monitoring the current is extremely important for a setup in which the outgoing voltage can be constantly changing. It allows to more accurately predict the behavior of the output voltage, thus enabling the device to better suppress spikes in output voltage and spikes in the current going through coil L_1.

Furthermore, a controller regulated by current can also be used as a constant current source. This property is mainly of importance when the operating point is in the steeper part of the PV module's VI-curve (where small changes in voltage can lead to drastic changes in current and vice versa).

The values for the feedback resistors R_2 and R_{11} were chosen according to formula 17 so that the output voltage does not exceed 23 V:

$$V_{out} = 1.21\,\mathrm{V}\left(1 + \frac{R_{11}}{R_2}\right) \tag{17}$$

By increasing $BUCK\_USET$ in formula 18, the outgoing voltage can then be modified as needed:

$$V_{out} = (1.21\,\mathrm{V} - BUCK\_USET) \cdot \frac{R_{11} + R_2}{R_2} \tag{18}$$

$BUCK\_USET$ is the analog voltage coming from the first DAC. The associated circuit can be found in figure 10.

In a manner analogous to regulating the output voltage, the maximum output current can also be controlled. By applying an analog voltage between 0 V and 1.5 V at input `CTRL1` of the LT3741

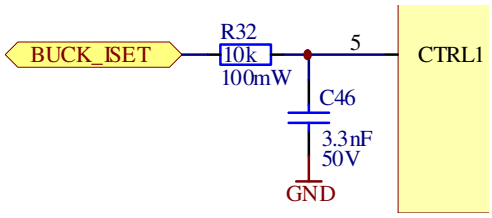

Figure 11: Setting the maximum output current via reference voltage between 0 V and 1.5 V

controller, the maximum *average* current going through coil L_1 and therefore the maximum output current can be directly controlled.

The corresponding circuit can be found in figure 11. The maximum average output current I_o is calculated using formula 19.

$$I_o = \frac{V_{CTRL1}}{30 \cdot R_4} \tag{19}$$

For this, V_{CTRL1} is the analog reference voltage coming from the second DAC and R_4 is the shunt resistor (10 mΩ, visible in figure 9).

For the microcontroller to generate appropriate reference voltages, it needs to measure both output voltage and output current. The output voltage is measured with the circuit in figure 12. The values for resistors R_{12} and R_{15} are such that voltage $BUCK\_UMEAS$ is scaled to the range between 0 V and 1.5 V.

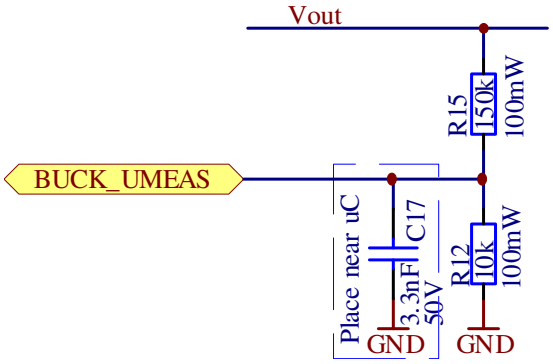

Figure 12: Messen der Ausgangsspannung

The output current is measured differentially via shunt resistor R_5. The corresponding circuit can be seeen in figure 13.

A particular problem for this measurement is that resistors R_{10} and R_{14} cause a bias current to flow through the shunt resistor R_5, thus leading to an offset V_{offset} of the measured voltage over R_5:

$$V_{offset} = \frac{3.3\,\text{V} \cdot R_5}{R_{14} + R_{10} + R_5} \tag{20}$$

Since the ADC has a resolution of 12 bits and a reference voltage of 3.3 V, one voltage increment can be calcualted according to the following equation:

$$V_{step} = \frac{3.3\,\text{V}}{2^{12}} = 806\,\mu\text{V} \tag{21}$$

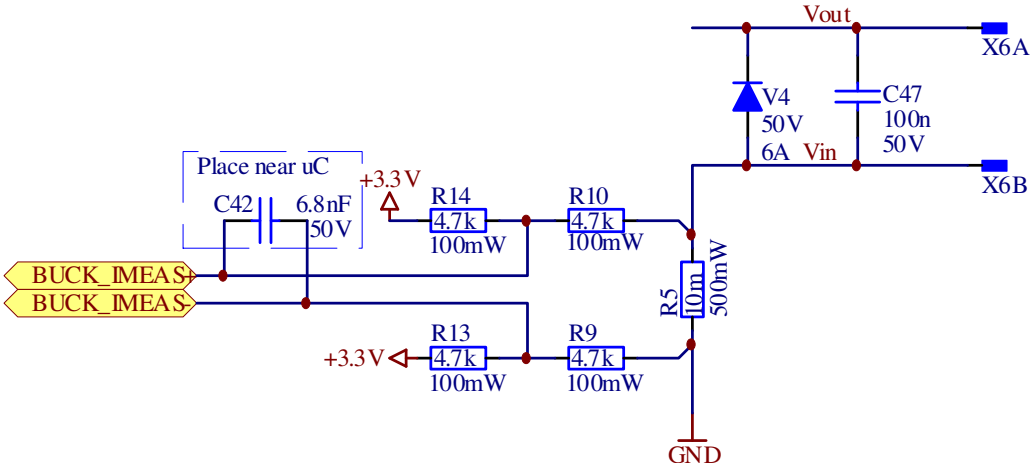

Figure 13: Messen des Ausgangsstromes

Resistors R_9, R_{10}, R_{10} and R_{14} should be as small as possiblein order to reduce disturbances in the traces, while at the same time being large enough for V_{offset} to be smaller than V_{step}. In order for the ADC's holding time not to be too long (which happens roughly at $\geq 5\,\mathrm{k\Omega}$), they should however also not be too large.

Equations 20 21 can now be solved for the four resistor values:

$$\begin{aligned} V_{step} &\geq V_{offset} \\ \frac{3.3\,\mathrm{V}}{2^{12}} &\geq 3.3\,\mathrm{V} \cdot \frac{R_5}{R_x + R_5} \\ \frac{1}{2^{12}} &\geq \frac{R_5}{R_x + R_5} \\ R_x &\geq \left(2^{12} - 1\right) \cdot R_5 \end{aligned}$$

where $\frac{R_x}{2} = R_9 = R_{10} = R_{13} = R_{14}$. This yields as its result $\frac{R_x}{2} \approx 22\,\Omega$.

A further limitation, especially for smaller resistors, is not to dissipate too much power. For this reason, the resistors will be dimensioned slightly higher at $270\,\Omega$. Thus, the resulting dissipated power for all four resistors comes to:

$$P_{loss} \approx \frac{(3.3\,\mathrm{V})^2}{2 \cdot 270\,\Omega} \approx 20\,\mathrm{mW}$$

The measured voltage at the shunt resistor is comparatively small. For this reason, we use the microcontroller's integrated preamplifier (PGA), which can attain a gain of up to factor 64. The amplified signal is then passed on to the internal differential ADC.

3.4.6 Output

Two banana plugs X_{6A} and X_{6B} provide the connection to the output voltage, while reverse voltage protection is achieved via diode V_4.

An external reference voltage of 1.5 V is used to ensure that the ADCs and DACs can make accurate measurements and can be used over their full range (see figure 15).

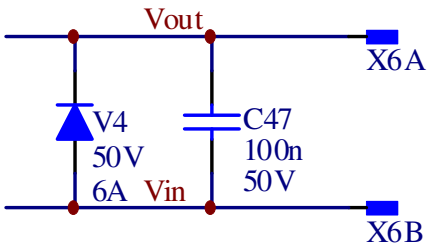

Figure 14: reverse voltage protection at output

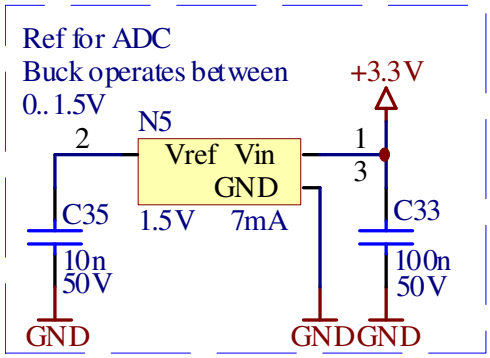

Figure 15: 1.5 V reference voltage for full-range operation of DACs and DACs

3.4.7 Enable and Under-Voltage Lockout circuit

The LT3741's *Enable* input is enabled and disabled by the microcontroller's *BUCK_EN* signal on one hand, on the other hand it is can be forcibly disabled in hardware when the 28 V rail drops below 25 V. This allows for a controlled and predictable behavior of the LT3741 during power-on and power-off. The corresponding circuit can be found in figure 16.

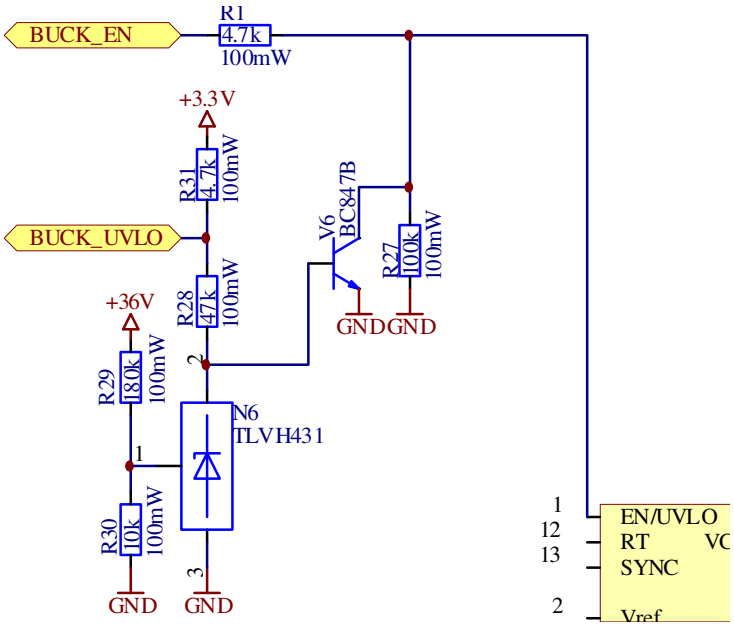

Figure 16: Under-Voltage Lock-Out (UVLO) allows for controlled power-on and power-off of the controller

In case of under-voltage, N_6 switches on and the transistor V_6 starts to conduct, thus pulling the *Enable* input to *Low*. Voltage $BUCK\_UVLO$ triggers an interrupt in the microcontroller.

4 PCB Design

When designing a PCB – especially when a switch-mode power converter is a central component to the design – the location of components and their *routing* (electrical connections) can be critical for correct operation. Some of the more important items that were considered are listed here.

- High frequency, high power loops are routed as tightly as possible.
- Sensitive, high impedance traces are kept separate from other signals and routed as differential pairs where necessary.
- Digital logic is kept separate from analog and high power circuitry.
- Power rails and their bypass capacitors need to be placed intelligently.
- Larger copper areas can be used to meet heat dissipation requirements.
- The positioning of mechanical parts can be annoying because they take up way more space than what one might initially, naively, expect.

Figure 17 shows how our $60\,\text{mm} \times 60\,\text{mm}$ printed circuit board is partitioned. In particular we would like to emphasise how the ground plane has been split from top to bottom, physically separating partition A from the other three partitions, and how the LT3741 is placed in the center where the two planes join. Partition A contains high power/high frequency components, such as the two switching MOSFETs, the inductor, and the output capacitors, whereas the other partitions contain more sensitive circuitry (in particular partition C). The split helps minimize any crosstalk. The LT3741 chip is placed at the joining position of the two split planes because it must communicated with the digital logic as well as power the high power circuitry.

Partition C contains the micro controller, LCD header, push/twist button header and other digital components.

Partition B contains the components responsible for generating the three voltage rails discussed in section 3.3. It was placed at the bottom of the board where the power input is located, to minimize the trace lengths required for power distribution on the board, and it was also placed far away from partition B such that interference with the digital circuitry is minimized.

Partition D is electrically isolated from the rest of the circuit and contains the components responsible for USB communication. It was isolated because the voltage potential of a connected USB device may be different than the potential our device is running on.

Figure 18 shows the two critical loops where short intervals of high amounts of current flow in this design. The first (green) loop is active when the switching MOSFET V_2 is conducting and transferring charge from the input bypass capacitors C_3, C_4, C_{12} and C_1 through the resistor $R4$ into the inductor L_1. The second (blue) loop is active when the switching mosfet V_3 is conducting and transferring charge from the inductor L_1 through the resistor R_4 into the output bypass capacitors C_{15}, C_{11}, C_7 and C_8.

It is critical for the total physical length of these loops to be minimized. Our solution can be seen in the physical PCB layout in figure 19.

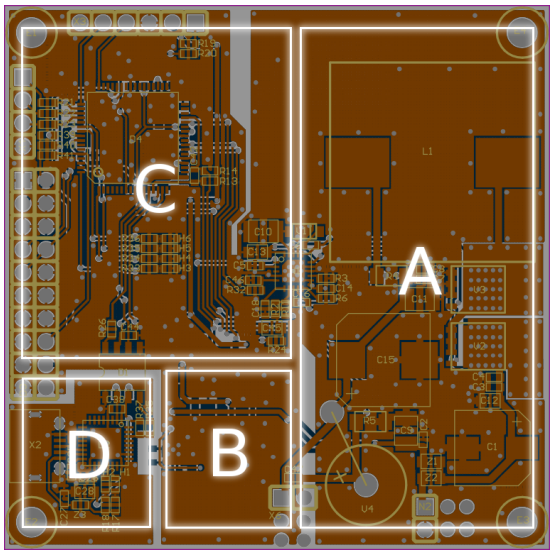

Figure 17: Partitioning scheme of component groups. **A:** High power components **B:** Voltage rails **C:** Digital logic **D:** Isolated transceiver logic

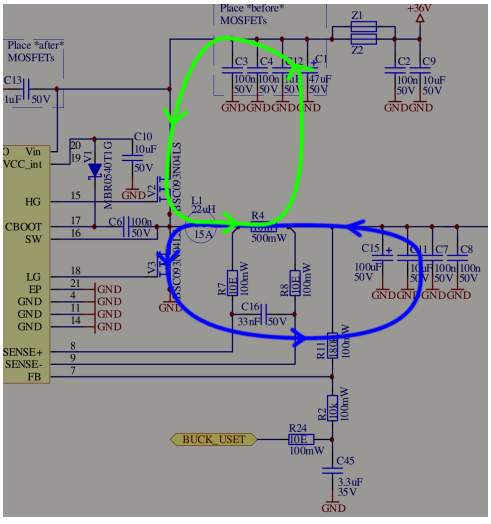

Figure 18: Critical high current, high frequency loops in the schematic. Blue indicates the current path of the first critical loop, green the second.

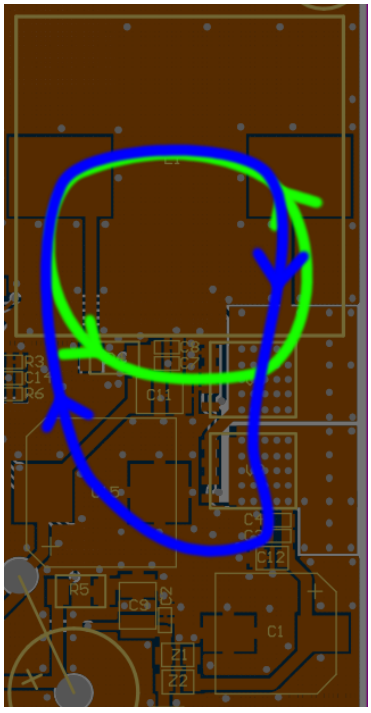

Figure 19: High current, high frequency loops are routed as tightly as possible

5 Software

5.1 Firmware

5.2 Constraints for the uC programm

The chosen microcontroller dsPIC33ep provides 16kB of ROM and 2kB of RAM, 12bit resolution in the ADC and DAC and up to 60 MIPS computing power. The anti-aliasing filter of the ADC is set to 5khz, which means that we need to sample with at least 10khz. However the LT3741 regulator takes about 300us to adjust its output voltage — 3 times longer then our sample rate. To remedy this we use Oversampling by factor 4, which has the nice benefits of giving us an additional bit of resolution and making the anti-aliasing filter simpler. The main routine for the adjustment of the regulator should not use more than 25the CPU time and must run every 400us, so it must not take longer than 100us or about 6000 Instructions to finish one calculation.

5.3 Calculation of the I-V curve

The I-V curve from (7) is implemented using a fixed point library supplied by Microchip. Since this library also provides an exponential function, the implementation is made straightforward.

5.4 Finding the operating point

To find the target operating point, we calculate the load resistance by dividing the actual voltage by the actual current $R_{load} = U_{is}/I_{is}$. Then we draw the load line $I = f(U) = U/R_{load}$ and find the intersection with the I-V curve of the model. This process is pictured in figure 20. The intersection is found by using a binary search algorithm, which is converging slower than

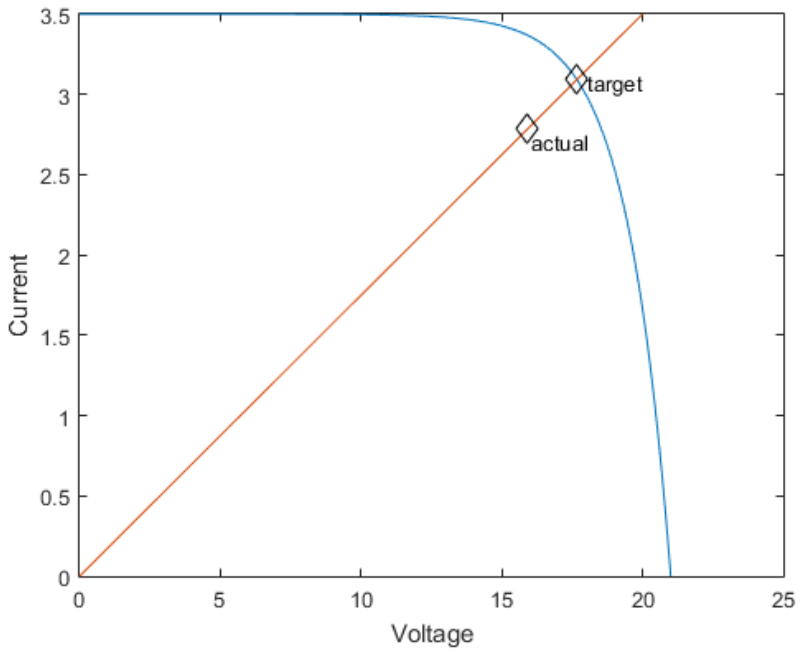

Figure 20: Actual and target operating points

newton's method but more stable — newton's method can fail if V_T in (7) is small.

5.5 Using more than one curve

If we want to use multiple curves to model the staircase characteristic shown in figure 4 we need to determine which curve is applicable for a given load. This process can be made less CPU intensive if we precalculate the resistance-thresholds by finding the intersections between two curves. There is always exactly one intersection if $V_{oc1} > V_{oc2}$ and $I_{sc1} < I_{sc2}$.

insert graph

5.6 Front-End

- Weshalb Kommunikation via PC?
- Was für Möglichkeiten bietet das Interface (senden von Instruktionen, Auswerten von Daten)?
- Verwendete Toolkits/Frameworks? (weshalb?)
- Genereller Aufbau der Benutzeroberfäche
- Möglichkeiten der Bedienung

6 Verification

There are a variety of tests that can be conducted to verify the performance and correctness of our device. The following is a list of test fixtures and their expected results based on simulations.

6.1 Test Fixtures

6.1.1 Trivial VI Curve

6.1.2 Non-trivial VI Curve

6.1.3 Ripple Voltage and Ripple Current vs Resistive Load

Using LTspice [3], the circuit of our regulator was modeled and the peak-to-peak ripple current and voltage was simulated using different resistive loads ranging from 100 mΩ to 1 kΩ at an output voltage of 12 V. Figure 21 is a plot of the ripple current and voltage versus the resistive load.

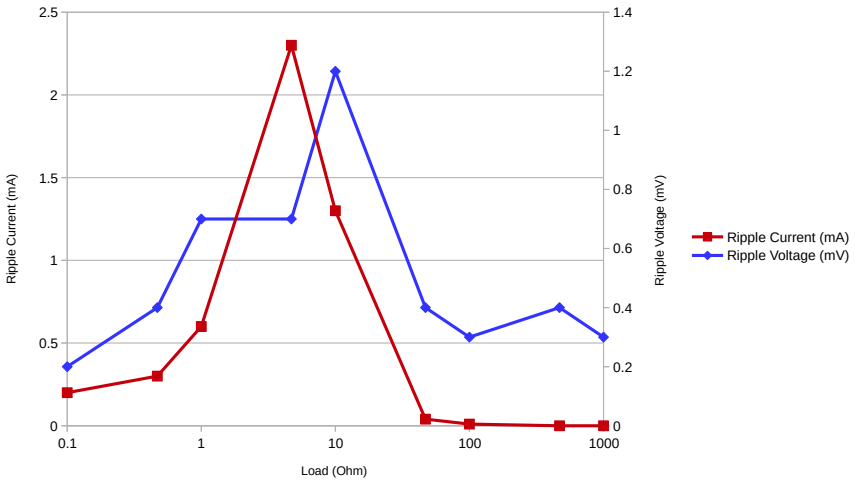

Figure 21: Simulation of the amplitude of the ripple voltage and ripple current vs different resistive loads, obtained using LTspice IV's model of the LT3741

In order to test this on the real device, a constant output voltage of 12 V is programmed and a potentiometer is attached to the device's output connectors, as illustrated in figure 22

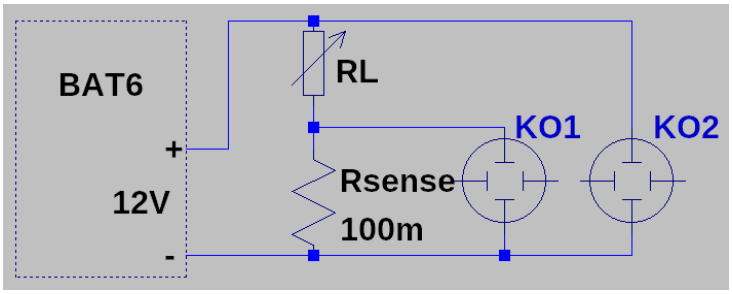

Figure 22: Test fixture for measuring ripple voltage & ripple current of the device

The ripple current is measured over a small sense resistor R_{sense} using an oscilloscope. The ripple voltage is measured using a second channel of the oscilloscope by measuring the output voltage.

The peak-to-peak ripple voltage and current is measured for different resistive loads ranging from 100 mΩ to 1 kΩ and compared to the simulated model.

6.1.4 Power Absorbtion

As stated in the specifications, the device must have the ability to sink current as well as source current. In order to test this, the device is programmed to output 12 V and is connected in series with a current limiting resistor and a second power source set to a higher voltage, as illustrated in figure 23.

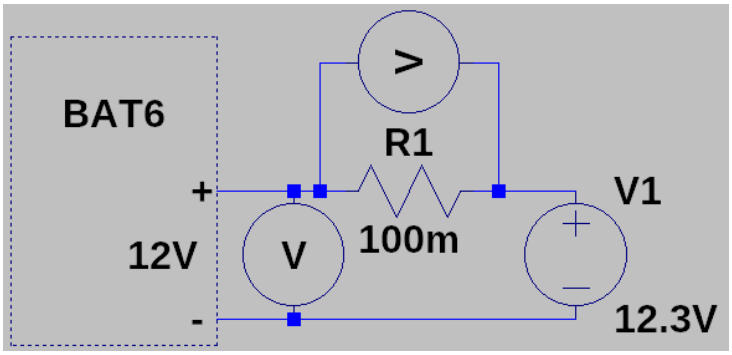

Figure 23: Test fixture for measuring power absorbtion of the device.

The second voltage source is slowly increased until 3 A are flowing through the current limiting resistor R_1 (which can be determined by measuring the voltage over said resistor), all while the device's output voltage is closely monitored. The output voltage is expected to remain constant.

6.1.5 Transient Response

This test is used to determine the reaction speed of the regulator and the VI control algorithm when switching quickly between two extreme resistive loads. The device is programmed to mimic the behaviour of a simple solar panel model. As illustrated in figure 24 the output voltage is measured using an oscilloscope and various resistive loads are switched on and off over the output using a MOSFET and a signal generator.

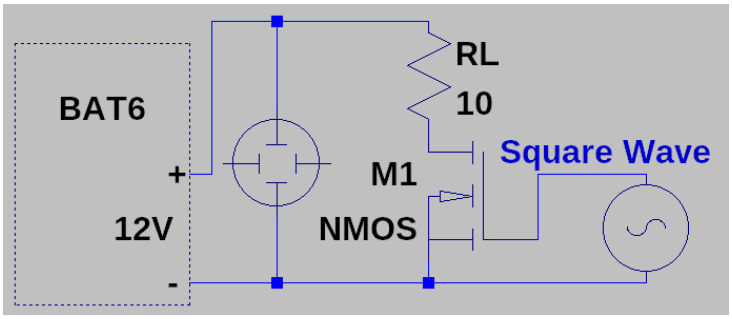

Figure 24: Test fixture for measuring the transient response of the device

The frequency of the signal generator is set to a low value such that the device's output voltage is always stable before the load is changed.

The results of this measurement will make a statement over the propagation delay of the algorithm as well as the time it takes for the voltage to stabilise again.

6.1.6 Reactive Loads

In the course specification we opted to test the device with various capacitive and inductive loads out of curiosity. During the course of the project we learned that this is not an applicable test because reactive loads are primarily used for testing the behaviour of power factor correction – which, according to the EN61000-3-2 regulations [5], affect devices consuming more than 75 W, meaning that the main power supply we use already implements power factor correction and testing for this would be meaningless. Furthermore, the measurements we obtain from tests using reactive loads would require an immense amount of additional research on our part before the results could be interpreted in any meaningful way. For this reason we have decided to omit this test case.

6.2 Measurement Results

Unfortunately, we were unable to operate the LT3741 for a period long enough to conduct any of the measurements listed above. The same regulator model (LT3741) was permanently damaged twice in a row. Please see the next section for a detailed analysis on what we think the issue is and how we would proceed if more time to do so were available.

6.3 Analysis of the Issue

6.3.1 A Quick Overview

The first regulator output the correct voltage of 12 V when being supplied with 32 V. Unplugging the device and re-plugging it into a 36 V power supply instantly damaged it permanently. After some detailed measurements it was concluded that the high-side driver inside the LT3741 was somehow damaged and not operating as it should. Our assumption was that – since we were operating the device very closely to its maximum ratings of 40 V – during switching, the high-side MOSFET driver was exposed to transients exceeding the device's absolute maximum ratings and thus damaging the driver permanently.

The regulator was replaced with a new one and the supply voltage was lowered from 36 V to 28 V in order to give more leeway for the supposed transient voltages. The new regulator appeared to output the correct voltage of 12 V, so a resistive load of 80 Ω was connected on the output of the regulator. After about 20 s of continuous operation, the output voltage again dropped and the device was permanently damaged. Unfortunately, we were unable to capture some vital measurements of the transients we were looking for to confirm our suspicions from the first failure. It is clear, however, that the damage was not caused by the device overheating, as none of the components were remotely warm to the touch. This seems to align with the transient theory.

6.4 Simulating the Issue

The physical layout of the regulator and the MOSFETs is depicted in figure 25. The physical length of the traces connecting the Switch (SW), High Gate (HG) and Low Gate (LG) pins of the regulator to the switching MOSFETs is fairly long (>2 cm). Most of the time, the parasitic inductances and capacitances are negligible. In this case, however, they aren't.

The series inductance and series resistance is calculated using an on-line calculator [1] [2] (the width, length, and thickness is known to be 0.4 mm, 2 cm and 35 µm respectively) and added to the simulation model seen in figure 26.

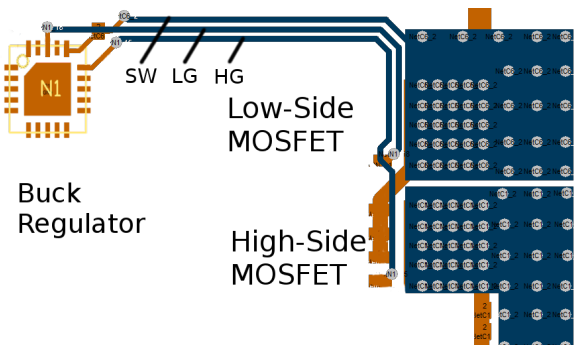

Figure 25

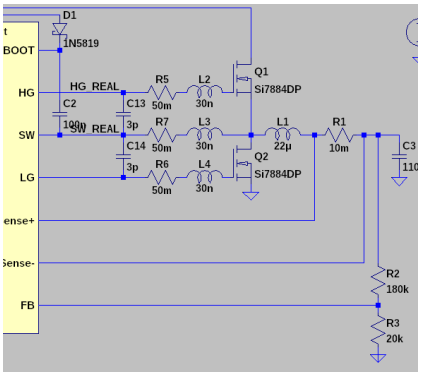

Figure 26

The voltage on the SW pin of the regulator is simulated and plotted. Figure 27 compares the more accurately modelled curve (in blue, labelled *sw_real*) with the ideal model of the voltage on the SW pin (in yellow, labelled *sw_ideal*). The two red lines represent the expected maximum voltage (28 V) and the device's absolute maximum rating on the SW pin (40 V).

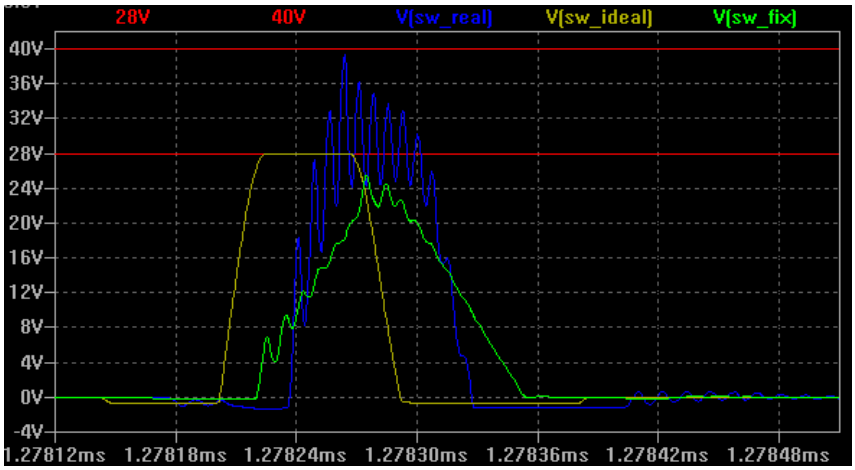

Figure 27

It is clear that these small parasitic inductances have a huge impact. The real curve (blue) exhibits ringing with an amplitude overshooting the expected maximum voltage by almost 12 V! It is therefore very likely that the high driver was destroyed due to an over-voltage event.

The immediate solution to this problem is to add resistors in series with each of the critical connections to dampen the ringing. The effect of a 3.3 Ω resistor in series with each connection is plotted in figure 27 (green curve, labelled *sw_fix*). When compared to the ideal and real curves, we see that the peak voltage has been reduced to a much less dangerous level.

The more optimal solution is of course to modify the PCB layout such that these traces have a much shorter distance.

7 Conclusions

- Was funktioniert?
- Was funktioniert nicht?
- Weshalb?
- Was könnte noch gemacht werden?

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