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Studiengang	EIT
Modul	Projekt 3
Team	2
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Version	1

Abstract

Contents

Versionsgeschichte

Saturday 2nd January, 2016 `Version 0.1:` Einleitung & Disposition

1 Einleitung

Mit der zunehmenden Verbreitung von erneuerbaren Energiequellen hat sich in den letzten Jahren die Solartechnologie zunehmender Popularität erfreut, und wird mit grosser Wahrscheinlichkeit in Zukunft noch weiter an Bedeutung gewinnen.

Doch wie mit vielen anderen Technologien wächst mit steigender Verwendung auch bei der Solartechnik das Bestreben, die Technologie besser zu verstehen und schlussendlich besser zu kontrollieren, um ihr Potenzial bestmöglich ausschöpfen zu können.

Im Rahmen des Projekts 4 soll im Frühlingssemester 2016 deshalb ein Überwachungsgät für Photovoltaik-Zellen entwickelt werden. Um die korrekte Funktionsweise dieses Überwachungsgerätes im Labor verifizieren zu können, soll in diesem Projekt ein Netzgerät entwickelt werden, das eine Photovoltaik-Zelle unter verschiedenen Bedingungen simulieren kann.

Als Zusatzanforderung soll nicht nur eine einzelnes Element, sondern auch die Serie- und Parallelschaltung mehrerer PV-Zellen simuliert werden können. Dazu werden mehrere Simulatoren entsprechend gekoppelt.

Der Simulator ist grundsätzlich ein Labornetzgerät mit der Besonderheit, dass verschiedene Strom-Spannungs-Kurven vom Benutzer definiert werden können. Diese unterschiedlichen Kurvenverläufe orientieren sich am Verhalten von PV-Modulen unter verschiedenen Umständen (z.B. volle Sonneneinstrahlung, teilweise abgeschattet/verdreckt, etc.).

Das Gerät ist mikrocontroller-basiert und hat ein einfaches Benutzer-Interface sowie die Möglichkeit, mit einem PC via serielle Schnittstelle zu kommunizieren.

2 Task Description

- Was ist der grundsätzliche Auftrag?
- Was ist das Ziel?
- Motivation hinter dem Projekt/Auftrag?
- Grundsätzliche Informationen zu Photovoltaik-Modulen und den zu untersuchenden Fragen (Verhalten unter nicht-idealen Umständen) liefern.
- Was sind die grundsätzlichen Anforderungen an unser Gerät?

3 Basic Concept

- Weshalb wurde das benutzte mathematische Modell gewählt?
- Weshalb wird ein Schaltregler benutzt?
- Weshalb wurde ein eigenes PCB entwickelt statt ein Steckbrett verwendet?
- Wie soll unser Gerät bedient werden können?

4 Component Selection

The selection of components is discussed in detail.

Es wird in Detail beschrieben, welche elektronische Komponenten aus welchem Grund ausgewählt worden sind.

- Was sind die Anforderungen an die Stromversorgung?
- Weshalb wird der dsPIC33EP-Chip verwendet?
- Weshalb wird der LT3741 verwendet?
- Wie erfolgt die Ansteuerung des LT3741?
- Weshalb wurde das verwendete LCD gewählt?
- Wie wird die serielle Schnittstelle realisiert?

4.1 36V Power Supply and Mains Input

The maximum required output power of our device was roughly calulated as $24\,\mathrm{V} \cdot 3\,\mathrm{A} = 72\,\mathrm{W}$. Assuming an efficiency of $\eta \approx 90\,\%$ an 80 W power supply is required.

The design and construction of a custom power supply would have consumed too much time and resources. Instead, we opted for an external power supply which can be mounted inside the housing. The selected power supply is capable of supplying 28 V at 75 W and can be seen in figure 1.

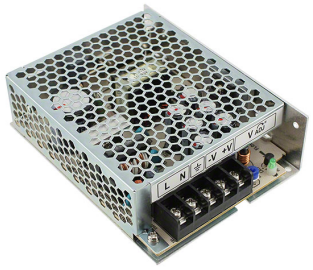

Figure 1: External PSU

Figure 2: Power Entry Module

Figure 3: Rocker Switch

The device can be plugged into a power outlet by means of an IEC 60320 C13 socket seen in figure 2. The socket has a built-in fuse as well as a built-in mains filter, which will reduce high frequency coupling from the device back into the mains.

A rocker switch (figure 3) is connected in series with the socket and the power supply, allowing for the end user to cut power at any time.

TODO: Show photo of wiring in housing

4.2 Voltage Rails

This design requires three different voltage levels (known as voltage *rails*), which are 28 V, 5 V and 3.3 V respecitvely. Each rail has different requirements as far as noise, power and efficiency goes.

First and foremost, the maximum current of each voltage rail must be approximately determined. This information is crucial for selecting appropriate voltage regulators.

The most power-hungry component on the 3.3 V rail is clearly the dsPIC33 microcontroller and LEDs. According to the datasheet, the microcontroller will consume $0.5\,\text{mA}\,\text{MHz}^{-1}$. Since the microcontroller will be clocked at 120 MHz, the minimum current can be calculated with the following equation.

$$I_{dsPIC} = 0.5\,\text{mA}\,\text{MHz}^{-1} \cdot 120\,\text{MHz} = 60\,\text{mA} \tag{1}$$

The other significant power-hungry components are the four LEDs connected to the dsPIC33 microcontroller. Each consume 15 mA. The total current consumption of the 3.3 V rail is therefore roughly:

$$I_{3.3\,\text{V}} = I_{dsPIC} + 4 \cdot 15\,\text{mA} = 120\,\text{mA} \tag{2}$$

The 3.3 V rail derives it's voltage from the 5 V rail. Additionally, the OLED display is powered by the 5 V rail, which, according to the datasheet, draws a maximum current of 135 mA. The total current consumption of the 5 V rail will approximately be:

$$I_{5\,\text{V}} = I_{3.3\,\text{V}} + 135\,\text{mA} = 255\,\text{mA} \tag{3}$$

A decision for each voltage rail must be made. Do we use a switch-mode power regulator or a linear regulator? The general trade-off is that swith-mode regulators have a very high efficiency, but due to the nature of how they transform voltages, they produce a lot more jitter on the output. In contrast, a linear regulator produces almost no jitter – in fact, it even dampens incoming jitter by a substantial amount – however, the linear regulator has very poor efficiency since it just "burns" the excess voltage and produces a lot of heat, making it a poor candidate for transforming between larger voltage differences.

The 28 V rail is already taken care of, since that's precisely the voltage the external power supply provides.

Seeing as there is a very large voltage difference between 28 V and the next lower rail, 5 V, a switch-mode regulator is clearly the only sane choice to be made for powering the 5 V rail due to efficiency reasons. The diagram of this circuit is illustrated in figure 4. There is little reason to discuss the selection of components of this circuit in great detail; It's using a standard configuration according to the datasheet. The regulator was chosen based on the current requirement $I_{5\,\text{V}}$ and is capable of supplying a maximum current of 750 mA.

All digital circuitry, such as the micro controller, operates at 3.3 V. It is particularly important for the 3.3 V rail to have as little noise/jitter as possible. This requirement stems from the fact that the analog-to-digital (ADC) conversions and digital-to-analog (DAC) conversions derive their reference voltage from the 3.3 V rail. Any noise on this rail could impact the accuracy of these conversions and could result in lower accuracy of the final, regulated output voltage of the device itself. For this reason we opted for a linear regulator to power the 3.3 V off of the 5 V rail. The circuit is illustrated in figure 4. This regulator was also chosen based on the current requirement $I_{3.3\,\text{V}}$ and is capable of supplying a maximum current of 1 A.

4.3 LT3741

There are many reasons why the LT3741 was chosen to regulate the output voltage of this device. The most important reasons are listed here.

- **Re-inventing the wheel.** Switch-mode regulators aren't new technology. They've been studied and perfected over decades by many engineers. For this reason we decided against building a regulator descretely and instead opted to use an existing regulator if available.

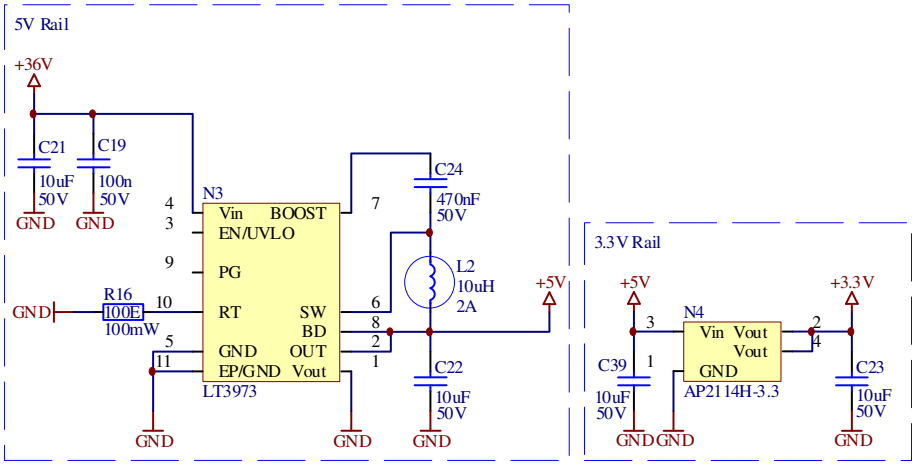

Figure 4: Speisung für 5V mittels Abwertswandler (links) und Speisung für 3.3V mittels Linearregler (rechts)

- **Voltage and current requirements.** The device is specified to output voltage levels between 0 V and 24 V and current levels between 0 A and 3.5 A. Further, the ripple voltage is specified to be ≤ 300 mV and the ripple current is specified to be ≤ 100 mA. The LT3741 fulfills all of these requirements.
- **The importance of power absorption.** Most switch-mode regulators are only able to *supply* power, but are incapable of *absorbing* power. Because our device may be connected in series (or parallel) with other power supplies, it must have the ability to absorb power too (which is the case if, say, it were connected to a voltage source outputting a higher voltage level than our own). A so-called *synchronous converter* possesses this property and the LT3741 is one of them.
- **Control inputs.** The LT3741 was chosen because it has dedicated input control pins for directly manipulating the regulated output current. This makes the design a lot simpler, because no complicated additional circuitry is required.

With the LT3741 selected, the selection of components required to control the LT3741 are discussed next.

4.3.1 Bypass Capacitors

The LT3741 is powered by the 28 V rail, which can be seen in figure 5 in the top right. Because the LT3741 consumes high amounts of power in very high frequent, short intervals (caused by the switching of the MOSFETs), the LT3741 is keen to feed high frequency disturbance back into the 28 V rail, which, if not handled correctly, could cause disturbances in the rest of the circuit. As a countermeasure we used a multitude of different ceramic and electrolytic bypass capacitors in parallel to help reduce EMI. Additionally, we used ferrite beads placed in series with the supply, which will absorb any high frequency feedback.

4.3.2 Switching Frequency

There is a tradeoff when selecting the switching frequency f_S. The higher f_S is selected, the lower the output ripple voltage will be, but the higher the power consumption will be (caused by switching losses). Generally, one will want to maximise f_S.

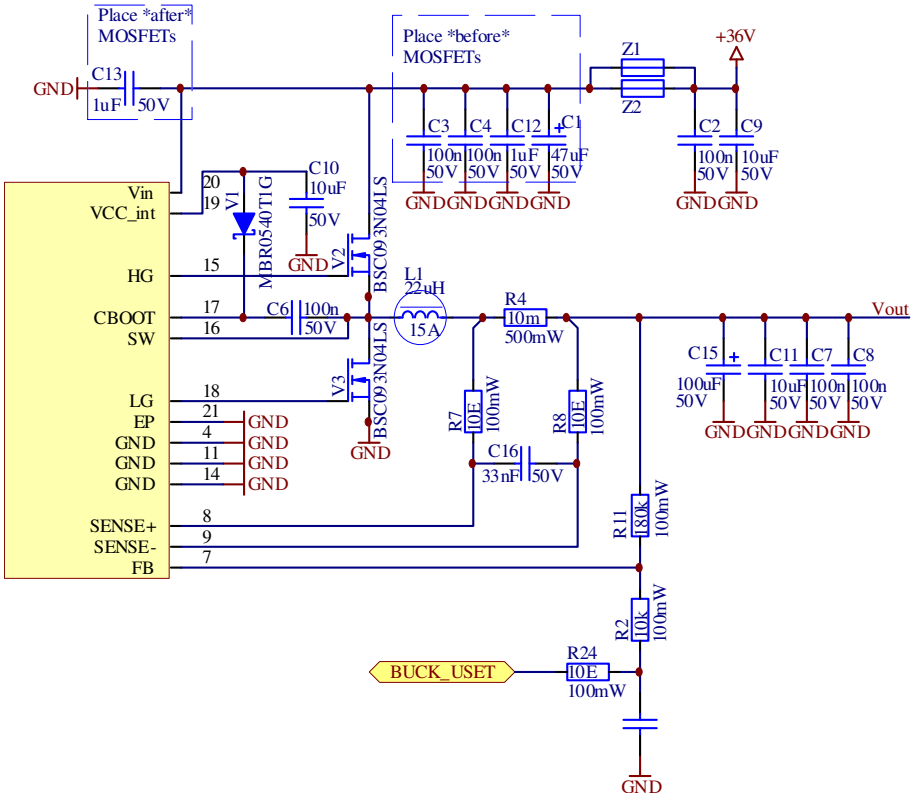

Figure 5: Herzstück des Projektes: Aufbau des LT3741 CVCC Synchronwandler

Due to all of the factors depending on f_S, it is only possible to determine this value imperically. We found a value of $f_S \approx 800\,\text{kHz}$ to be best suitable. In the rest of the calculations, f_S is assumed to be 1 MHz to allow for some leeway.

The switching frequency f_S is programmed by using a specific resistor on one of the inputs of the LT3741.

4.3.3 Inductor Selection

The size of the inductor L_1, as illustrated in figure 5, was calculated using formula 4

$$L_1 = \left(\frac{U_{in} \cdot U_{out} - U_{out}^2}{0.3 \cdot f_S \cdot I_O \cdot U_{in}} \right) = 6\,\mu\text{H} \tag{4}$$

where U_{in} is the input voltage 28 V, U_{out} is the output voltage at peak power (which exists at $U_{out} = 14\,\text{V}$), f_S is the switching frequency 1 MHz and I_O is the maximum output current, assumed to be $I_O = 5\,\text{A}$ for some additional leeway.

We ended up selecting a larger inductor of $L_1 = 22\,\mu\text{H}$ to further decrease ripple current.

In addition to the value of the inductor, the maximum current rating, DCR, and saturation current are also important factors to consider. The maximum current of the inductor is calculated using formula 5

$$I_{L_{1_{peak}}} = I_O + \left(\frac{U_{in} \cdot U_{out} - U_{out}^2}{2 \cdot f_S \cdot L_1 \cdot U_{in}} \right) = 5.2\,\text{A} \tag{5}$$

Where L_1 is the value of the selected inductor, 22 µH. The saturation current of the inductor was sized factor 1.2 higher than the peak current.

$$I_{L_{1_{saturation}}} = 1.2 \cdot I_{L_{1_{peak}}} \tag{6}$$

A list of candidates matching the above parameters are listed in table 1.

Table 1

Digikey	Price (CHF)	Inductance (µH)	DCR (Ω)	Ohmic Loss (W)
732-4237-1-ND	8.03	22	0.007	0.175
732-2179-1-ND	6.4	47	0.0335	0.8375
732-2177-1-ND	6.4	22	0.0146	0.365

It is clear that the one with the lowest DCR will be the most optimal. The one highlighted in grey is the one we chose.

4.3.4 MOSFET selection

In contrast to a non-synchronous regulator, this design uses two complementary MOSFETs V_2 and V_3, where V_3 acts as an active replacement for the free wheeling diode typically found in non-synchronous designs. As mentioned earlier, a crucial feature of this device is the ability to *absorb* power. V_3 makes this possible because it is able to regulate current in the opposite direction through the inductor L_1.

When selecting switching MOSFETs, the following parameters are critical in determining the best devices for a given application: Q_G (Total Gate Charge), $R_{DS_{(on)}}$ (On-Resistance), Q_{GD} (Gate to Drain Charge), Q_{GS} (Gate to Source Charge), R_G (Gate Resistance), U_{GS} (gate-to-source voltage), U_{DS} (drain-to-source-voltage), $I_{D_{max}}$ (peak drain current) and $U_{GS_{THR}}$ (gate threshold voltage).

The maximum drain current is equal to the previously calculated peak inductor current $I_{L_{1_{peak}}}$ in equation 5.

$$I_{D_{max}} = I_{L_{1_{peak}}} = I_O + \left(\frac{U_{in} \cdot U_{out} - U_{out}^2}{2 \cdot f_S \cdot L_1 \cdot U_{in}} \right) = 5.2\,\text{A} \tag{7}$$

where U_{in} is the input voltage 28 V, U_{out} is the output voltage at peak power (which exists at $U_{out} = 14$ V), f_S is the switching frequency 1 MHz, L_1 is the value of the selected inductor (22 µH) and I_O is the maximum output current, assumed to be $I_O = 5$ A.

The maximum drain-to-source voltage U_{DS} must be greater than the input voltage $U_{in} = 28$ V, including transients. We selected MOSFETs with $U_{DS} = 40$ V.

The signals driving the gates of the MOSFETs have a maximum voltage of 5 V with respect to the source. During start-up and recovery conditions, the gate drive signals may be as low as 3 V. To ensure that the LT3741 recovers properly, the maximum gate threshold voltage should be less than 2 V. For a robust design, the maximum gate-to-source voltage U_{GS} should be greater than 7 V.

Power losses in the MOSFETs are related to the on-resistance $R_{DS(on)}$; the transition losses related to the gate resistance R_G; gate-to-drain capacitance Q_{GD} and gate-to-source capacitance Q_{GS}. Power loss to the on-resistance is an Ohmic loss, $I^2 R_{DS_{(on)}}$. The power loss in the high side MOSFET V_2 can be approximated with formula 8.

$$P_{LOSS} = (\text{ohmic loss}) + (\text{transission loss})$$
$$\approx \left(I_O^2 \cdot R_{DS_{(on)}} \cdot \rho_T\right) + \left(\frac{U_{in} \cdot I_O}{5\,\text{V}} \cdot (Q_{GD} + Q_{GS}) \cdot (2 \cdot R_G + R_{PU} + R_{PD}) \cdot f_S\right) \tag{8}$$

where ρ_T is a temperature-dependant term of the MOSFET's on-resistance. Using 70 °C as the maximum operating temperature, ρ_T is roughly equal to 1.3. R_{PD} and R_{PU} are the LT3741 high side gate driver output empedance, 1.3 Ω and 2.3 Ω respectively.

Another power loss related to switching MOSFET selection is the power lost to driving the gates. The total gate charge, Q_G, must be charged and discharged each switching cycle. The power is lost to the internal LDO within the LT3741. the power lost to the charging of the gates is:

$$P_{LOSS\_LDO} \approx ((U_{in} - 5\,\text{V}) \cdot (Q_{GLG} + Q_{GHG}) \cdot f_S \tag{9}$$

where G_{GLG} is the low side gate charge and Q_{GHG} is the high side gate charge.

In the table 2 are various candidates that meet the above constraints. For each candidate the power losses P_{LOSS} and P_{LOSS_LDO} were calculated.

Table 2

$R_{DS_{(on)}}$	Q_{GD}	Q_{GS}	R_G	$U_{GS_{THR}}$	Ohmic Loss	Transision Loss	Total Loss	Drive Loss
0.0032	4	2.5	0.4	2.5	0.104	1.0296	1.1336	0.806
0.0039	7	9	2.4	3.3	0.12675	4.8384	4.96515	1.984
0.0042	7	9	2.4	3.3	0.1365	4.8384	4.9749	1.984
0.008	2	4.5	3	2	0.26	2.2464	2.5064	0.558
0.0067	5.3	3.9	1.5	1	0.21775	2.18592	2.40367	0.7998
0.0093	2	4.9	1	2	0.30225	1.39104	1.69329	1.488
0.019	8	4	1.3	2	0.6175	2.6784	3.2959	1.798
0.0095	7.5	6	1	3	0.30875	2.7216	3.03035	1.736

The MOSFET highlighted in grey is the one we selected. In this case, it is only the second best candidate that fits the required parameters, but it is a lot cheaper than the best fit and has better documentation.

The same device is used for both the high-side and low-side switch.

4.3.5 Measurement of Output Voltage and Output Current

The LT3741 is both voltage regulated and current regulated. The voltage divider $R_{11} \parallel R_2$ (see figure 5 on page 7 and figure 6 on page 10) allows for the measurement of the output voltage, and a shunt resistor R_4 allows for the exact monitoring of the current going through coil L_1. The value for resistor R_4 was chosen so that the maximum outoing current can be 5 A.

Monitoring the current is extremely important for a setup in which the outgoing voltage can be constantly changing. It allows to more accurately predict the behavior of the output voltage, thus enabling the device to better suppress spikes in output voltage and spikes in the current going through coil L_1.

Furthermore, a controller regulated by current can also be used as a constant current source. This property is mainly of importance when the operating point is in the steeper part of the PV

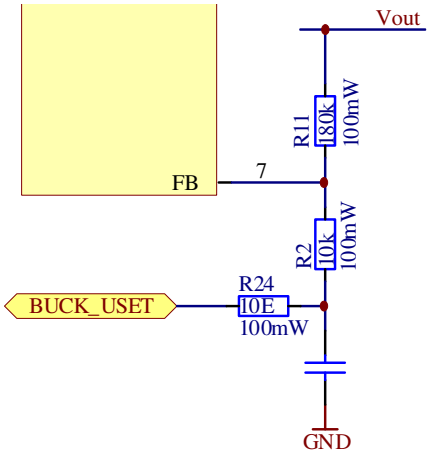

Figure 6: regulation of output voltage by changing the reference voltage in the feedback loop via an analog reference voltage between 0 V and 1.21 V

module's UI-curve (where small changes in voltage can lead to drastic changes in current and vice versa).

The values for the feedback resistors R_2 and R_{11} were chosen according to formula 10 so that the output voltage does not exceed 23 V:

$$U_{out} = 1.21\,\mathrm{V}\left(1 + \frac{R_{11}}{R_2}\right) \tag{10}$$

By increasing $BUCK\_USET$ in formula 11, the outgoing voltage can then be modified as needed:

$$U_{out} = (1.21\,\mathrm{V} - BUCK\_USET) \cdot \frac{R_{11} + R_2}{R_2} \tag{11}$$

$BUCK\_USET$ is the analog voltage coming from the first DAC. The associated circuit can be found in figure 6.

In a manner analogous to regulating the output voltage, the maximum output current can also be controlled. By applying an analog voltage between 0 V and 1.5 V at input `CTRL1` of the LT3741 controller, the maximum *average* current going through coil L_1 and therefore the maximum output current can be directly controlled.

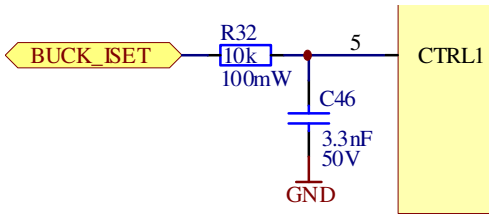

Figure 7: Setting the maximum output current via reference voltage between 0 V and 1.5 V

The corresponding circuit can be found in figure 7. The maximum average output current I_o is calculated using formula 12.

$$I_o = \frac{U_{CTRL1}}{30 \cdot R_4} \tag{12}$$

For this, U_{CTRL1} is the analog reference voltage coming from the second DAC and R_4 is the shunt resistor (10 mΩ, visible in figure 5).

For the microcontroller to generate appropriate reference voltages, it needs to measure both output voltage and output current. The output voltage is measured with the circuit in figure 8. The values for resistors R_{12} and R_{15} are such that voltage $BUCK\_UMEAS$ is scaled to the range between 0 V and 1.5 V.

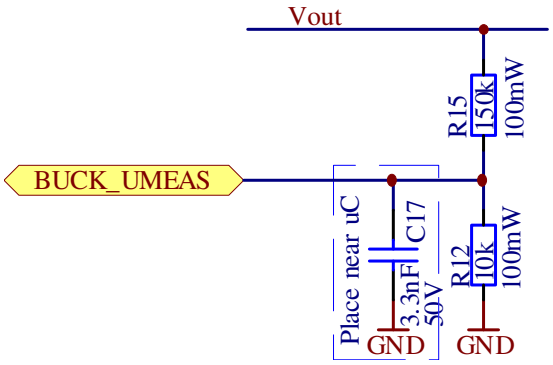

Figure 8: Messen der Ausgangsspannung

The output current is measured differentially via shunt resistor R_5. The corresponding circuit can be seeen in figure 9.

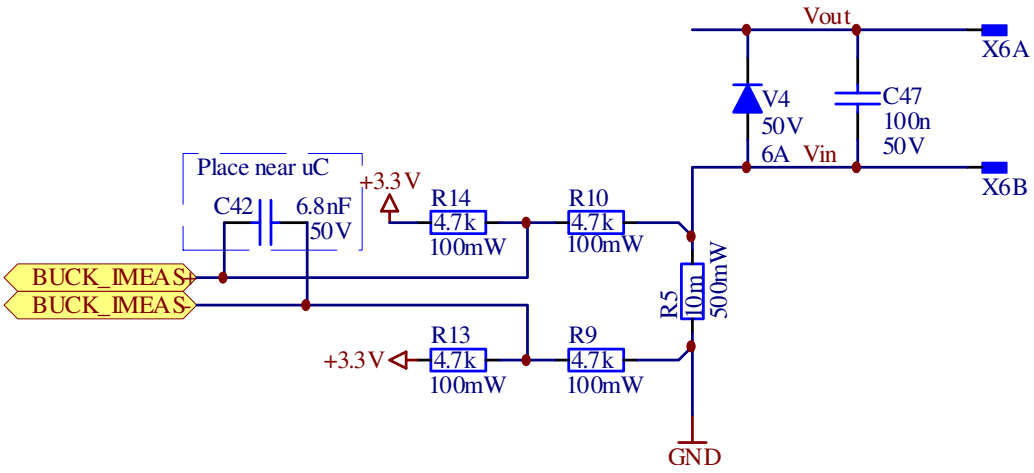

Figure 9: Messen des Ausgangsstromes

A particular problem for this measurement is that resistors R_{10} and R_{14} cause a bias current to flow through the shunt resistor R_5, thus leading to an offset U_{offset} of the measured voltage over R_5:

$$U_{offset} = \frac{3.3\,\mathrm{V} \cdot R_5}{R_{14} + R_{10} + R_5} \tag{13}$$

Since the ADC has a resolution of 12 bits and a reference voltage of 3.3 V, one voltage increment can be calcualted according to the following equation:

$$U_{step} = \frac{3.3\,\mathrm{V}}{2^{12}} = 806\,\mu\mathrm{V} \tag{14}$$

Resistors R_9, R_{10}, R_{10} and R_{14} should be as small as possiblein order to reduce disturbances in the traces, while at the same time being large enough for U_{offset} to be smaller than U_{step}. In order for the ADC's holding time not to be too long (which happens roughly at $\geq 5\,\mathrm{k\Omega}$), they should however also not be too large.

Equations 13 14 can now be solved for the four resistor values:

$$\begin{aligned} U_{step} &\geq U_{offset} \\ \frac{3.3\,\mathrm{V}}{2^{12}} &\geq 3.3\,\mathrm{V} \cdot \frac{R_5}{R_x + R_5} \\ \frac{1}{2^{12}} &\geq \frac{R_5}{R_x + R_5} \\ R_x &\geq \left(2^{12} - 1\right) \cdot R_5 \end{aligned}$$

where $\frac{R_x}{2} = R_9 = R_{10} = R_{13} = R_{14}$. This yields as its result $\frac{R_x}{2} \approx 22\,\Omega$.

A further limitation, especially for smaller resistors, is not to dissipate too much power. For this reason, the resistors will be dimensioned slightly higher at $270\,\Omega$ dimensioniert. Thus, the resulting dissipated power for all four resistors comes to:

$$P_{loss} \approx \frac{3.3\,\mathrm{V}^2}{2 \cdot 270\,\Omega} \approx 20\,\mathrm{mW}$$

The measured voltage at the shunt resistor is comparatively small. For this reason, we use the microcontroller's integrated preamplifier (PGA), which can attain a gain of up to factor 64. The amplified signal is then passed on to the internal differential ADC.

4.3.6 Output

Two banana plugs X_{6A} and X_{6B} provide the connection to the output voltage, while reverse voltage protection is implemented via diode V_4.

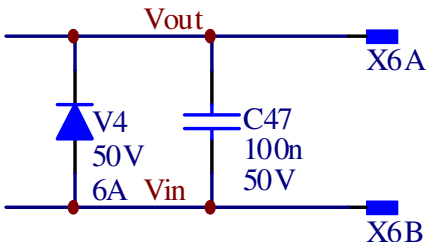

Figure 10: reverse voltage protection at output

An external reference voltage of 1.5 V is used to ensure that the ADCs and DACs can make accurate measurements and can be used over their full range (see figure 11).

4.3.7 Enable and Under-Voltage Lockout circuit

The LT3741's *Enable* input is enabled and disabled by the microcontroller's $BUCK\_EN$ signal on one hand, on the other hand, it can be disabled in hardware in case the 28 V rail drops below

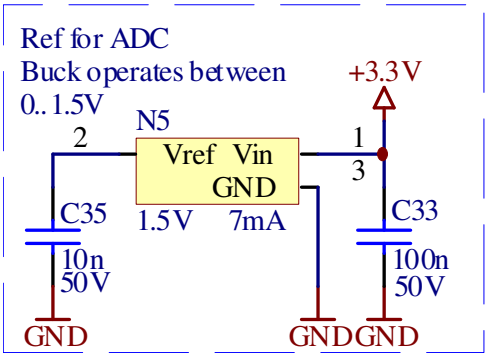

Figure 11: 1.5 V reference voltage for full-range operation of DACs and DACs

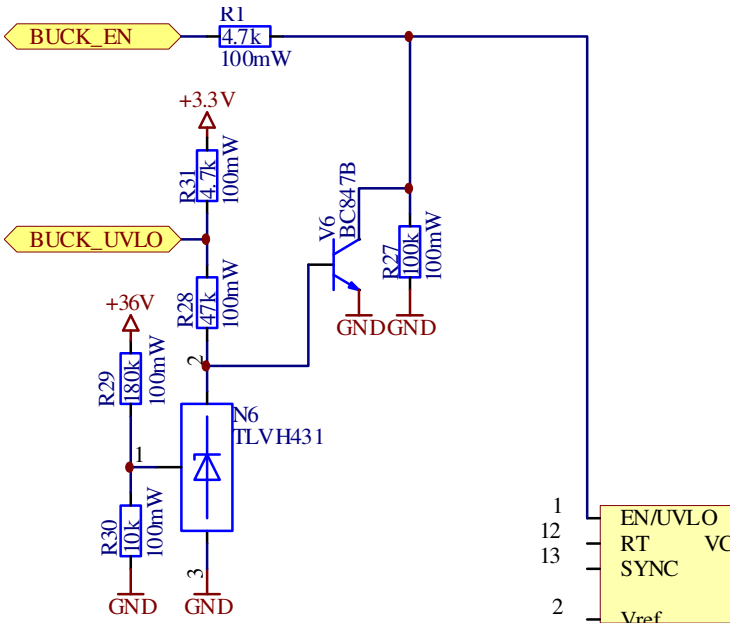

Figure 12: Under-Voltage Lock-Out (UVLO) allows for controlled power-on and power-off of the controller

25 V. This allows for controlled and predictable behavior of the LG3741 during power-on and power-off processes. The corresponding circuit can be found in figure 12.

In case of under-voltage, N_6 switches to locking mode, and the transistor V_6 starts to conduct, thus pulling the *Enable* input to *Low*. Voltage $BUCK\_UVLO$ triggers an interrupt in the microcontroller.

5 PCB Design

- Überlegungen zur Anordnung der Komponenten auf dem PCB
- Kritische Punkte:
  - Differentielle Messung
  - Buck-Regler und Spannungsversorgung
- Überlegungen zu den Ground-Planes

6 Firmware

- Wie wird das mathematische Modell in Software implementiert?
- Wie wird die Kommunikation mit einem PC implementiert? (Protokoll)
- Event-System
- User-Interface am Gerät

7 Front-End

- Weshalb Kommunikation via PC?
- Was für Möglichkeiten bietet das Interface (senden von Instruktionen, Auswerten von Daten)?
- Verwendete Toolkits/Frameworks? (weshalb?)
- Genereller Aufbau der Benutzeroberfäche
- Möglichkeiten der Bedienung

8 Verification

- Gehäuse-Erdungstest
- Was sind die Referenzwerte für die zu testenden Spezifikationen?
- Was ist das Verhalten des Gerätes bei verschiedenen resistiven, kapazitiven und induktiven Lasten (und Kombinationen davon)?
- Was ist das Verhalten des Floating Potentials und die Stromaufnahme bei verschiedenen resistiven, kapazitiven und induktiven Lasten (und Kombinationen davon)?
- Funktioniert das Interface korrekt?

9 Fazit

- Was funktioniert?
- Was funktioniert nicht?
- Weshalb?
- Was könnte noch gemacht werden?