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## Liquid Crystal Display (LCD)

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### HIGHLIGHTS

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# dsPIC33/PIC24 Family Reference Manual

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**Note:** This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33/PIC24 devices.

Please consult the note at the beginning of the “**Liquid Crystal Display (LCD)**” chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Website at: <http://www.microchip.com>

## 1.0 INTRODUCTION

The Liquid Crystal Display (LCD) driver module generates the timing control to drive a Static or Multiplexed LCD panel. In the 100-pin devices, the module drives panels of up to eight commons and up to 60 segments when five to eight commons are used, and up to 64 segments when one to four commons are used. It also provides control of the LCD pixel data.

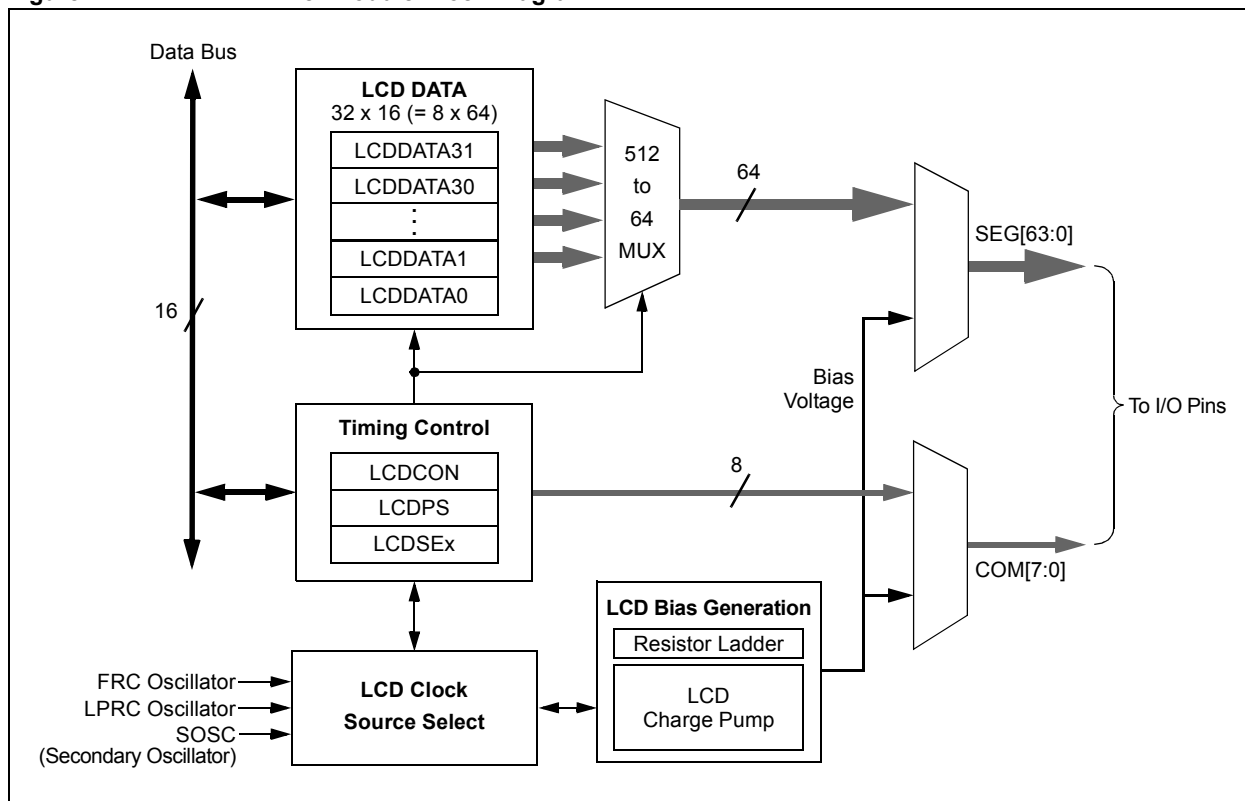
The LCD driver module supports:

- Direct Driving of LCD Panel
- Three LCD Clock Sources with Selectable Prescaler
- Up to Eight Commons:
  - Static (one common)
  - 1/2 Multiplex (two commons)
  - 1/3 Multiplex (three commons)
  - 1/8 Multiplex (eight commons)
- Up to 60 Segments (in 100-pin devices when 1/5-1/8 Multiplex is selected), 64 (in 100-pin devices when up to 1/4 Multiplex is selected), 46 (in 80-pin devices when 1/5-1/8 Multiplex is selected), 50 (in 80-pin devices when up to 1/4 Multiplex is selected), 30 (in 64-pin devices when 1/5-1/8 Multiplex is selected) and 34 (in 64-pin devices when up to 1/4 Multiplex is selected)
- Static, 1/2 or 1/3 LCD Bias
- On-Chip Bias Generator with Dedicated Charge Pump to Support a Range of Fixed and Variable Bias Options
- Internal Resistors for Bias Voltage Generation
- Software Contrast Control for LCD Using the Internal Biasing
- Enhanced LCD Mode with Dual Memory

A simplified block diagram of the module is shown in [Figure 1-1](#).

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Figure 1-1: LCD Driver Module Block Diagram



## 2.0 LCD REGISTERS

The LCD driver module has 78 registers:

- [LCDCON](#): LCD Control Register
- [LCDPS](#): LCD Phase Register
- [LCDREG](#): LCD Voltage Regulator Control Register
- [LCDREF](#): LCD Reference Ladder Control Register
- [LCDCTRL](#): LCD Automatic Control Register
- [LCDSTAT](#): LCD Automatic Status Register
- [LCDTEVNT](#): LCD Time Event Selection Register
- Three LCD Frame Counter Registers (LCDFC0:LCDFC2)
- [LCDSEx](#): LCD Segment x Enable Register (LCDSE3:LCDSE0)
- 32 LCD Data Registers (LCDDATA31:LCDDATA0)
- 32 LCD SDATA Registers (LCDSDATA31:LCDSDATA0)

The LCDCON register, shown in [Register 2-1](#), controls the overall operation of the module. Once the module is configured, the LCDEN (LCDCON[15]) bit is used to enable or disable the LCD module. The LCD panel can also operate during Sleep by clearing the SLPEN (LCDCON[6]) bit.

The LCDPS register, shown in [Register 2-2](#), configures the LCD clock source prescaler and the type of waveform: Type-A or Type-B. For details on these features, see [Section 4.0 “LCD Clock Source Selection”](#), [Table 15-1](#) and [Section 10.0 “LCD Waveform Generation”](#).

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**Register 2-1: LCDCON: LCD Control Register**

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
LCDEN	—	LCDSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/C-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SLPEN	WERR	CS[1:0]		LMUX[2:0]		
bit 7							bit 0

<b>Legend:</b>	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

bit 15      **LCDEN:** LCD Driver Enable bit

- 1 = LCD driver module is enabled
- 0 = LCD driver module is disabled

bit 14      **Unimplemented:** Read as '0'

bit 13      **LCDSIDL:** LCD Stop in CPU Idle Mode Control bit

- 1 = LCD driver halts in CPU Idle mode
- 0 = LCD driver continues to operate in CPU Idle mode

bit 12-7      **Unimplemented:** Read as '0'

bit 6      **SLPEN:** LCD Driver Enable in Sleep Mode bit

- 1 = LCD driver module is disabled in Sleep mode
- 0 = LCD driver module is enabled in Sleep mode

bit 5      **WERR:** LCD Write Failed Error bit

- 1 = LCDDATAx register is written while WA (LCDPS[4]) = 0 (must be cleared in software)
- 0 = No LCD write error

bit 4-3      **CS[1:0]:** Clock Source Select bits

- 00 = FRC
- 01 = LPRC
- 1x = SOSC

bit 2-0      **LMUX[2:0]:** LCD Commons Select bits

LMUX[2:0]	Multiplex	Bias
111	1/8 MUX (COM[7:0])	1/3
110	1/7 MUX (COM[6:0])	1/3
101	1/6 MUX (COM[5:0])	1/3
100	1/5 MUX (COM[4:0])	1/3
011	1/4 MUX (COM[3:0])	1/3
010	1/3 MUX (COM[2:0])	1/2 or 1/3
001	1/2 MUX (COM[1:0])	1/2 or 1/3
000	Static (COM0)	Static

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**Register 2-2: LCDPS: LCD Phase Register**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
WFT	BIASMD	LCDA	WA	LP[3:0]			
bit 7							bit 0

<b>Legend:</b>	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **WFT:** Waveform Type Select bit  
 1 = Type-B waveform (phase changes on each frame boundary)  
 0 = Type-A waveform (phase changes within each common type)

bit 6 **BIASMD:** Bias Mode Select bit  
When LMUX[2:0] = 000 or 011-111:  
 0 = Static Bias mode/1/3 Bias mode (do not set this bit to '1')  
When LMUX[2:0] = 001 or 010:  
 1 = 1/2 Bias mode  
 0 = 1/3 Bias mode

bit 5 **LCDA:** LCD Active Status bit  
 1 = LCD driver module is active  
 0 = LCD driver module is inactive

bit 4 **WA:** LCD Write Allow Status bit  
 1 = Write into the LCDDATAx registers is allowed  
 0 = Write into the LCDDATAx registers is not allowed

bit 3-0 **LP[3:0]:** LCD Prescaler Select bits  
 1111 = 1:16  
 1110 = 1:15  
 1101 = 1:14  
 1100 = 1:13  
 1011 = 1:12  
 1010 = 1:11  
 1001 = 1:10  
 1000 = 1:9  
 0111 = 1:8  
 0110 = 1:7  
 0101 = 1:6  
 0100 = 1:5  
 0011 = 1:4  
 0010 = 1:3  
 0001 = 1:2  
 0000 = 1:1

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## 3.0 LCD SEGMENT PINS CONFIGURATION

The LCDSE<sub>x</sub> registers configure the functions of the port pins. Setting the segment enable bit for a particular segment configures that pin as an LCD driver. There are four LCD Segment Enable registers, as shown in [Table 3-1](#). The prototype LCDSE<sub>x</sub> register is shown in [Register 3-1](#).

**Table 3-1: LCDSE<sub>x</sub> Registers and Associated Segments**

Register	Segments
LCDSE0	Seg 15:Seg 0
LCDSE1	Seg 31:Seg 16
LCDSE2	Seg 47:Seg 32
LCDSE3	Seg 63:Seg 48

Once the module is initialized for the LCD panel, the individual bits of the LCDDATA<sub>x</sub> registers are cleared, or set, to represent a clear or dark pixel, respectively.

Specific sets of LCDDATA<sub>x</sub> registers are used with specific segments and common signals. Each bit represents a unique combination of a specific segment connected to a specific common.

Individual LCDDATA<sub>x</sub> bits are named by the convention, “SxxCy”, with “xx” as the segment number and “y” as the common number. The relationship is summarized in [Register 2-2](#). The prototype LCDDATA<sub>x</sub> register is shown in [Register 3-2](#).

**Note:** Not all LCDSE<sub>x</sub> and LCDDATA<sub>x</sub> registers are implemented in all devices. Refer to the specific device data sheet for more details.

**Register 3-1: LCDSE<sub>x</sub>: LCD Segment x Enable Register**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SE(n+15)	SE(n+14)	SE(n+13)	SE(n+12)	SE(n+11)	SE(n+10)	SE(n+9)	SE(n+8)
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SE(n+7)	SE(n+6)	SE(n+5)	SE(n+4)	SE(n+3)	SE(n+2)	SE(n+1)	SE(n)
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as ‘0’

-n = Value at POR

‘1’ = Bit is set

‘0’ = Bit is cleared

x = Bit is unknown

bit 7-0 **SE(n+15):SE(n):** Segment Enable bits

For LCDSE0: n = 0

For LCDSE1: n = 16

For LCDSE2: n = 32

For LCDSE3: n = 48

1 = Segment function of the pin is enabled; digital I/O is disabled

0 = Segment function of the pin is disabled

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**Register 3-2: LCDDATAx: LCD Data x Registers**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
S(n+15)Cy	S(n+14)Cy	S(n+13)Cy	S(n+12)Cy	S(n+11)Cy	S(n+10)Cy	S(n+9)Cy	S(n+8)Cy
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
S(n+7)Cy	S(n+6)Cy	S(n+5)Cy	S(n+4)Cy	S(n+3)Cy	S(n+2)Cy	S(n+1)Cy	S(n)Cy
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-0                      **S(n+15)Cy:S(n)Cy:** Pixel On bits

For registers, LCDDATA0 through LCDDATA3:  $n = (16x)$ ,  $y = 0$   
For registers, LCDDATA4 through LCDDATA7:  $n = (16(x - 4))$ ,  $y = 1$   
For registers, LCDDATA8 through LCDDATA11:  $n = (16(x - 8))$ ,  $y = 2$   
For registers, LCDDATA12 through LCDDATA15:  $n = (16(x - 12))$ ,  $y = 3$   
For registers, LCDDATA16 through LCDDATA19:  $n = (16(x - 16))$ ,  $y = 4$   
For registers, LCDDATA20 through LCDDATA23:  $n = (16(x - 20))$ ,  $y = 5$   
For registers, LCDDATA24 through LCDDATA27:  $n = (16(x - 24))$ ,  $y = 6$   
For registers, LCDDATA28 through LCDDATA31:  $n = (16(x - 28))$ ,  $y = 7$   
1 = Pixel on  
0 = Pixel off

**Table 3-2: LCDDATAx Registers and Bits for Segment and COM Combinations**

COM Lines	Segments			
	0 to 15	16 to 31	32 to 47	48 to 64
0	LCDDATA0 S00C0:S15C0	LCDDATA1 S16C0:S31C0	LCDDATA2 S32C0:S47C0	LCDDATA3 S48C0:S63C0
1	LCDDATA4 S00C1:S15C1	LCDDATA5 S16C1:S31C1	LCDDATA6 S32C1:S47C1	LCDDATA7 S48C1:S63C1
2	LCDDATA8 S00C2:S15C2	LCDDATA9 S16C2:S31C2	LCDDATA10 S32C2:S47C2	LCDDATA11 S48C2:S63C2
3	LCDDATA12 S00C3:S15C3	LCDDATA13 S16C3:S31C3	LCDDATA14 S32C3:S47C3	LCDDATA15 S48C3:S63C3
4	LCDDATA16 S00C4:S15C4	LCDDATA17 S16C4:S31C4	LCDDATA18 S32C4:S47C4	LCDDATA19 S48C4:S63C4
5	LCDDATA20 S00C5:S15C5	LCDDATA21 S16C5:S31C5	LCDDATA22 S32C5:S47C5	LCDDATA23 S48C5:S63C5
6	LCDDATA24 S00C6:S15C6	LCDDATA25 S16C6:S31C6	LCDDATA26 S32C6:S47C6	LCDDATA27 S48C6:S63C6
7	LCDDATA28 S00C7:S15C7	LCDDATA29 S16C7:S31C7	LCDDATA30 S32C7:S47C7	LCDDATA31 S48C7:S63C7

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## 4.0 LCD CLOCK SOURCE SELECTION

The LCD driver module has three possible clock sources:

- FRC/8192
- SOSC Clock/32
- LPRC/32

The first clock source is the 8 MHz Fast Internal RC (FRC) oscillator, divided by 8,192. This divider ratio is chosen to provide about 1 kHz output. The divider is not programmable. Instead, the LCD Prescaler Select bits, LCDPS[3:0], are used to set the LCD frame clock rate.

The second clock source is the SOSC oscillator/32. This also outputs about 1 kHz when a 32.768 kHz crystal is used with the SOSC oscillator. To use the SOSC oscillator as a clock source, set the SOSSEN (OSCCON[1]) bit.

The third clock source is a 31.25 kHz internal LPRC oscillator/32 that provides approximately 1 kHz output.

The second and third clock sources may be used to continue running the LCD while the processor is in Sleep.

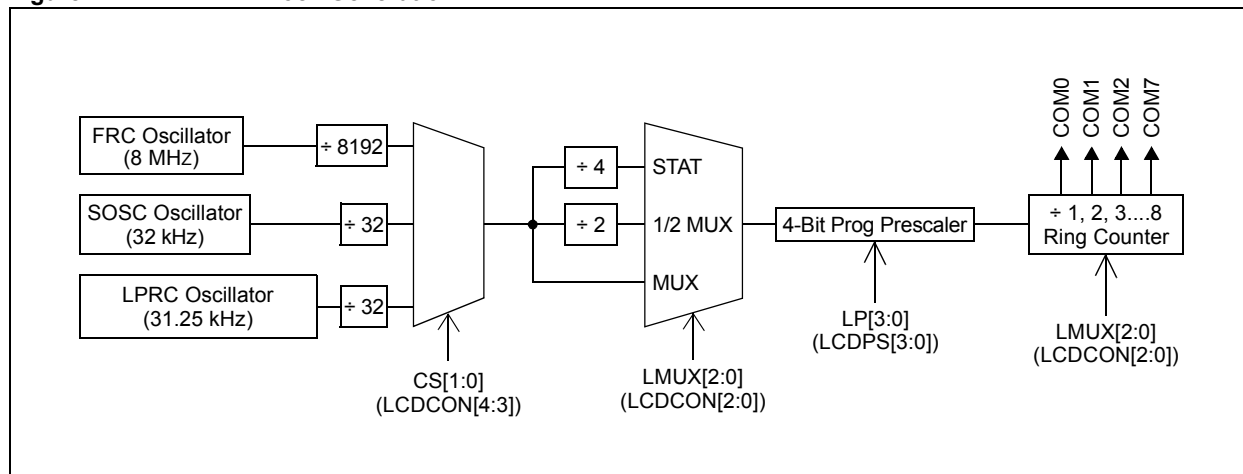
These clock sources are selected through the bits, CS[1:0] (LCDCON[4:3]).

### 4.1 LCD Prescaler

A 16-bit counter is available as a prescaler for the LCD clock. The prescaler is not directly readable or writable. Its value is set by the LP[3:0] bits (LCDPS[3:0]) that determine the prescaler assignment and prescale ratio.

Selectable prescale values are from 1:1 through 1:16, in increments of one.

Figure 4-1: LCD Clock Generation





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## 5.0 LCD BIAS TYPES

The LCD module can be configured in one of three Bias types:

- Static Bias (Two Voltage Levels: VSS and VDD)
- 1/2 Bias (Three Voltage Levels: VSS, 1/2 VDD and VDD)
- 1/3 Bias (Four Voltage Levels: VSS, 1/3 VDD, 2/3 VDD and VDD)

LCD Bias voltages can be generated with an internal resistor ladder, internal Bias generator or external resistor ladder.

### 5.1 Internal Resistor Biasing

This mode does not use external resistors, but rather, internal resistor ladders that are configured to generate the Bias voltage.

The internal reference ladder actually consists of three separate ladders. Disabling the internal reference ladder disconnects all of the ladders, allowing external voltages to be supplied.

Depending on the total resistance of the resistor ladders, the Biasing can be classified as low, medium or high power.

[Table 5-1](#) shows the total resistance of each of the ladders. [Figure 5-1](#) shows the internal resistor ladder connections. When the internal resistor ladder is selected, the Bias voltage will be internal; it can also provide software contrast control (using LCDCST[2:0]).

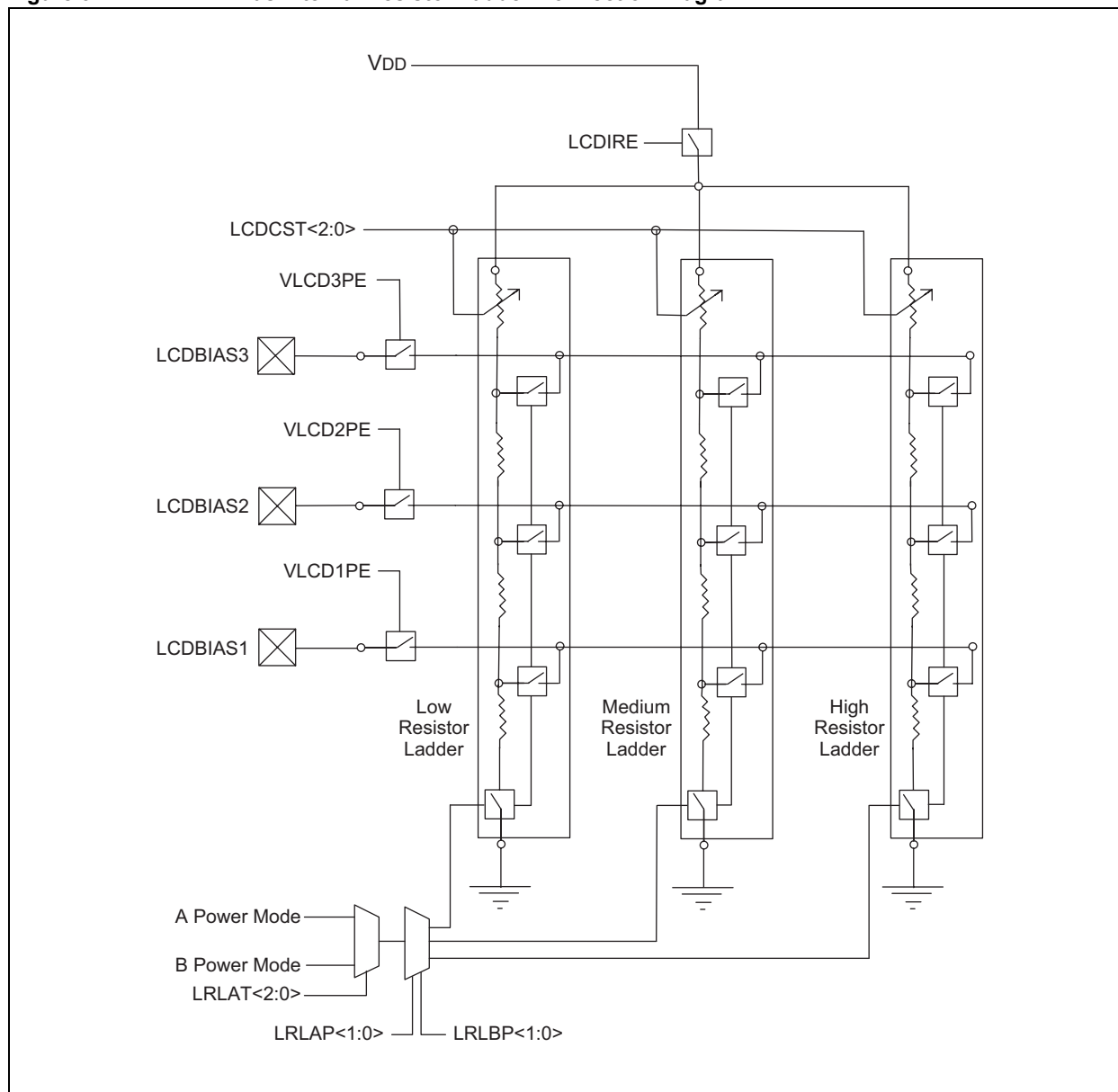
**Note:** Depending on the LCD glass and resistor ladder selected, the bias capacitors may have to be changed in order to allow the charge pump to boost LCD voltage. Please refer to [Section 5.3 “Bias Configurations”](#).

**Table 5-1: Internal Resistance Ladder Power Modes**

Power Mode	Nominal Resistance of Entire Ladder	IDD
Low	3 MΩ	1 μA
Medium	300 kΩ	10 μA
High	30 kΩ	100 μA

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Figure 5-1: LCD Bias Internal Resistor Ladder Connection Diagram



There are two power modes, designated as “Mode A” and “Mode B”. Mode A is set by the bits, LRLAP[1:0], and Mode B by the LRLBP[1:0] bits. The resistor ladder to use for Modes A and B are selected by the bits, LRLAP[1:0] and LRLBP[1:0], respectively.

Each ladder has a matching contrast control ladder, tuned to the nominal resistance of the reference ladder. This contrast control resistor can be controlled by the LCDCST[2:0] bits (LCDREF[13:11]). Disabling the internal reference ladder results in all of the ladders being disconnected, allowing external voltages to be supplied.

To get additional current in High-Power mode, when LRLAP[1:0] (LCDREF[7:6]) = 11, both the medium and high-power resistor ladders are activated.

Whenever the LCD module is inactive (LCDA (LCDPS[5]) = 0), the reference ladder will be turned off.

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## 5.1.1 AUTOMATIC POWER MODE SWITCHING

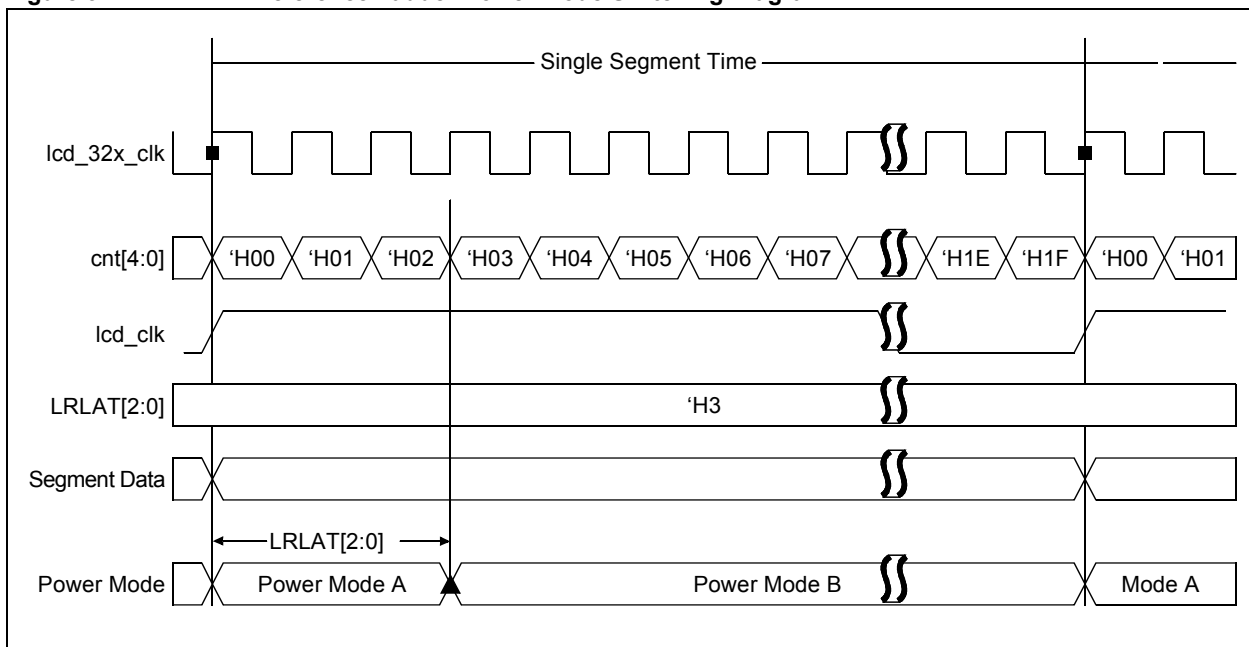
As an LCD segment is electrically only a capacitor, current is drawn only during the interval when the voltage is switching. To minimize total device current, the LCD reference ladder can be operated in a different power mode for the transition portion of the duration. This is controlled by the LCDREF register.

Mode A Power mode is active for a programmable time, beginning at the time when the LCD segment waveform is transitioning. The LRLAT[2:0] (LCDREF[2:0]) bits select how long the transition or if Mode A is active. Mode B Power mode is active for the remaining time before the segments or commons change again.

As shown in Figure 5-2, there are 32 counts in a single segment time. Type-A can be chosen during the time when the waveform is in transition. Type-B can be used when the clock is stable or not in transition.

By using this feature of automatic power switching using Type-A/Type-B, the power consumption can be optimized for a given contrast.

**Figure 5-2: LCD Reference Ladder Power Mode Switching Diagram**

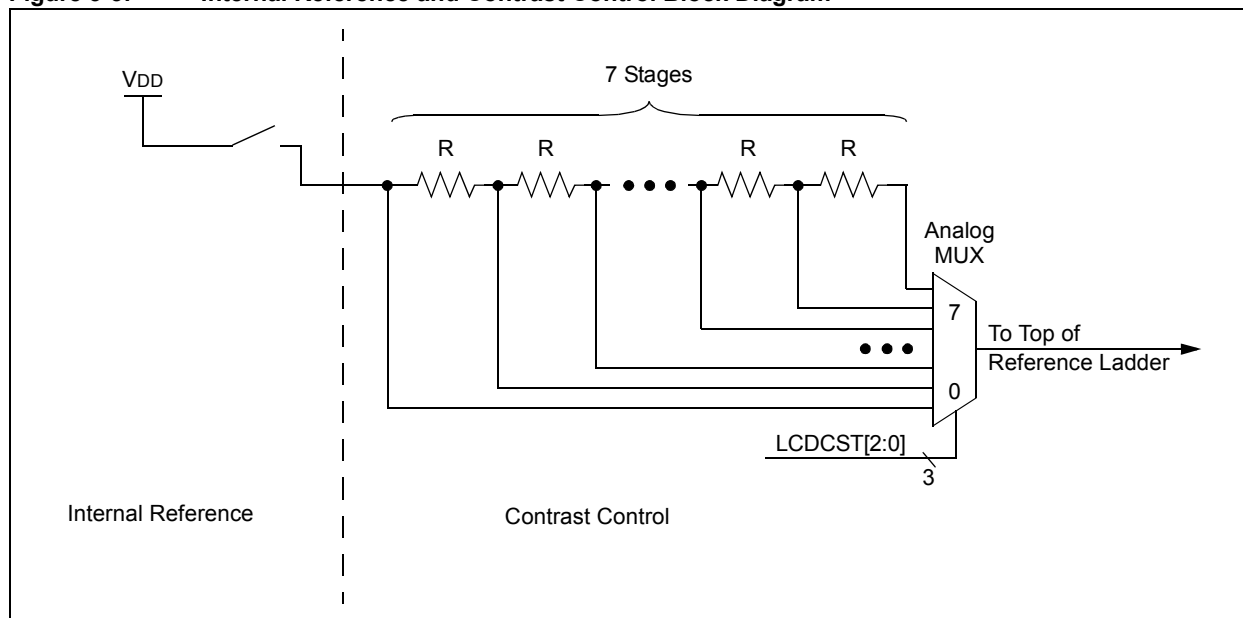


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## 5.1.2 CONTRAST CONTROL

The LCD contrast control circuit consists of a 7-tap resistor ladder, controlled by the LCDCST[2:0] bits (see [Figure 5-3](#)).

**Figure 5-3: Internal Reference and Contrast Control Block Diagram**



## 5.1.3 INTERNAL REFERENCE

Under firmware control, an internal reference for the LCD Bias voltages can be enabled. When enabled, the source of this voltage can be VDD.

When no internal reference is selected, the LCD contrast control circuit is disabled and the LCD Bias must be provided externally. Whenever the LCD module is inactive (LCDA = 0), the internal reference will be turned off.

## 5.1.4 VLCDxPE PINS

The VLCD3PE, VLCD2PE and VLCD1PE bits provide the ability for an external LCD Bias network to be used instead of the internal ladder. Use of the VLCDxPE bits does not prevent use of the internal ladder.

Each VLCDxPE bit has an independent control in the LCDREF register, allowing access to any or all of the LCD Bias signals.

This architecture allows for maximum flexibility in different applications. The VLCDxPE bits could be used to add capacitors to the internal reference ladder for increasing the drive capacity. For applications where the internal contrast control is insufficient, the firmware can choose to enable only the VLCD3PE bit, allowing an external contrast control circuit to use the internal reference divider.

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**Register 5-1: LCDREF: LCD Reference Ladder Control Register**

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LCDIRE	—	LDCDST[2:0]			VLCD3PE	VLCD2PE	VLCD1PE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
LRLAP[1:0]		LRLBP[1:0]		—	LRLAT[2:0]		
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15      **LCDIRE:** LCD Internal Reference Enable bit  
             1 = Internal LCD reference is enabled and connected to the internal contrast control circuit  
             0 = Internal LCD reference is disabled
- bit 14      **Unimplemented:** Read as '0'
- bit 13-11   **LDCST[2:0]:** LCD Contrast Control bits  
             Selects the Resistance of the LCD Contrast Control Resistor Ladder:  
             111 = Resistor ladder is at maximum resistance (minimum contrast)  
             110 = Resistor ladder is at 6/7th of maximum resistance  
             101 = Resistor ladder is at 5/7th of maximum resistance  
             100 = Resistor ladder is at 4/7th of maximum resistance  
             011 = Resistor ladder is at 3/7th of maximum resistance  
             010 = Resistor ladder is at 2/7th of maximum resistance  
             001 = Resistor ladder is at 1/7th of maximum resistance  
             000 = Minimum resistance (maximum contrast); resistor ladder is shorted
- bit 10      **VLCD3PE:** LCD Bias 3 Pin Enable bit  
             1 = Bias 3 level is connected to the external pin, LCDBIAS3  
             0 = Bias 3 level is internal (internal resistor ladder)
- bit 9        **VLCD2PE:** LCD Bias 2 Pin Enable bit  
             1 = Bias 2 level is connected to the external pin, LCDBIAS2  
             0 = Bias 2 level is internal (internal resistor ladder)
- bit 8        **VLCD1PE:** LCD Bias 1 Pin Enable bit  
             1 = Bias 1 level is connected to the external pin, LCDBIAS1  
             0 = Bias 1 level is internal (internal resistor ladder)
- bit 7-6      **LRLAP[1:0]:** LCD Reference Ladder A Time Power Control bits  
             During Time Interval A:  
             11 = Internal LCD reference ladder is powered in High-Power mode  
             10 = Internal LCD reference ladder is powered in Medium Power mode  
             01 = Internal LCD reference ladder is powered in Low-Power mode  
             00 = Internal LCD reference ladder is powered down and unconnected
- bit 5-4      **LRLBP[1:0]:** LCD Reference Ladder B Time Power Control bits  
             During Time Interval B:  
             11 = Internal LCD reference ladder is powered in High-Power mode  
             10 = Internal LCD reference ladder is powered in Medium Power mode  
             01 = Internal LCD reference ladder is powered in Low-Power mode  
             00 = Internal LCD reference ladder is powered down and unconnected
- bit 3        **Unimplemented:** Read as '0'

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## Register 5-1: LCDREF: LCD Reference Ladder Control Register (Continued)

bit 2-0

**LRLAT[2:0]:** LCD Reference Ladder A Time Interval Control bits

Sets the number of 32 clock counts when the A Time Interval Power mode is active.

For Type-A Waveforms (WFT = 0):

111 = Internal LCD reference ladder is in A Power mode for 7 clocks and B Power mode for 9 clocks  
110 = Internal LCD reference ladder is in A Power mode for 6 clocks and B Power mode for 10 clocks  
101 = Internal LCD reference ladder is in A Power mode for 5 clocks and B Power mode for 11 clocks  
100 = Internal LCD reference ladder is in A Power mode for 4 clocks and B Power mode for 12 clocks  
011 = Internal LCD reference ladder is in A Power mode for 3 clocks and B Power mode for 13 clocks  
010 = Internal LCD reference ladder is in A Power mode for 2 clocks and B Power mode for 14 clocks  
001 = Internal LCD reference ladder is in A Power mode for 1 clock and B Power mode for 15 clocks  
000 = Internal LCD reference ladder is always in B Power mode

For Type-B Waveforms (WFT = 1):

111 = Internal LCD reference ladder is in A Power mode for 7 clocks and B Power mode for 25 clocks  
110 = Internal LCD reference ladder is in A Power mode for 6 clocks and B Power mode for 26 clocks  
101 = Internal LCD reference ladder is in A Power mode for 5 clocks and B Power mode for 27 clocks  
100 = Internal LCD reference ladder is in A Power mode for 4 clocks and B Power mode for 28 clocks  
011 = Internal LCD reference ladder is in A Power mode for 3 clocks and B Power mode for 29 clocks  
010 = Internal LCD reference ladder is in A Power mode for 2 clocks and B Power mode for 30 clocks  
001 = Internal LCD reference ladder is in A Power mode for 1 clock and B Power mode for 31 clocks  
000 = Internal LCD reference ladder is always in B Power mode

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## 5.2 LCD Bias Generation

The LCD driver module is capable of generating the required Bias voltages for LCD operation with a minimum of external components. This includes the ability to generate the different voltage levels required by the different Bias types that are required by the LCD. The driver module can also provide Bias voltages, both above and below the microcontroller VDD, through the use of an on-chip LCD voltage regulator.

### 5.2.1 LCD BIAS TYPES

There is support for three Bias types based on the waveforms generated to control segments and commons:

- Static (two discrete levels)
- 1/2 Bias (three discrete levels)
- 1/3 Bias (four discrete levels)

The use of different waveforms in driving the LCD is discussed in more detail in [Section 10.0 “LCD Waveform Generation”](#).

### 5.2.2 LCD VOLTAGE REGULATOR

The purpose of the LCD regulator is to provide proper Bias voltage and good contrast for the LCD, regardless of VDD levels. This module contains a charge pump and internal voltage reference. The regulator can be configured by using external components to boost Bias voltage above VDD. It can also operate a display at a constant voltage below VDD. The regulator can also be selectively disabled to allow Bias voltages to be generated by an external resistor network.

The LCD regulator is controlled through the LCDREG register ([Register 5-2](#)). It is enabled or disabled using the CKSEL[1:0] bits, while the charge pump can be selectively enabled using the CPEN bit. When the regulator is enabled, the MODE13 bit is used to select the Bias type. The peak LCD Bias voltage, measured as a difference between the potentials of LCDBIAS3 and LCDBIAS0, is configured with the BIAS[2:0] bits.

# dsPIC33/PIC24 Family Reference Manual

**Register 5-2: LCDREG: LCD Voltage Regulator Control Register**

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
CPEN	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
—	—	BIAS[2:0] <sup>(1)</sup>			MODE13 <sup>(1)</sup>	CKSEL[1:0]	
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **CPEN:** LCD Charge Pump Enable bit

1 = Charge pump enabled; highest LCD Bias voltage is 3.6V

0 = Charge pump disabled; highest LCD Bias voltage is AVDD

bit 14-6 **Unimplemented:** Read as '0'

bit 5-3 **BIAS[2:0]:** Regulator Voltage Output Control bits<sup>(1)</sup>

111 = 3.60V peak (offset on LCDBIAS0 of 0V)

110 = 3.47V peak (offset on LCDBIAS0 of 0.13V)

101 = 3.34V peak (offset on LCDBIAS0 of 0.26V)

100 = 3.21V peak (offset on LCDBIAS0 of 0.39V)

011 = 3.08V peak (offset on LCDBIAS0 of 0.52V)

010 = 2.95V peak (offset on LCDBIAS0 of 0.65V)

001 = 2.82V peak (offset on LCDBIAS0 of 0.78V)

000 = 2.69V peak (offset on LCDBIAS0 of 0.91V)

bit 2 **MODE13:** 1/3 LCD Bias Enable bit<sup>(1)</sup>

1 = Regulator output supports 1/3 LCD Bias mode

0 = Regulator output supports Static LCD Bias mode

bit 1-0 **CKSEL[1:0]:** Regulator Clock Source Select bits

11 = 31 kHz LPRC

10 = 8 MHz FRC

01 = SOSC

00 = LCD regulator is disabled

**Note 1:** In some of the newer devices, these bits are not implemented. Please check the data sheet to see if these bits are implemented. In the new charge pump design, the intermediate voltages (LCDBIAS2 and LCDBIAS1) are generated from the internal resistor ladder. Bias configuration, explained in [Section 5.3 "Bias Configurations"](#), is not valid for the new charge pump. In the new charge pump, the LCDBIAS3 voltage is generated and connected to the top of the internal resistor ladder. In this Charge Pump mode, the LCDBIAS0 should be grounded.



# Liquid Crystal Display (LCD)

## 5.3 Bias Configurations

The dsPIC33/PIC24 family devices have four distinct circuit configurations for LCD Bias generation:

- M0: Regulator with Boost
- M1: Regulator without Boost
- M2: Resistor Ladder with Software Contrast
- M3: Resistor Ladder with Hardware Contrast

### 5.3.1 M0 (REGULATOR WITH BOOST)

In M0 operation, the LCD charge pump feature is enabled. This allows the regulator to generate voltages up to +3.6V to the LCD (as measured at LCDBIAS3).

M0 uses a Flyback Capacitor connected between V<sub>LCAP1</sub> and V<sub>LCAP2</sub>, as well as filter capacitors on LCDBIAS0 through LCDBIAS3, to obtain the required voltage boost (Figure 5-4). The output voltage (V<sub>BIAS</sub>) is the difference of the potential between LCDBIAS3 and LCDBIAS0. It is set by the BIAS[2:0] bits, which adjust the offset between LCDBIAS0 and V<sub>SS</sub>. The Flyback Capacitor (C<sub>FLY</sub>) acts as a charge storage element for large LCD loads. This mode is useful in those cases where the voltage requirements of the LCD are higher than the microcontroller's V<sub>DD</sub>. It also permits software control of the display's contrast, by adjustment of the Bias voltage, by changing the value of the BIAS<sub>x</sub> bits. Example 5-1 demonstrates how to set up charge pump M0 mode in new devices without the BIAS[2:0] (LCDREG[5:3]) bits.

M0 supports Static and 1/3 Bias types. Generation of the voltage levels for 1/3 Bias is handled automatically, but must be configured in software.

M0 is enabled by selecting a valid regulator clock source (CKSEL[1:0] set to any value except '00') and setting the CPEN bit. If a Static Bias type is required, the MODE13 bit must be cleared.

#### Example 5-1: Basic LCD and M0 Mode Configuration for Devices without BIAS[2:0] Bits

```
IFS6bits.LCDIF = 0;
LCDPSbits.LP = 2;           //frame clock pre-scaler
LCDSE0 = 0x013F;           //enable segments 0, 1, 2, 3, 4, 5, & 8
LCDSE1bits.SE18 = 1;       //enable segment 18

LCDREFbits.LCDIRE = 1;     //enable internal LCD Reference
LCDREFbits.LRLBP = 0x01;  //Interval B Low Power mode Ref ladder

LCDREG = 0x8001;           //Charge pump enable and LPRC clock select
LCDCON = 0x800F;           ///LCD enable with LPRC clock and 1/8 mux, 1/3 Bias

//Write Primary Memory to light pixels
LCDDATA0bits.S04C0 = 1;    //seg4 COM0
LCDDATA1bits.S18C0 = 1;    //seg18 COM0
```

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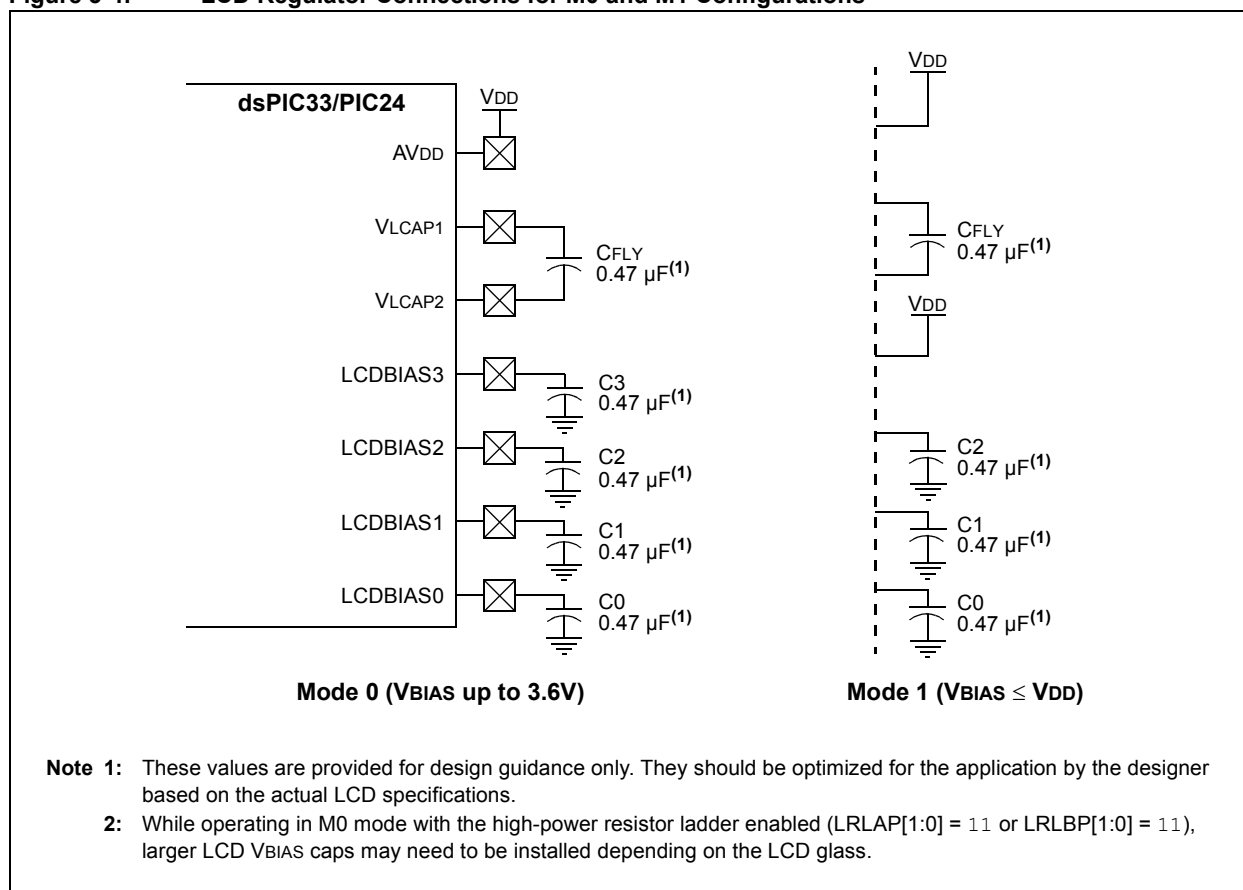
## 5.3.2 M1 (REGULATOR WITHOUT BOOST)

M1 operation is similar to M0, but does not use the LCD charge pump. It can provide VBIAS up to the voltage level supplied directly to LCDBIAS3. It can be used in cases where VDD for the application is expected to never drop below a level that can provide adequate contrast for the LCD. The connection of external components is very similar to M0, except that LCDBIAS3 must be tied directly to VDD (Figure 5-4).

**Note:** When the device is put to Sleep while operating in M0 or M1 mode, make sure that the Bias capacitors are fully discharged to get the lowest Sleep current.

- The BIAS[2:0] bits can still be used to adjust contrast in software by changing VBIAS. As with M0, changing these bits changes the offset between LCDBIAS0 and Vss. In M1, this is reflected in the change between the LCDBIAS0 and the voltage tied to LCDBIAS3. Thus, if VDD should change, VBIAS will also change; where in M0, the level of VBIAS is constant.
- Like M0, M1 supports Static and 1/3 Bias types. Generation of the voltage levels for 1/3 Bias is handled automatically, but must be configured in software. M1 is enabled by selecting a valid regulator clock source (CKSEL[1:0] set to any value except '00') and clearing the CPEN bit. If 1/3 Bias type is required, the MODE13 bit should also be set.

Figure 5-4: LCD Regulator Connections for M0 and M1 Configurations<sup>(2)</sup>



# Liquid Crystal Display (LCD)

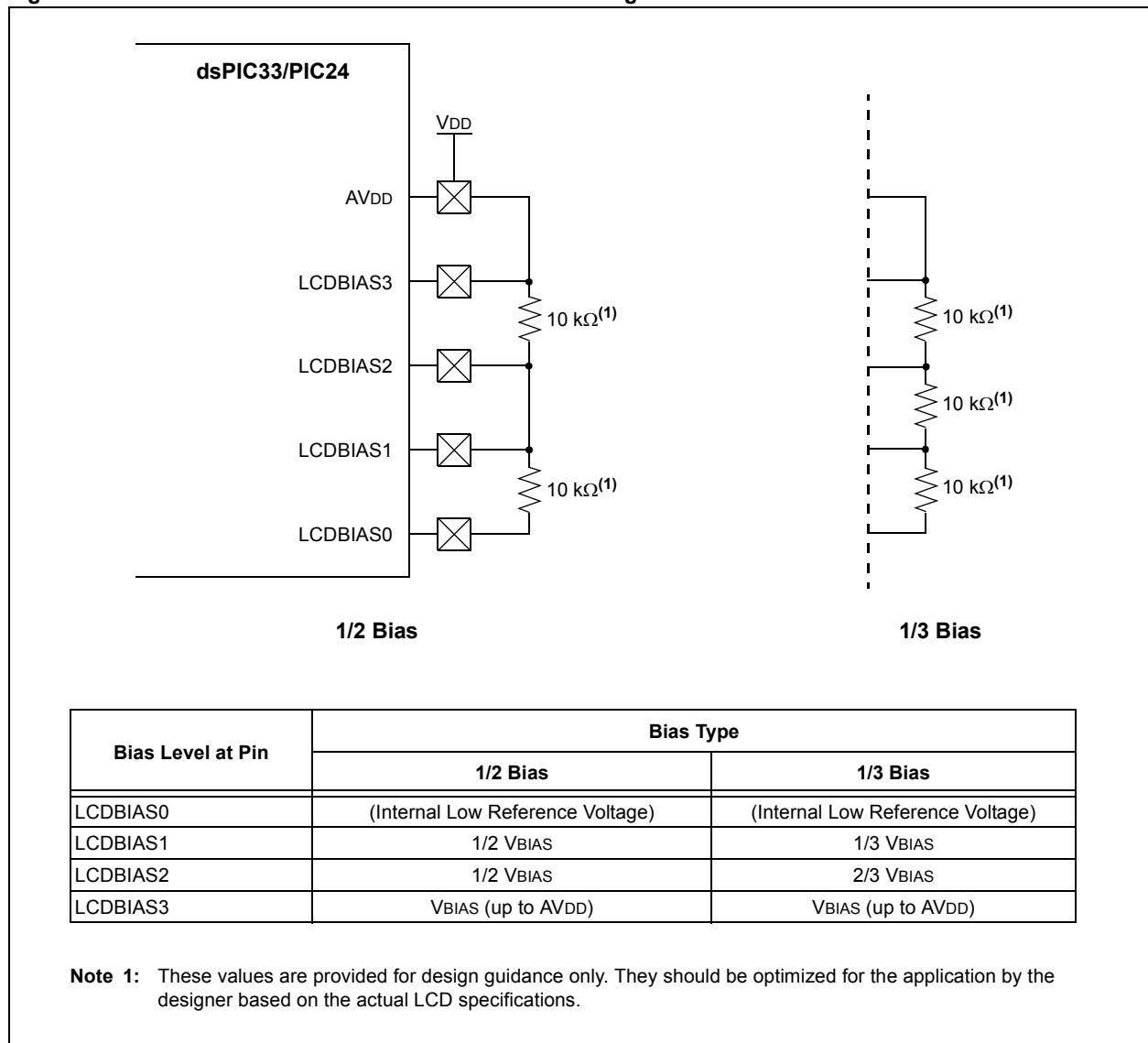
## 5.3.3 M2 (RESISTOR LADDER WITH SOFTWARE CONTRAST)

M2 operation also uses the LCD regulator but disables the charge pump. The regulator's internal voltage reference remains active as a way to regulate contrast. It is used in cases where the current requirements of the LCD exceed the capacity of the regulator's charge pump.

In this configuration, the LCD Bias voltage levels are created by an external resistor voltage divider, connected across LCDBIAS0 through LCDBIAS3, with the top of the divider tied to VDD (Figure 5-5). The potential at the bottom of the ladder is determined by the LCD regulator's voltage reference, tied internally to LCDBIAS0. The Bias type is determined by the voltages on the LCDBIASx pins, which are controlled by the configuration of the resistor ladder. Most applications using M2 will use a 1/3 or 1/2 Bias type. While Static Bias can also be used, it offers extremely limited contrast range and additional current consumption over other Bias Generation modes.

Like M1, the LCDBIASx pins can be used to control contrast, limited by the level of VDD supplied to the device. Also, since there is no capacitor required across VLCAP1 and VLCAP2, these pins are available as digital I/O ports: RG2 and RG3. M2 is selected by clearing the CKSEL[1:0] bits and setting the CPEN bit.

**Figure 5-5: Resistor Ladder Connections for M2 Configuration**



# dsPIC33/PIC24 Family Reference Manual

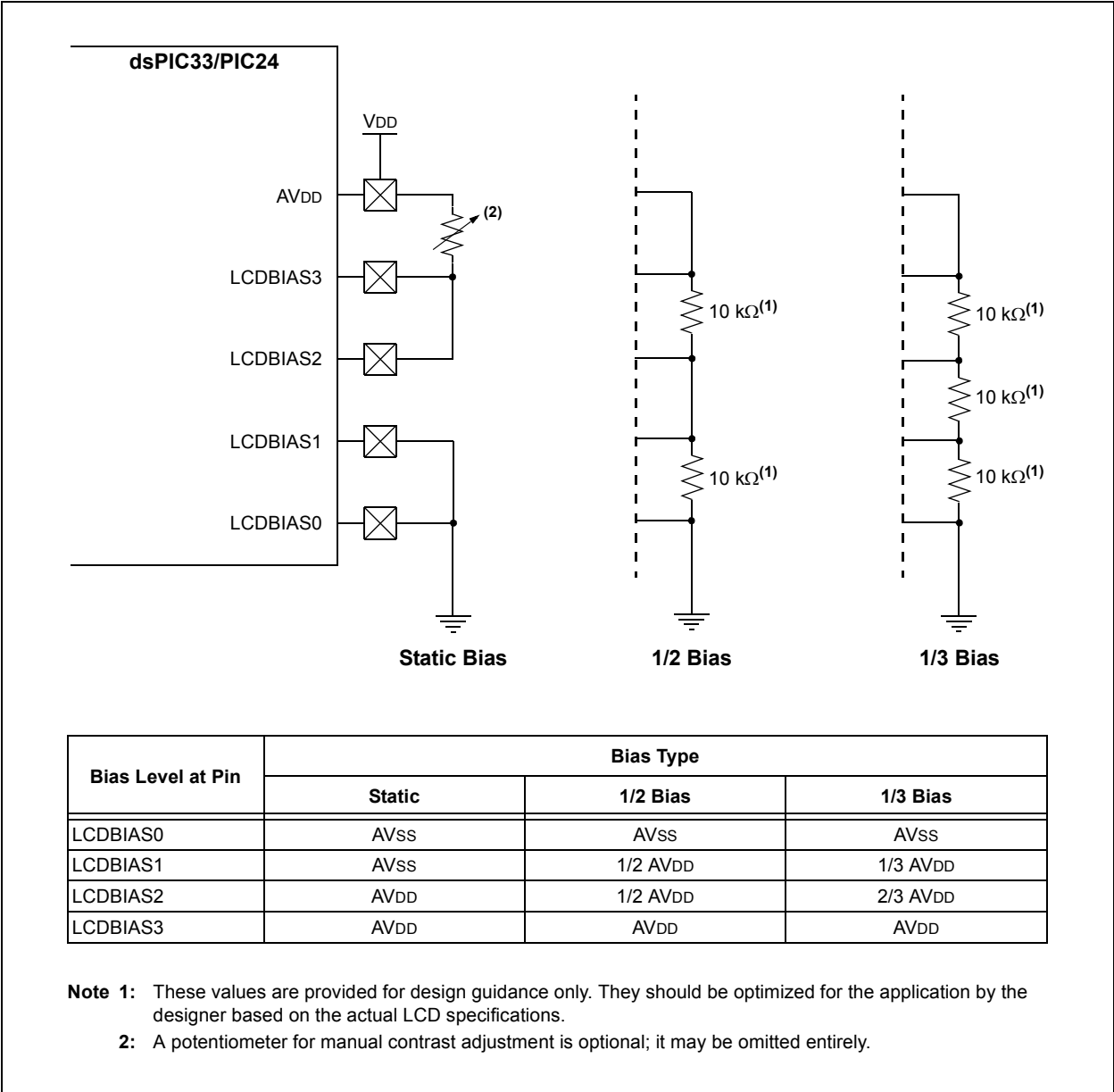
## 5.3.4 M3 (RESISTOR LADDER WITH HARDWARE CONTRAST)

In M3, the LCD regulator is completely disabled. Like M2, LCD Bias levels are tied to AVDD and are generated using an external divider. The difference is that the internal voltage reference is also disabled and the bottom of the ladder is tied to ground (VSS) (see Figure 5-6). The value of the resistors, and the difference between VSS and VDD, determine the contrast range; no software adjustment is possible. This configuration is also used where the LCD module's current requirements exceed the capacity of the charge pump and software contrast control is not needed.

Depending on the Bias type required, resistors are connected between some or all of the pins. A potentiometer can also be connected between LCDBIAS3 and VDD to allow for hardware controlled contrast adjustment.

M3 is selected by clearing the CKSEL[1:0] and CPEN bits.

Figure 5-6: Resistor Ladder Connections for M3 Configuration



# Liquid Crystal Display (LCD)

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## 5.4 Design Considerations for the LCD Charge Pump

When designing applications that use the LCD regulator with the charge pump enabled, users must always consider both the dynamic current and RMS (Static) current requirements of the display, and what the charge pump can deliver. Both dynamic and Static current can be determined by [Equation 5-1](#):

**Equation 5-1:**

$$I = C \times \frac{dV}{dT}$$

For dynamic current, C is the value of the capacitors attached to LCDBIAS3 and LCDBIAS2. The variable, dV, is the voltage drop allowed on C2 and C3 during a voltage switch on the LCD display, and dT is the duration of the transient current after a clock pulse occurs.

For practical design purposes, these will be assumed to be 0.047  $\mu$ F for C, 0.1V for dV and 1  $\mu$ s for dT. This yields a dynamic current of 4.7 mA for 1  $\mu$ s.

RMS (Root Mean Square) current is determined by the value of C<sub>FLY</sub> for C, the voltage across VLCAP1 and VLCAP2 for dV, and the regulator clock period (T<sub>PER</sub>) for dT. Assuming a C<sub>FLY</sub> value of 0.047  $\mu$ F, a value of 1.02V across C<sub>FLY</sub> and a T<sub>PER</sub> of 30, the maximum theoretical Static current will be 1.8 mA. Since the charge pump must charge five capacitors, the maximum current becomes 360  $\mu$ A.

For a real-world assumption of 50% efficiency, this yields a practical current of 180  $\mu$ A. Users should compare the calculated current capacity against the requirements of the LCD. While dV and dT are relatively fixed by device design, the values of C<sub>FLY</sub> and the capacitors on the LCDBIASx pins can be changed to increase or decrease current. As always, any changes should be evaluated in the actual circuit for their impact on the application.

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## 6.0 LCD MULTIPLEX TYPES

The LCD driver module can be configured into four Multiplex types:

- Static (only COM0 used)
- 1/2 Multiplex (COM0 and COM1 are used)
- 1/3 Multiplex (COM0, COM1 and COM2 are used)
- 1/4 Multiplex (COM0, COM1, COM2 and COM3 are used)
- 1/5 Multiplex (COM0, COM1, COM2, COM3 and COM4 are used)
- 1/6 Multiplex (COM0, COM1, COM2, COM3, COM4 and COM5 are used)
- 1/7 Multiplex (COM0, COM1, COM2, COM3, COM4, COM5 and COM6 are used)
- 1/8 Multiplex (COM0, COM1, COM2, COM3, COM4, COM5, COM6 and COM7 are used)

The LMUX[2:0] bits setting (LCDCON[2:0]) decides the function of the COM pins. (For details, see [Table 6-1](#).)

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. If the pin is a COM drive, the TRIS setting of that pin is overridden.

**Note:** On a Power-on Reset, the LMUX[2:0] bits are '000'.

**Table 6-1:** COM[7:0] Pin Function

LMUX[2:0]	COM7 Pin	COM6 Pin	COM5 Pin	COM4 Pin	COM3 Pin	COM2 Pin	COM1 Pin	COM0 Pin
111	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
110	I/O Pin	COM6	COM5	COM4	COM3	COM2	COM1	COM0
101	I/O Pin	I/O Pin	COM5	COM4	COM3	COM2	COM1	COM0
100	I/O Pin	I/O Pin	I/O Pin	COM4	COM3	COM2	COM1	COM0
011	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM3	COM2	COM1	COM0
010	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM2	COM1	COM0
001	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM1	COM0
000	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM0

**Note:** Pins, COM[7:4], can also be used as SEG pins when 1/4 Multiplex to Static Multiplex are used. These pins can be used as I/O pins only if the respective bits in the LCDSEx registers are set to '0'.

# Liquid Crystal Display (LCD)

## 7.0 SEGMENT ENABLES

The LCDSEx registers are used to select the pin function for each segment pin. The selection allows each pin to operate as either an LCD segment driver or a digital only pin. To configure the pin as a segment driver, the corresponding bits in the LCDSEx registers must be set to '1'.

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. Any bit set in the LCDSEx registers overrides any bit settings in the corresponding TRIS register.

**Note:** On a Power-on Reset, these pins are configured as digital I/Os.

## 8.0 PIXEL CONTROL

The LCDDATAx registers contain bits that define the state of each pixel. Each bit defines one unique pixel. Table 3-2 shows the correlation of each bit in the LCDDATAx registers to the respective common and segment signals.

Any LCD pixel location not being used for display can be used as general purpose RAM.

## 9.0 LCD FRAME FREQUENCY

The rate at which the COM and SEG outputs change is called the LCD frame frequency.

**Table 9-1: Frame Frequency Formulas**

Multiplex	Frame Frequency =
Static (000)	$\text{Clock Source}/(4 \times 1 \times (\text{LP}[3:0] + 1))$
1/2 (001)	$\text{Clock Source}/(2 \times 2 \times (\text{LP}[3:0] + 1))$
1/3 (010)	$\text{Clock Source}/(1 \times 3 \times (\text{LP}[3:0] + 1))$
1/4 (011)	$\text{Clock Source}/(1 \times 4 \times (\text{LP}[3:0] + 1))$
1/5 (100)	$\text{Clock Source}/(1 \times 5 \times (\text{LP}[3:0] + 1))$
1/6 (101)	$\text{Clock Source}/(1 \times 6 \times (\text{LP}[3:0] + 1))$
1/7 (110)	$\text{Clock Source}/(1 \times 7 \times (\text{LP}[3:0] + 1))$
1/8 (111)	$\text{Clock Source}/(1 \times 8 \times (\text{LP}[3:0] + 1))$

**Note:** The clock source is FRC/8192, SOSC/32 or LPRC/32.

## 10.0 LCD WAVEFORM GENERATION

LCD waveform generation is based on the philosophy that the net AC voltage across the dark pixel should be maximized and the net AC voltage across the clear pixel should be minimized. The net DC voltage across any pixel should be zero.

The COM signal represents the time slice for each common, while the SEG contains the pixel data.

The pixel signal (COM-SEG) will have no DC component and can take only one of the two RMS values. The higher RMS value will create a dark pixel and a lower RMS value will create a clear pixel.

As the number of commons increases, the delta between the two RMS values decreases. The delta represents the maximum contrast that the display can have.

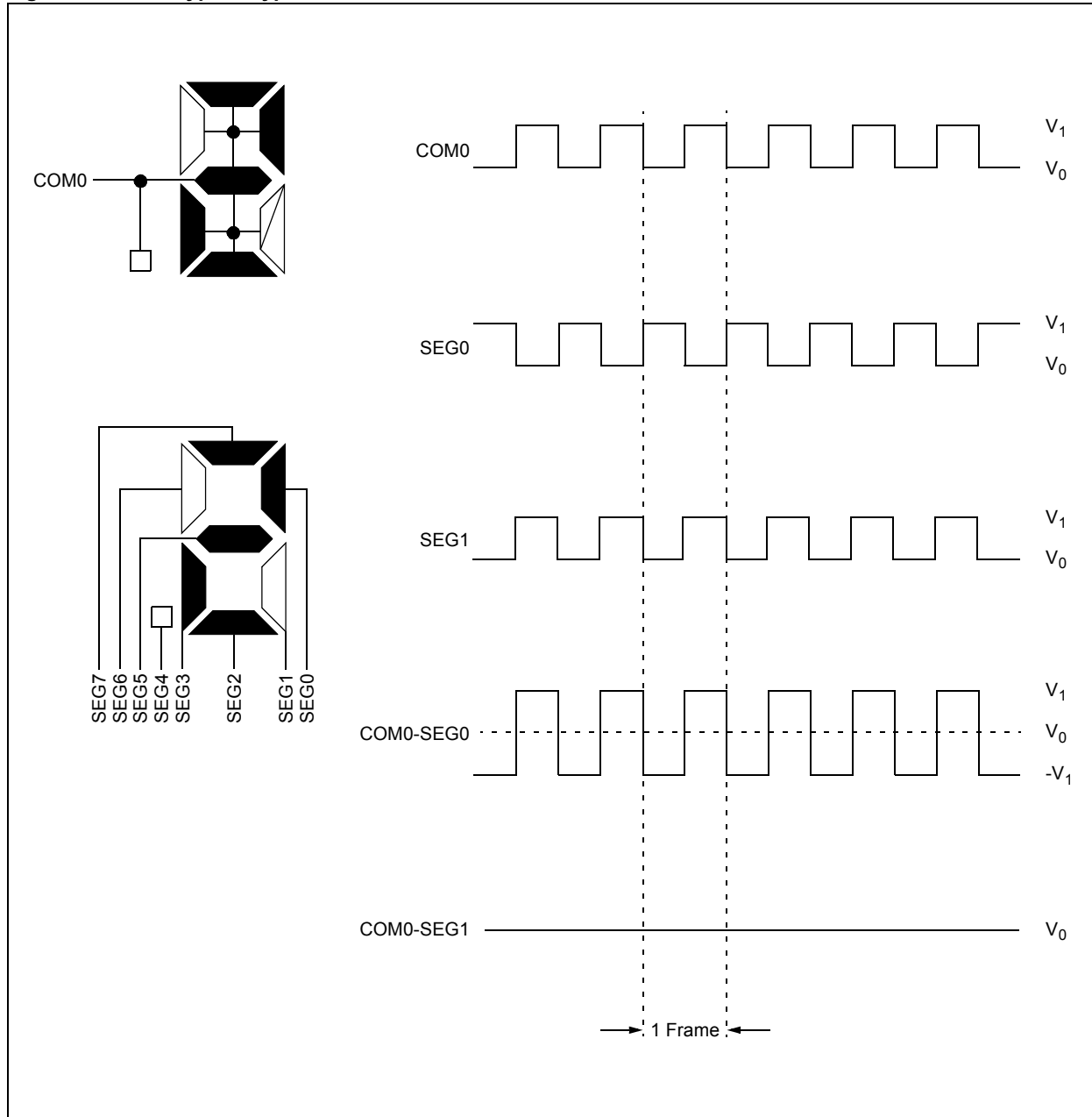
The LCDs can be driven by two types of waveforms: Type-A and Type-B. In a Type-A waveform, the phase changes within each common type, whereas a Type-B waveform's phase changes on each frame boundary. Thus, Type-A waveforms maintain 0 V<sub>DC</sub> over a single frame, whereas Type-B waveforms take two frames.

**Note:** If Sleep has to be executed with LCD Sleep enabled (SLPEN (LCDCON[6]) = 1), care must be taken to execute Sleep only when the V<sub>DC</sub> on all the pixels is '0'.

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Figure 10-1 through Figure 10-13 provide waveforms for Static, Half-Multiplex, One-Third Multiplex and Quarter Multiplex drives for Type-A and Type-B waveforms.

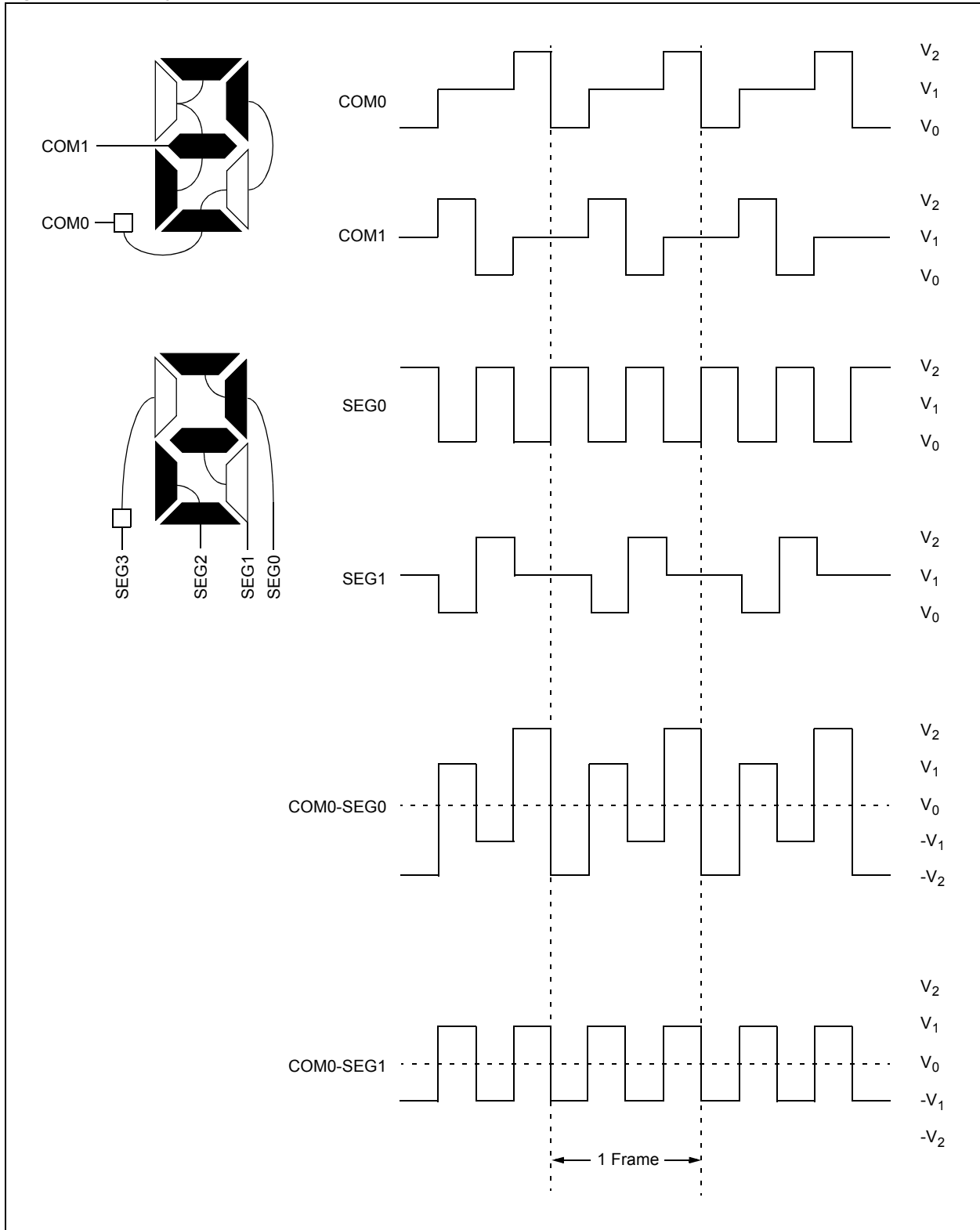
**Figure 10-1: Type-A/Type-B Waveforms in Static Drive**





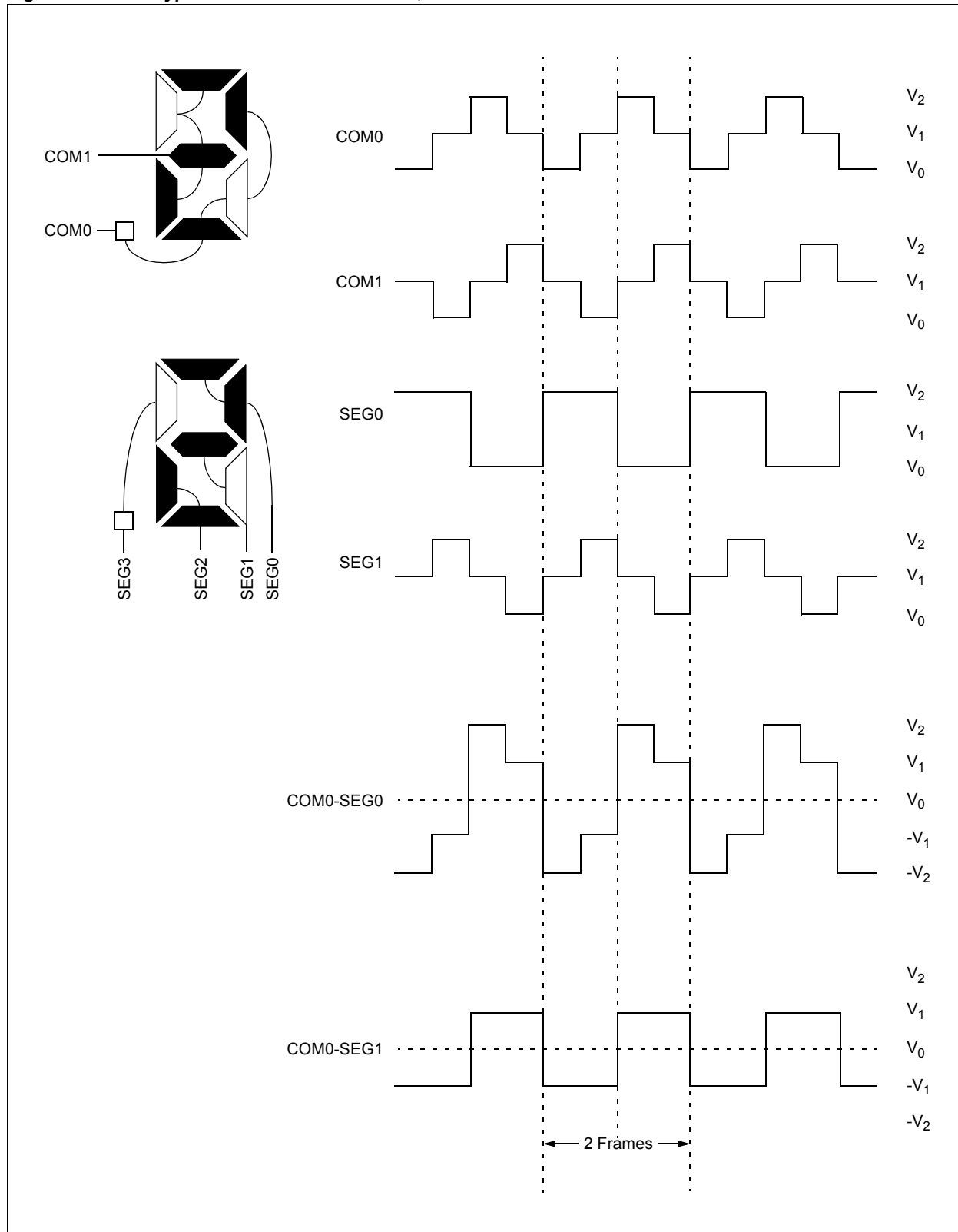
# Liquid Crystal Display (LCD)

Figure 10-2: Type-A Waveforms in 1/2 MUX, 1/2 Bias Drive



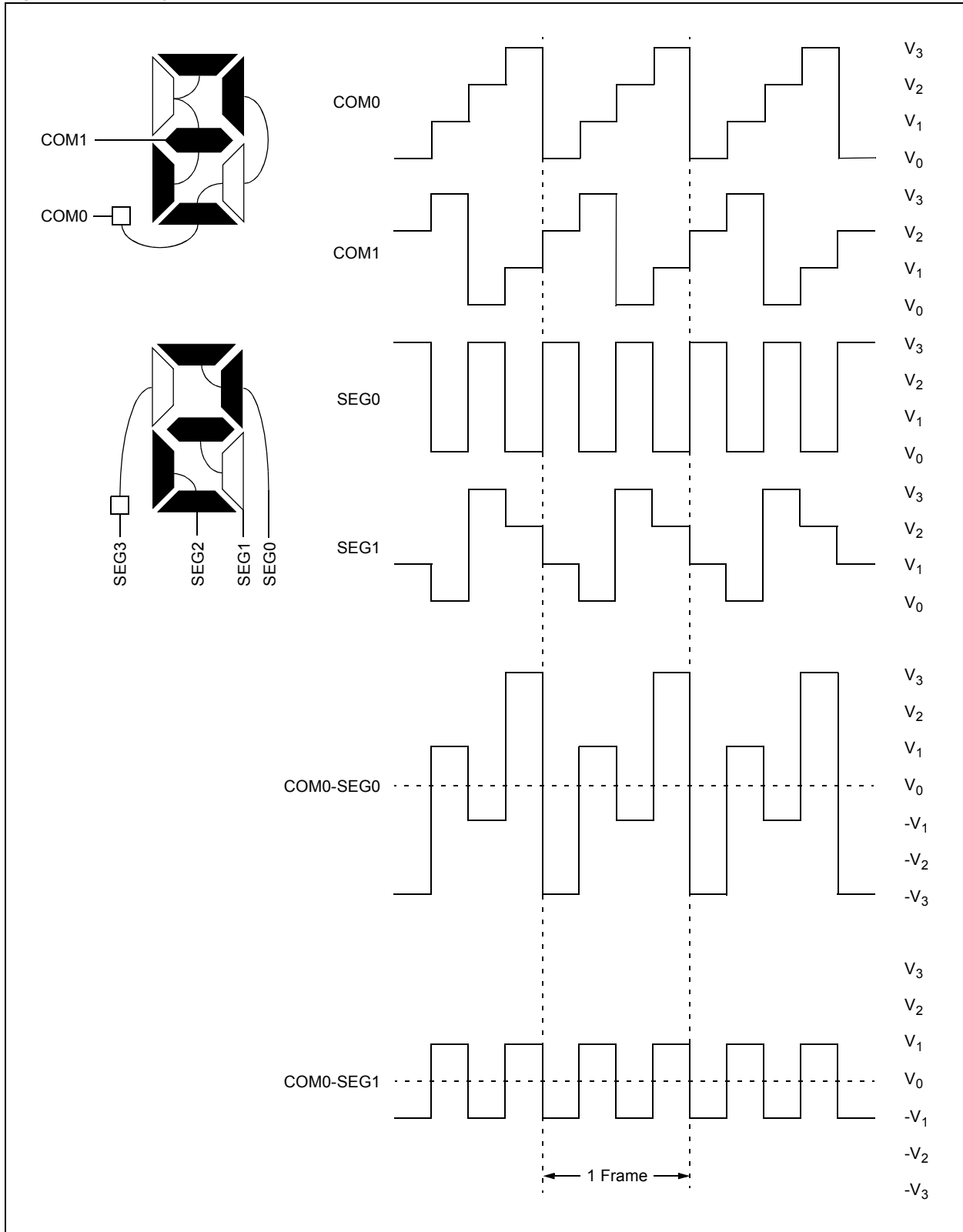
# dsPIC33/PIC24 Family Reference Manual

Figure 10-3: Type-B Waveforms in 1/2 MUX, 1/2 Bias Drive



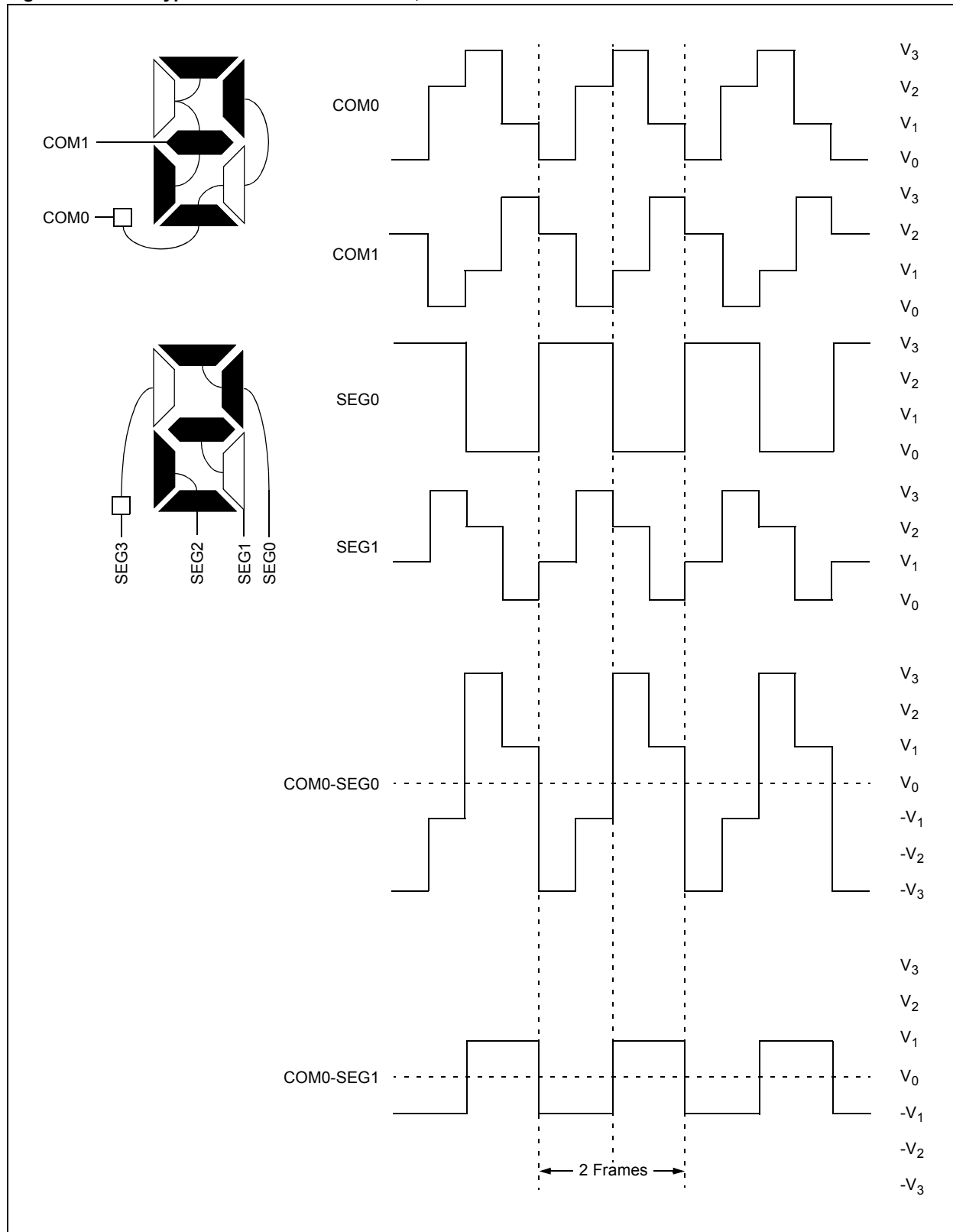
# Liquid Crystal Display (LCD)

**Figure 10-4: Type-A Waveforms in 1/2 MUX, 1/3 Bias Drive**



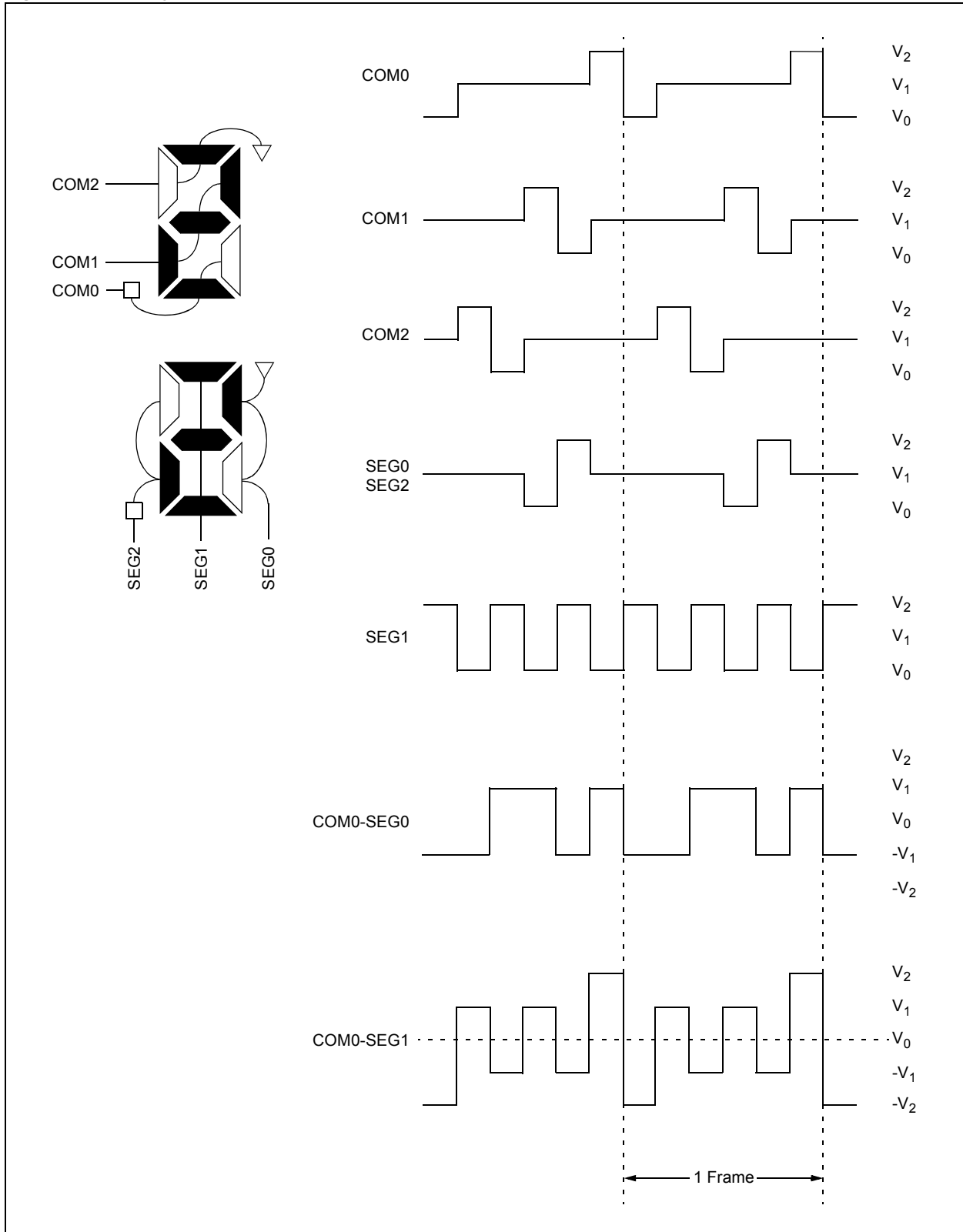
# dsPIC33/PIC24 Family Reference Manual

Figure 10-5: Type-B Waveforms in 1/2 MUX, 1/3 Bias Drive



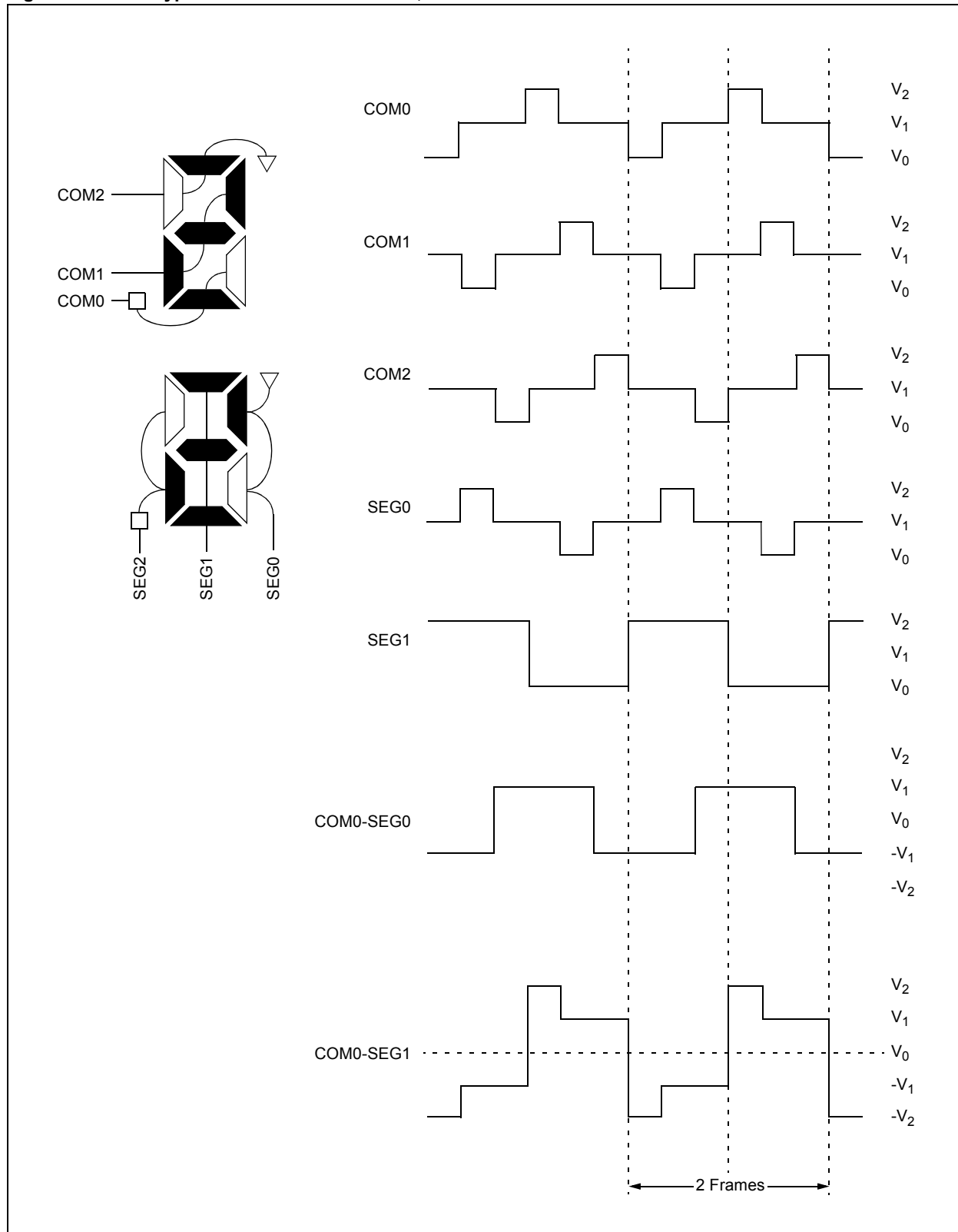
# Liquid Crystal Display (LCD)

**Figure 10-6: Type-A Waveforms in 1/3 MUX, 1/2 Bias Drive**



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Figure 10-7: Type-B Waveforms in 1/3 MUX, 1/2 Bias Drive



# Liquid Crystal Display (LCD)

**Figure 10-8: Type-A Waveforms in 1/3 MUX, 1/3 Bias Drive**

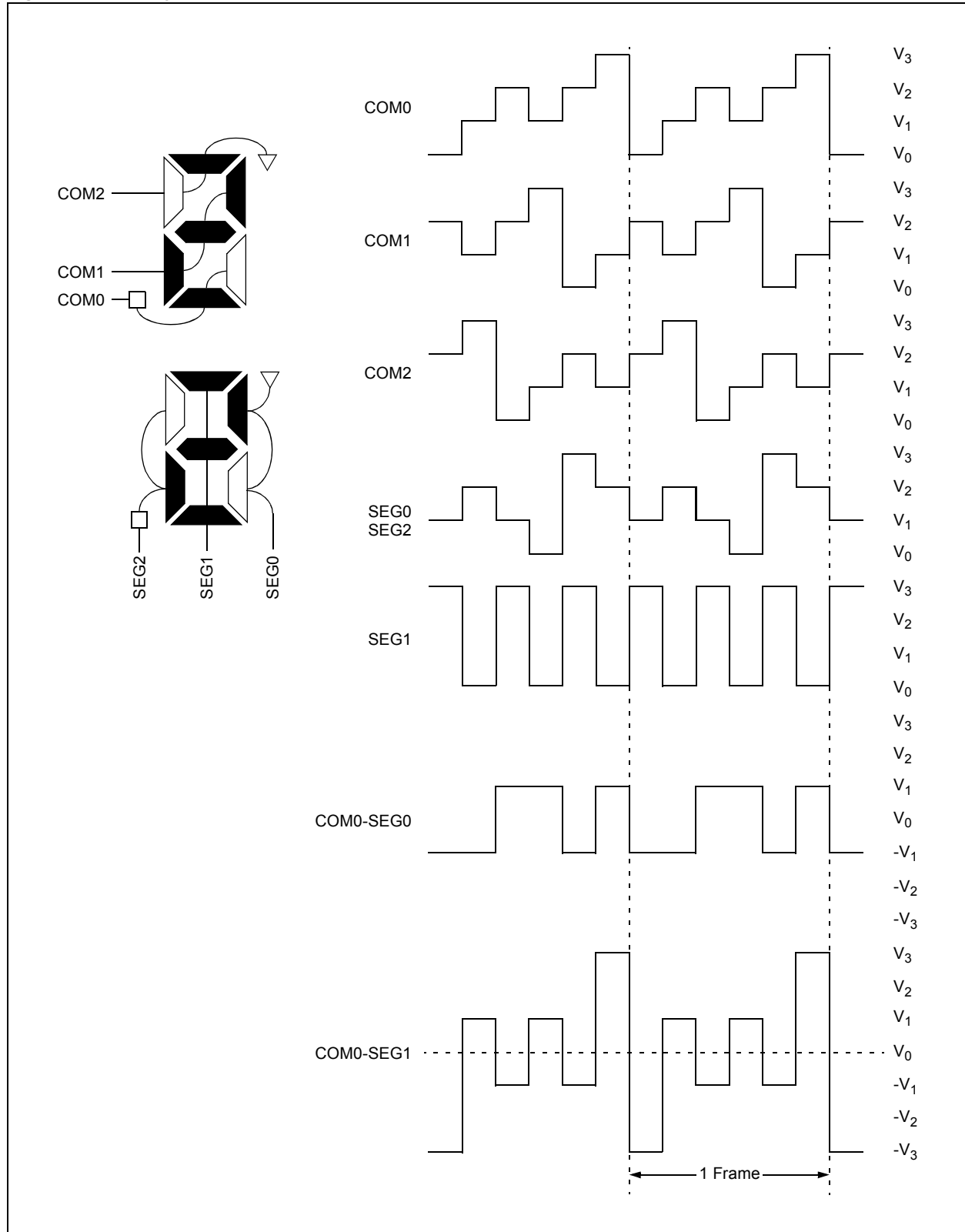
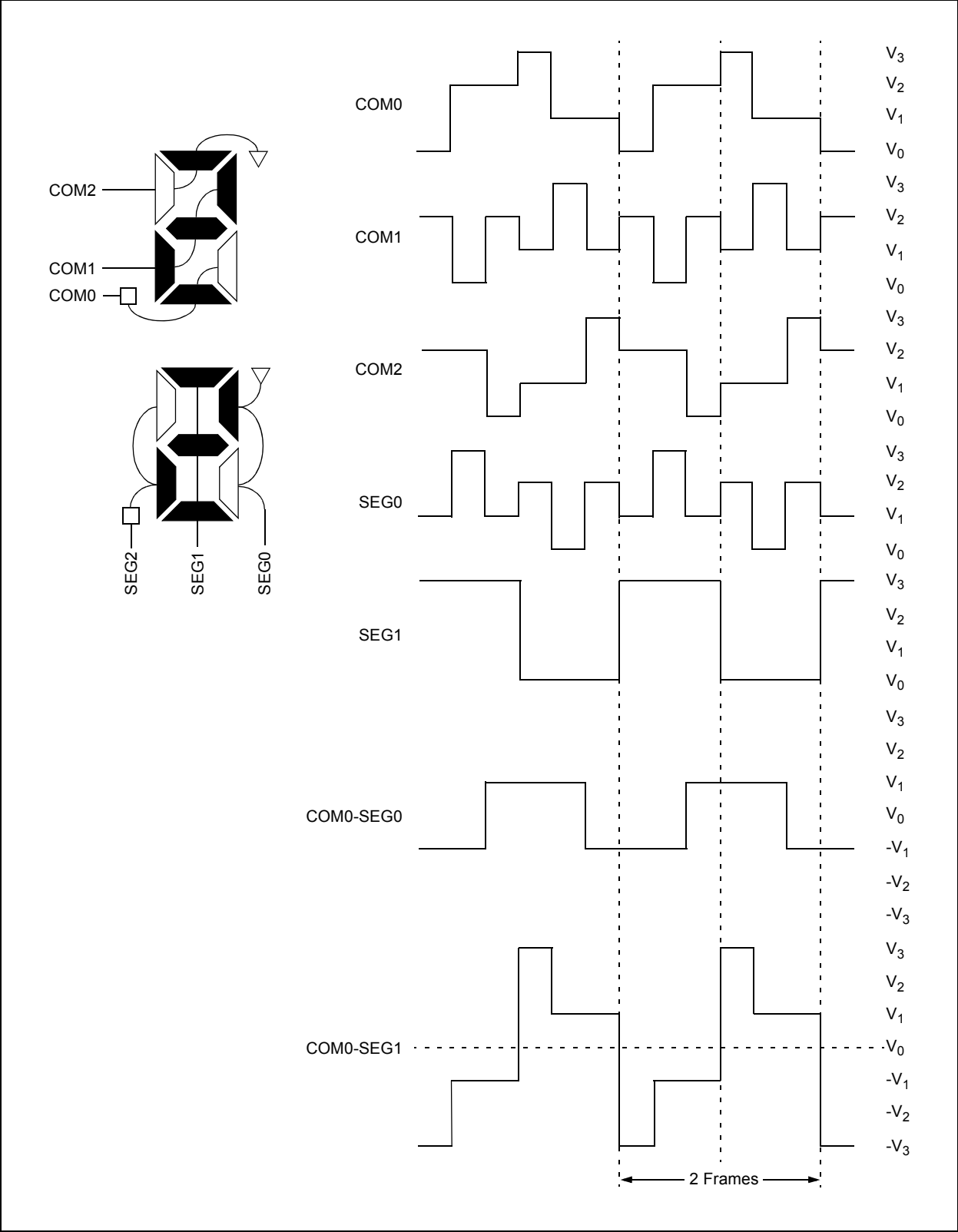


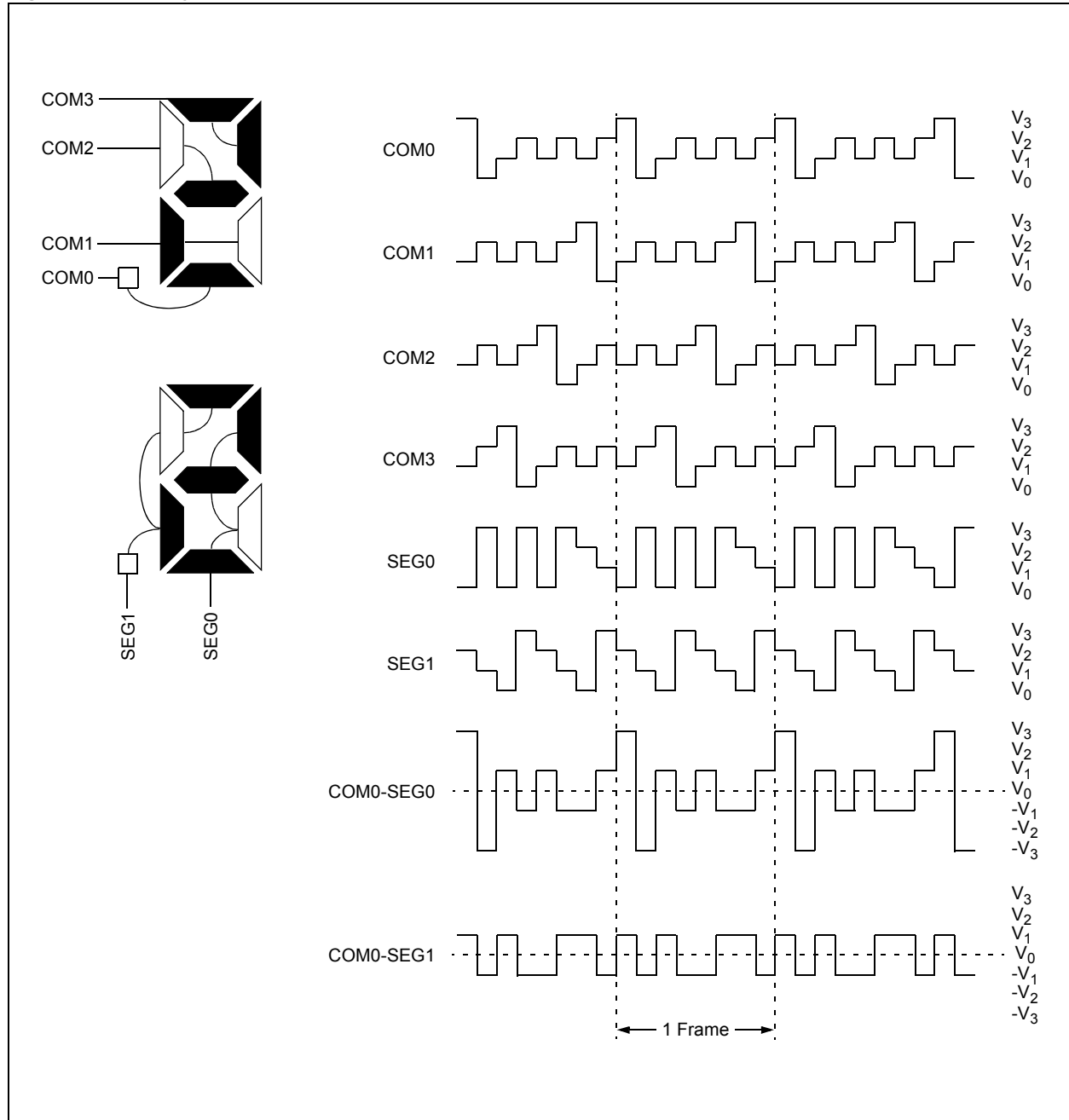
Figure 10-9: Type-B Waveforms in 1/3 MUX, 1/3 Bias Drive





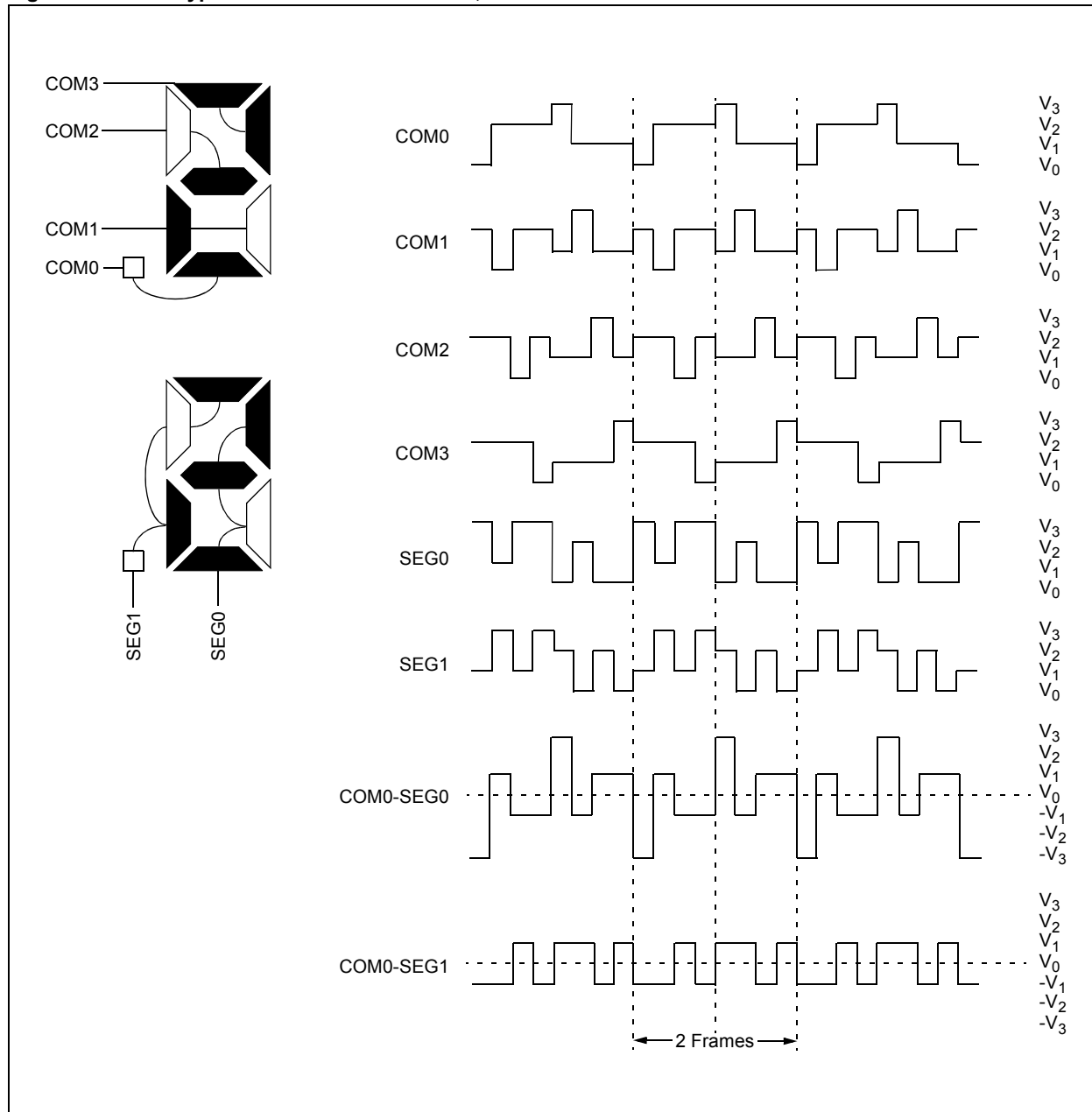
# Liquid Crystal Display (LCD)

Figure 10-10: Type-A Waveforms in 1/4 MUX, 1/3 Bias Drive



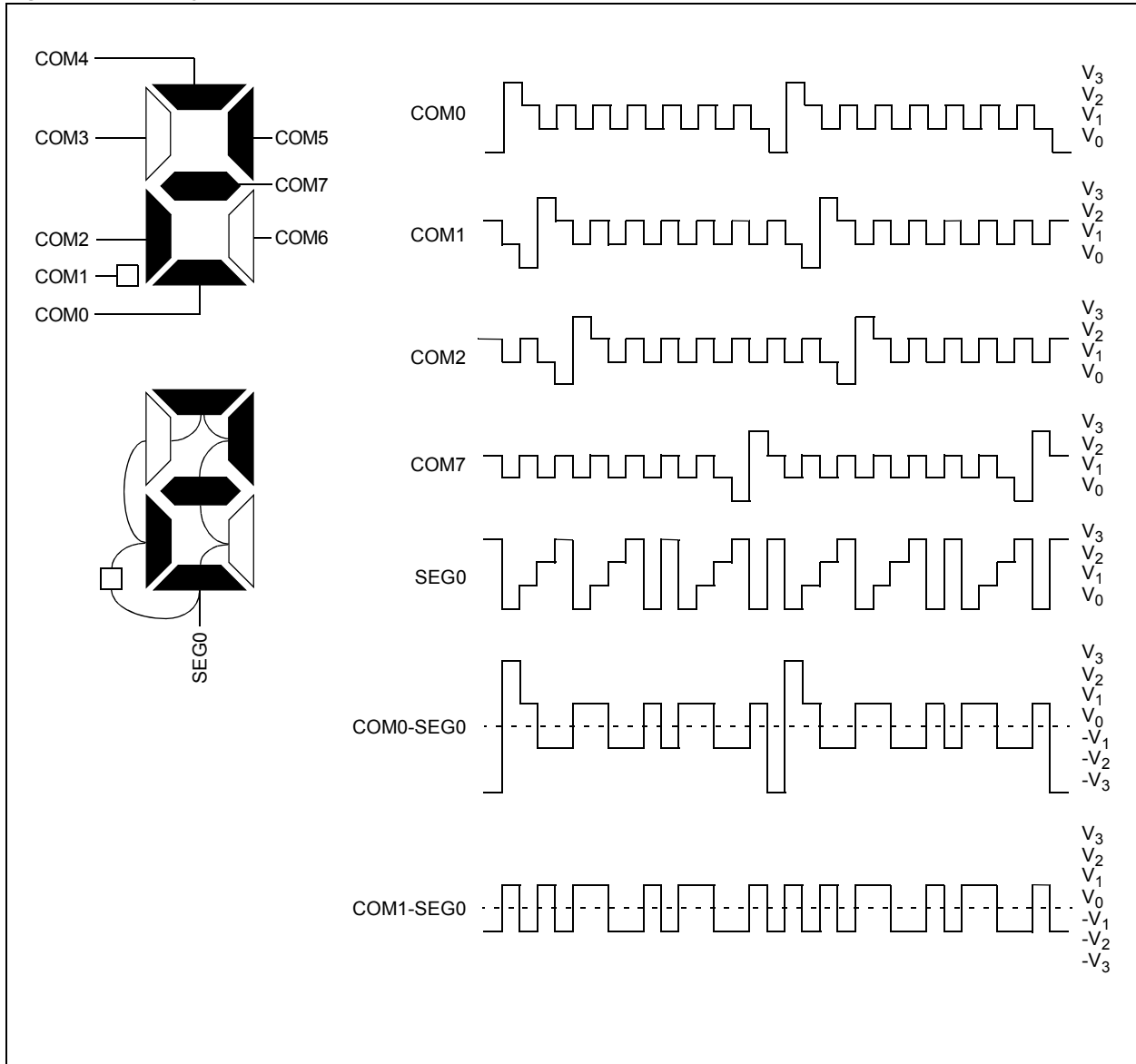
# dsPIC33/PIC24 Family Reference Manual

Figure 10-11: Type-B Waveforms in 1/4 MUX, 1/3 Bias Drive



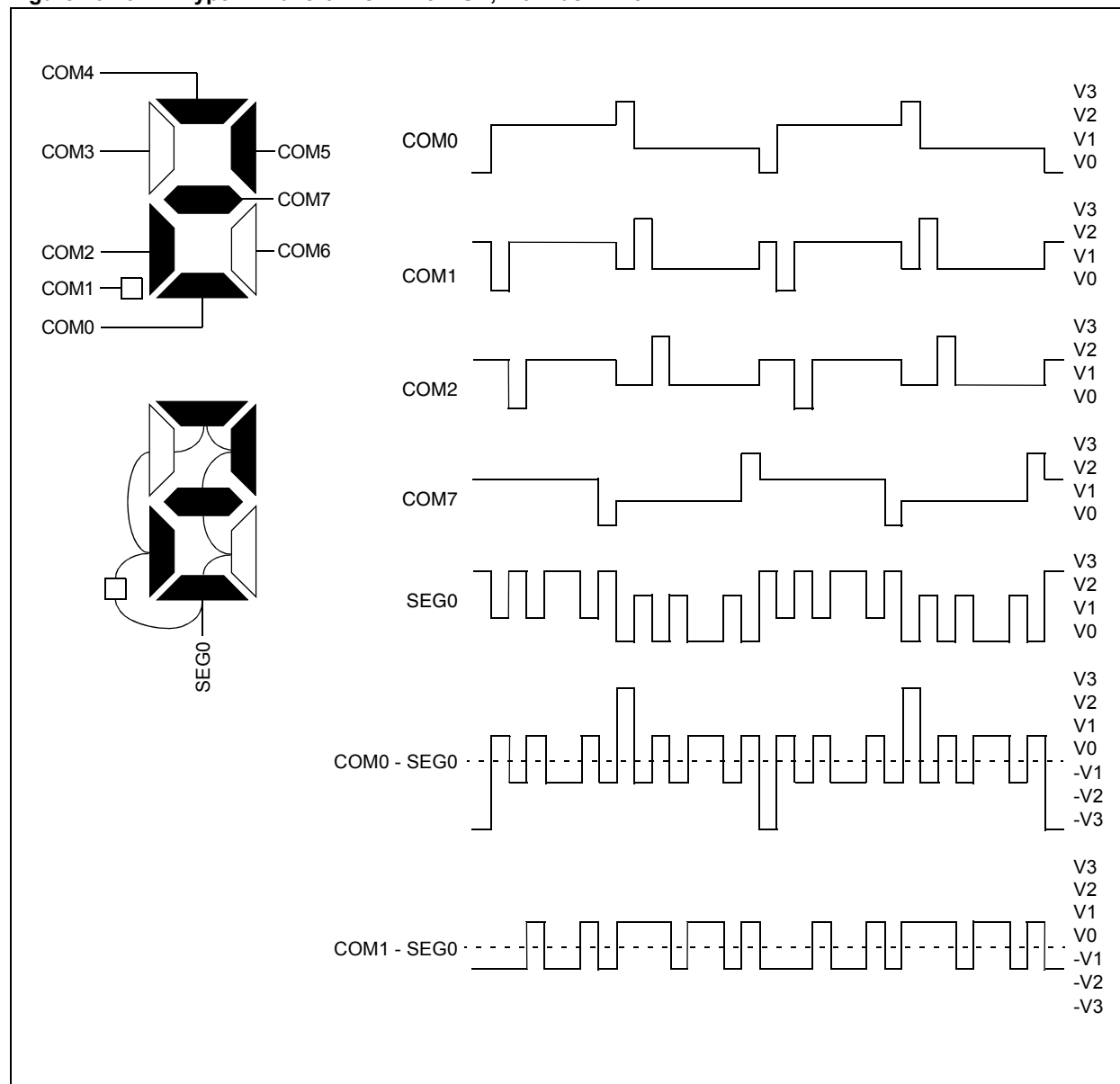
# Liquid Crystal Display (LCD)

Figure 10-12: Type-A Waveforms in 1/8 MUX, 1/3 Bias Drive



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**Figure 10-13: Type-B Waveforms in 1/8 MUX, 1/3 Bias Drive**



# Liquid Crystal Display (LCD)

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## 11.0 LCD INTERRUPTS

The LCD timing generation provides an interrupt that defines the LCD frame timing. This interrupt can be used to coordinate the writing of the pixel data with the start of a new frame, which produces a visually crisp transition of the image.

This interrupt can also be used to synchronize external events to the LCD. For example, the interface to an external segment driver can be synchronized for segment data updates to the LCD frame.

A new frame is defined as beginning at the leading edge of the COM0 common signal. The interrupt will be set immediately after the LCD controller completes accessing all pixel data required for a frame. This will occur at a fixed interval before the frame boundary (TFINT), as shown in [Figure 11-1](#).

The LCD controller will begin to access data for the next frame, within the interval from the interrupt to when the controller begins accessing data after the interrupt (TFWR). New data must be written within TFWR, as this is when the LCD controller will begin to access the data for the next frame.

When the LCD driver is running with Type-B waveforms and the LMUX[2:0] bits are not equal to '00', there are some additional issues.

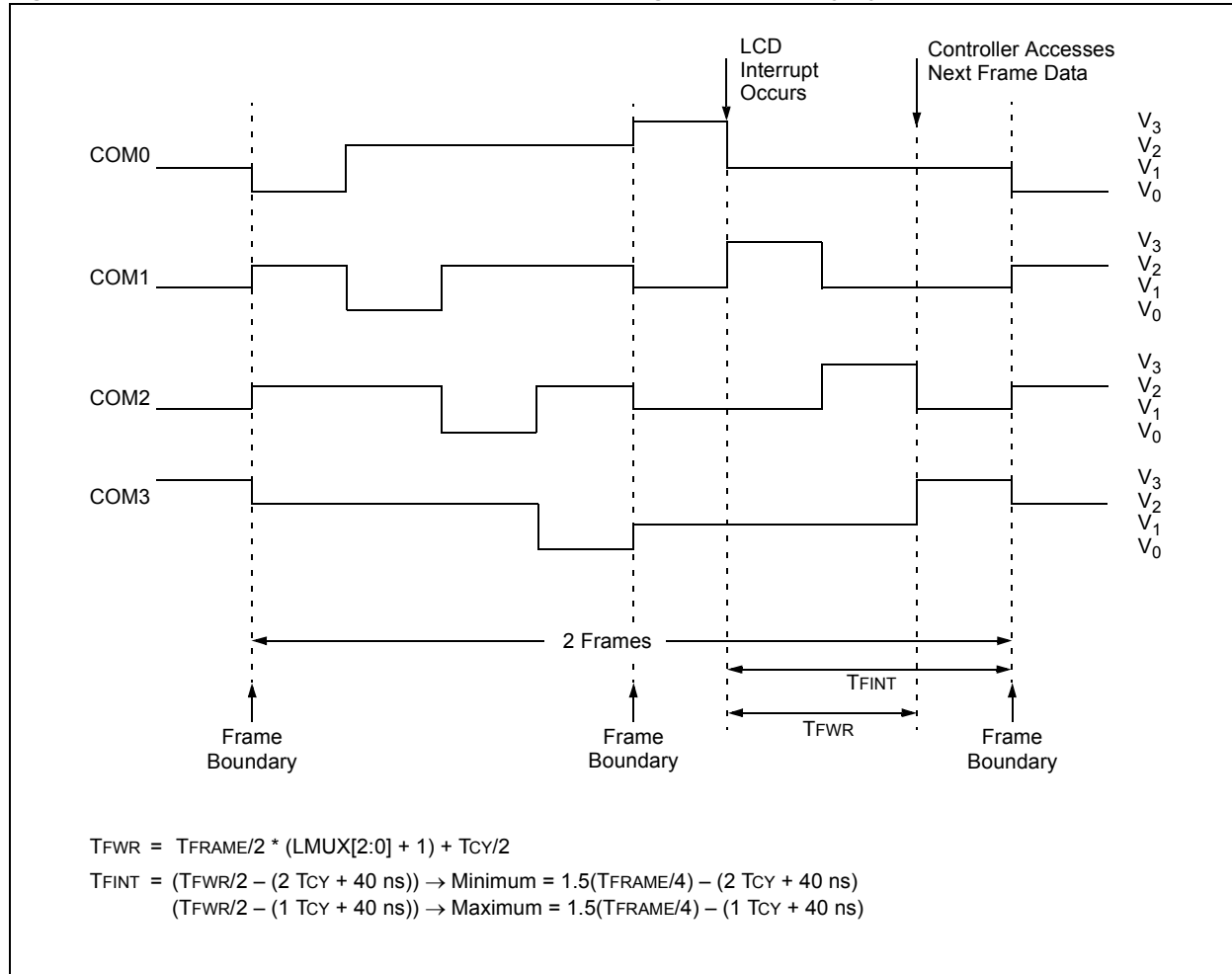
Since the DC voltage on the pixel takes two frames to maintain 0V, the pixel data must not change between subsequent frames. If the pixel data were allowed to change, the waveform for the odd frames would not necessarily be the complement of the waveform generated in the even frames, and a DC component would be introduced into the panel. Because of this, using Type-B waveforms requires synchronizing the LCD pixel updates to occur within a subframe after the frame interrupt.

To correctly sequence writing in Type-B, the interrupt only occurs on complete phase intervals. If the user attempts to write when the write is disabled, the WERR bit (LCDCON[5]) is set.

<b>Note:</b>	The interrupt is not generated when the Type-A waveform is selected and when the Type-B with no Multiplex (Static) is selected.
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**Figure 11-1: Example Waveforms and Interrupt Timing in Quarter Duty Cycle Drive**



## 12.0 CONFIGURING THE LCD MODULE

To configure the LCD module:

1. Select the frame clock prescale using bits, LP[3:0] ([LCDPS\[3:0\]](#)).
2. Configure the appropriate pins to function as segment drivers using the [LCDSEx](#) registers.
3. If using the internal reference resistors for Biasing, enable the internal reference ladder and:
  - Define the Mode A and Mode B interval by using the LRLAT[2:0] bits ([LCDREF\[2:0\]](#))
  - Define the low, medium or high ladder for Mode A and Mode B by using the LRLAP[1:0] bits ([LCDREF\[7:6\]](#)) and the LRLBP[1:0] bits ([LCDREF\[5:4\]](#)), respectively
  - Set the VLCDxPE bits ([LCDREF\[10:8\]](#)) and enable the LCDIRE bit ([LCDREF\[15\]](#))
4. Configure the following LCD module functions using the [LCDCON](#) register:
  - Multiplex and Bias mode – LMUX[2:0] bits
  - Timing Source – CS[1:0] bits
  - Sleep mode – SLPEN bit
5. Write the initial values to the [LCDDATAx: LCD Data x Registers](#): LCDDATA0 through LCDDATA31.
6. Clear the LCD Interrupt Flag, LCDIF, and if desired, enable the interrupt by setting bit, LCDIE.
7. Enable the LCD module by setting bit, LCDEN ([LCDCON\[15\]](#)).

## 13.0 OPERATION DURING SLEEP

The LCD module can operate during Sleep. The selection is controlled by the SLPEN bit (LCDCON[6]). Setting the SLPEN bit allows the LCD module to go to Sleep. Clearing the SLPEN bit allows the module to continue to operate during Sleep.

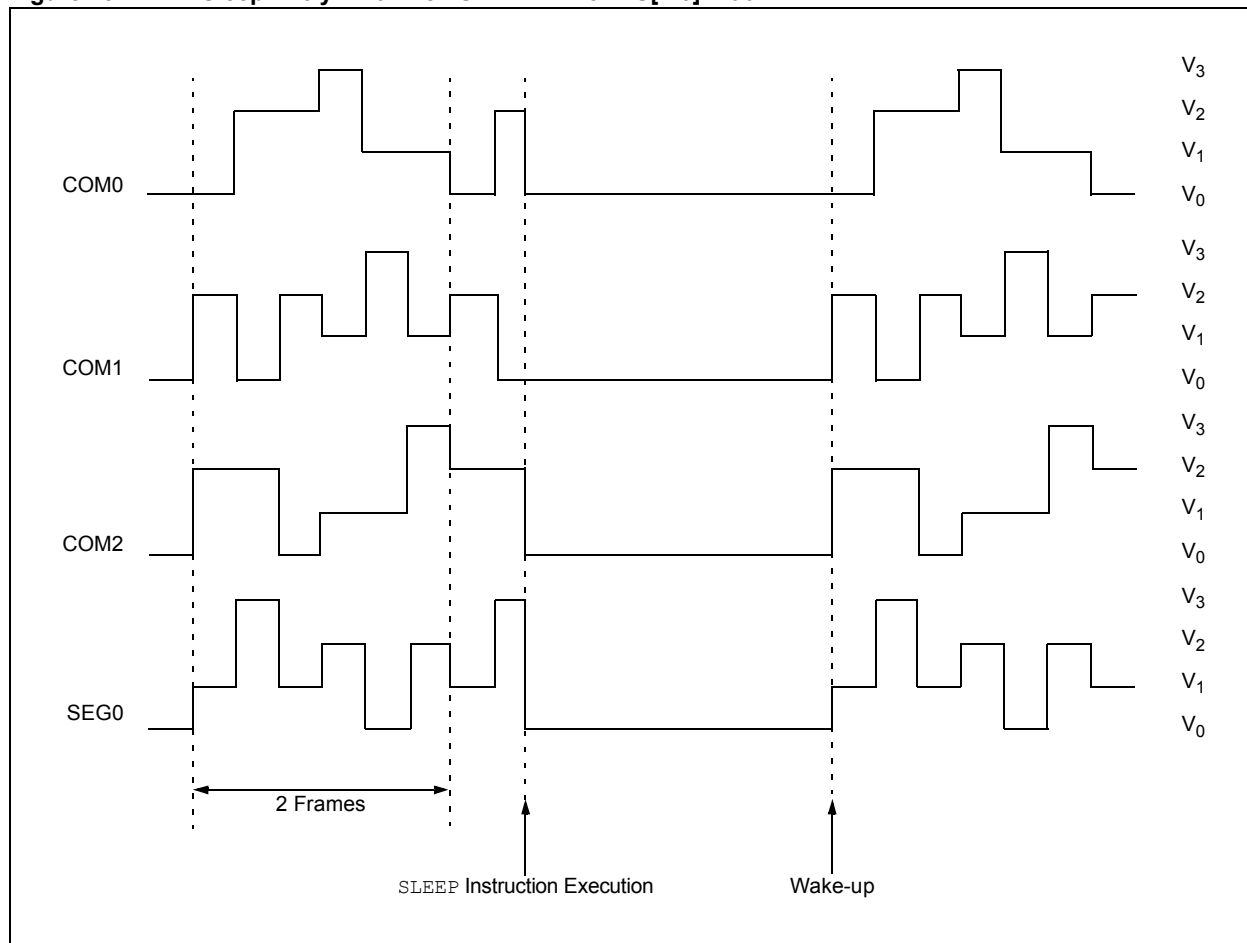
If a `SLEEP` instruction is executed and `SLPEN = 1`, the LCD module will cease all functions and go into a very Low-Current Consumption mode. The module will stop operation immediately and drive the minimum LCD voltage on both segment and common lines. Figure 13-1 shows this operation.

The LCD module current consumption will not decrease in this mode, but the overall consumption of the device will be lower due to the shutdown of the core and other peripheral functions.

To ensure that no DC component is introduced on the panel, the `SLEEP` instruction should be executed immediately after an LCD frame boundary. The LCD interrupt can be used to determine the frame boundary. See Section 11.0 “LCD Interrupts” for the formulas to calculate the delay.

If a `SLEEP` instruction is executed and `SLPEN = 0`, the module will continue to display the current contents of the LCDDATAx registers. The LCD data cannot be changed.

Figure 13-1: Sleep Entry/Exit when `SLPEN = 1` or `CS[1:0] = 00`





# Liquid Crystal Display (LCD)

## 14.0 ENHANCED LCD MODE

In the Enhanced LCD mode of operation, there are many new features that are available to do core-independent activity, such as Blinking, animation, etc. This mode can also be disabled so as to be backward compatible with the legacy LCD module if `ELCDEN (LCDCTRL[0]) = 0`.

The new features of the Enhanced LCD mode are:

- Dual Display Memory
- Blinking the Pixel
- Blanking the Pixel
- Dedicated Timer for Time Generation for Automated Switching of Blinking/Blanking
- Status Register to Indicate the Behavior of the Enhanced Mode Operation

### 14.1 Dual Display Memory

There is dual display memory for data, primary data memory and the secondary data memory (LCDDATAx and LCDSDATAx). There are various modes of operation based on the `DMSEL[1:0]` bits selection ([Table 14-1](#)).

**Table 14-1: DMSEL Modes of Operation**

Operation Mode	DMSEL[1:0] Selection	Description
Primary Memory Only Mode	DMSEL[1:0] = 00	Selects Primary Memory as Display Memory
Secondary Memory Only Mode	DMSEL[1:0] = 01	Selects Secondary Memory as Display Memory
One-Time Switch Between Primary and Secondary Memory	DMSEL[1:0] = 10	Switch One Time Between Primary and Secondary Memories Based on SMFCS[2:0] Bits
Continue Operation with Primary and Secondary Memory	DMSEL[1:0] = 11	Continue Alternating Selection Between Primary and Secondary Memories Based on SMFCS[2:0] Bits

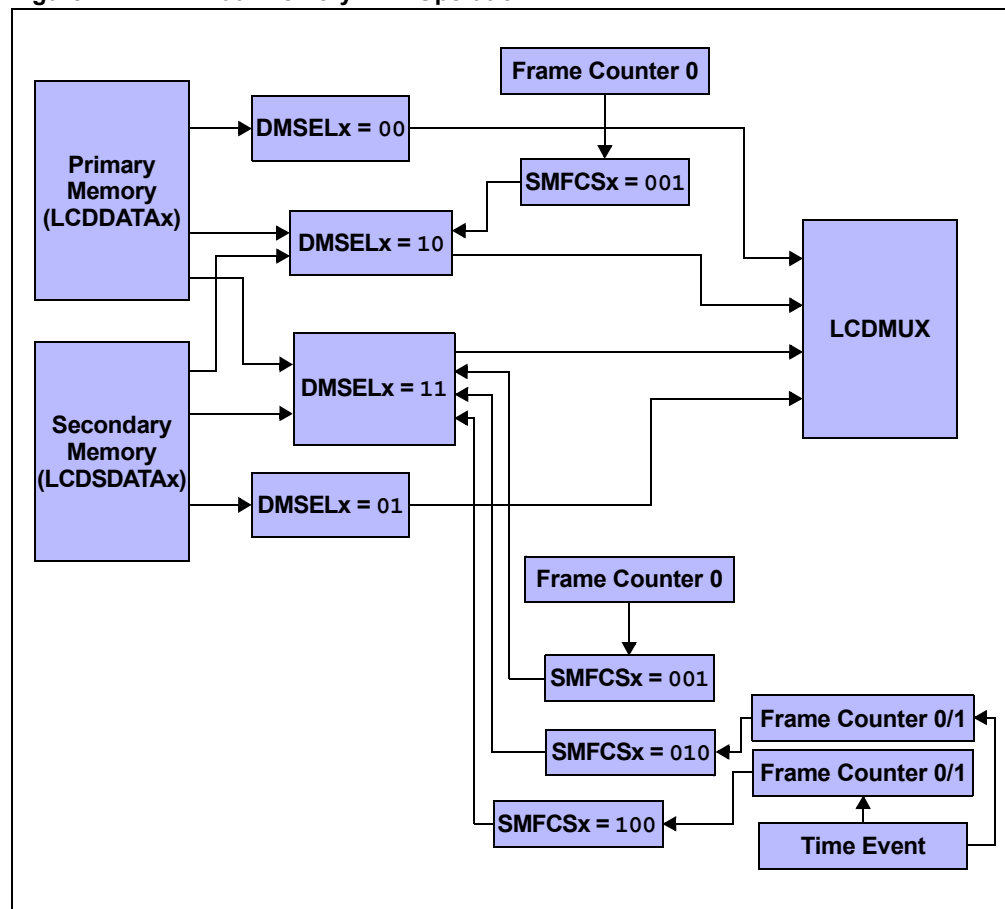
The secondary memory is a register-based memory used to store secondary pixel data or to select the pixel to Blink/Blank. The memory selection is accomplished by the Data Memory Selection bits, `DMSEL[1:0]`.

When secondary memory is assigned to display data, a time-based event is available to select the memory between primary and secondary. When secondary memory is assigned to select Blink pixels, a time-based event is available to select the Blink frequency. The time-based event is defined by the user and has many options based on the register bits. These operations can be executed without the core invention.

It is the user's responsibility to perform the following:

- Set the LOCK bit to avoid accidental writes
- Check the memory active states before writing data into memory
- If the secondary memory is selected for pixel selection, set the lock bit for secondary memory

Figure 14-1: Dual Memory LCD Operation



# Liquid Crystal Display (LCD)

## EXAMPLE 14-1: DUAL MEMORY OPERATION WITH SMFCS = 1 (CONTINUOUSLY ALTERNATE WITH SECOND AND PRIMARY MEMORY WITH FC0 FRAME COUNTER)

```
LCDSE0bits.SE00=1;
LCDSE0bits.SE01=1;
LCDSE0bits.SE02=1;
LCDSE0bits.SE03=1;
LCDSE0bits.SE04=1;
LCDSE0bits.SE05=1;
LCDSE0bits.SE08=1;

IFS6bits.LCDIF=0;
LCDPS=0x02;
LCDREF=0x80FF;
LCDCON=0x800F;
LCDCTRLbits.FCCS=0;           // LCD clock source

LCDASTATbits.DMSEL=3;         // alternate between the memory
LCDASTATbits.SMEMEN=1;
LCDASTATbits.PMEMDIS=0;
LCDCTRLbits.BLINKMODE=0;      // selected pixels

/////primary memory data write //////////////////////////////////
LCDDATA0bits.S00C0=0;
LCDDATA4bits.S00C1=0;
LCDDATA8bits.S00C2=0;
LCDDATA12bits.S00C3=0;

LCDDATA0bits.S01C0=1;
LCDDATA4bits.S01C1=0;
LCDDATA8bits.S01C2=1;
LCDDATA12bits.S01C3=0;

//////////secondary memory data write //////////////////////
LCSDATA16bits.S00C4=1;
LCSDATA20bits.S00C5=1;
LCSDATA24bits.S00C6=1;
LCSDATA28bits.S00C7=1;

LCSDATA16bits.S01C4=1;
LCSDATA20bits.S01C5=1;
LCSDATA24bits.S01C6=1;
LCDCTRLbits.SMFCs=1;
LCDFC0=0xFF;
LCDCTRLbits.ELCDEN=1;
```

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## 14.2 Blink Mode

In Blink mode, pixels will alternate between the ON and OFF state at the frequency given by the selected frame counter. There are two modes to operate in Blink mode:

- Blink the selected pixels (BLINKMODE[1:0] = 01); see [Example 14-2](#)
- Blink all the pixels (BLINKMODE[1:0] = 10); see [Example 14-3](#)

When BLINKMODE[1:0] bits = 01 is selected, the secondary memory is used to select the pixels that need to be Blinked (i.e., only the pixels selected in the secondary memory will Blink).

### EXAMPLE 14-2: BLINK WITH SELECTED PIXELS FROM SECONDARY MEMORY (BLINKFCS[2:0] = 1, LCDFC1 = 100)

```
LCDSE0bits.SE00=1;
LCDSE0bits.SE01=1

LCDDATA12bits.S01C3=1;
LCDDATA12bits.S01C3=1;    //Pixel that will be blinked
LCDDATA16bits.S01C4=1;
LCDDATA28bits.S01C7=1;    //Pixel that will be blinked

IFS6bits.LCDATIF=0;
LCDACTRLbits.FCCS=00;    // LCD clock source

LCDASTATbits.SMEMEN=1;
LCDACTRLbits.BLINKMODE=1; // Blink the selected pixels in the secondary memory

LCDSDATA28bits.S01C7=1;   //blink content on secondary display
LCDSDATA12bits.S01C3=1;   //blink content on secondary display

LCDACTRLbits.BLINKFCS=1;  // Blink with FC1
LCDFC1=100;

LCDACTRLbits.ELCDEN=1;
```

### EXAMPLE 14-3: BLINK ALL PIXELS (FC0 = 0x3F, FC1 = 0xC0 WITH LCDTEVNT = 0xFF)

```
LCDSE0bits.SE00=1;
LCDSE0bits.SE01=1

LCDDATA12bits.S01C3=1;    //enable pixels to blink
LCDDATA12bits.S01C3=1;    //enable pixels to blink
LCDDATA16bits.S01C4=1;    //enable pixels to blink
LCDDATA28bits.S01C7=1;    //enable pixels to blink

IFS6bits.LCDATIF=0;
LCDACTRLbits.FCCS=00;    // LCD clock source
LCDACTRLbits.BLINKMODE=2; //Blink all pixels

LCDACTRLbits.BLINKFCS=4;  // Blink alternate between
LCDFC0=0x3F;              // Blink rate with FC0
LCDFC1=0xC0;              // Blink rate with FC1
LCDTEVNT =0xFF;           //TEVENT for the FC0,FC1

LCDACTRLbits.ELCDEN=1;
```

## 14.3 Blank Mode

In Blank mode, pixels will alternate between the ON and OFF state at the frequency given by the selected frame counter. The Blank mode overrides any display configuration to drive the pixels into an OFF state, including the Blink mode settings.

- Blank the selected pixels (BLANKMODE[1:0] = 01)
- Blank all the pixels (BLANKMODE[1:0] = 10)

When BLANKMODE[1:0] bits = 01 is chosen, the secondary memory is used as the selected option (i.e., only the pixels selected in the secondary memory will Blank).

**Table 14-2: Blink and Blank with Secondary Memory**

Blink/Blank	Primary Memory	Secondary Memory	Blink/Blank	Pixel On	Comments
10	1	x	Yes	Yes	Blink/Blank with all pixels
10	0	x	No	No	Nothing on
01	1	1	Yes	Yes	Blink/Blank with selected pixels <sup>(1)</sup>
01	1	0	No	Yes	Blink/Blank with selected pixels <sup>(1)</sup>
01	0	1	No	No	Nothing on
01	0	0	No	No	Nothing on

**Note 1:** The pixels are selected using secondary memory.

## 14.4 Autonomous Blink/Blank Segments without Core Intervention for Animation

The LCD module is configurable and has function selection bits to select the following options:

- Blink frequency selection based on time-based event
- Blink frequency toggle selection based on time-based event
- Blank operation selection based on time-based event
- Pixel will alternate between ON and OFF state at the frequency given by the selected frame counter

### 14.4.1 CONTROL OF THE AUTOMATIC DISPLAY FEATURES

The LCD module generates internal signals, triggers and interrupt events based on a 16-bit count value. There are three frame counters to support core-independent operations.

#### 14.4.1.1 Frame Counters

The frame counter is used to create a time-based event for several automatic features (e.g., Blinking, Blanking, Automated Display modes). The LCD module has three independent frame counters (FC0, FC1 and FC2). The counters can be associated with any functions by user configurations.

- Frame counter gets enabled based on Blink/Blank/memory switchover request on the selected frame counter.
- Frame counter values are not allowed to be written when LCD is active. The frame counter is synchronized to the LCD frame start and generates an internal event each time the counter overflows. The FCx register can only be written when Frame Counter x is disabled.
- The frame counter overflow is used as a timer-based event by Core Independent Operations (CIP) based on user configuration.
- This module supports selection of different time-based events for several functions, without core intervention, based on user configuration.
- The FCx value should be a multiple of the frame frequency.

#### 14.4.1.2 LCD Automation Timer Interrupt

The LCD automation timer interrupt can be asserted on a Frame Counter (FCx) event, time event or by the SBLANK (LCDSTAT[14]) flag bit.

Enhancement LCD Interrupt Flag (LCDATIF) = (FCx Event + Time Event + SBLANK).

All combined asserts the interrupt and the user can check the status bits in order to find the reason for the interrupt.

14.4.2 TIMER EVENT SELECTION REGISTER

Timer event selection is used to select the frame counter without core invention. The frame counters switch over the based frame counter selection in the LCD Automatic Control register when the timer event overflows.

Figure 14-2: Blink Mode with BLINKMODE[1:0] = 10, FC0 = 2, FC1 = 4, TEVENT[15:0] = 8 and BLINKFCS[2:0] = 100

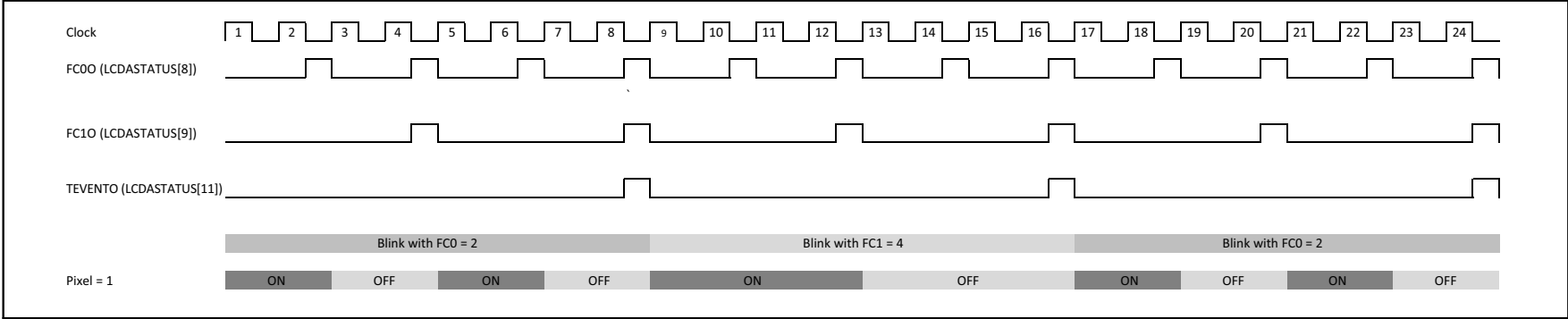
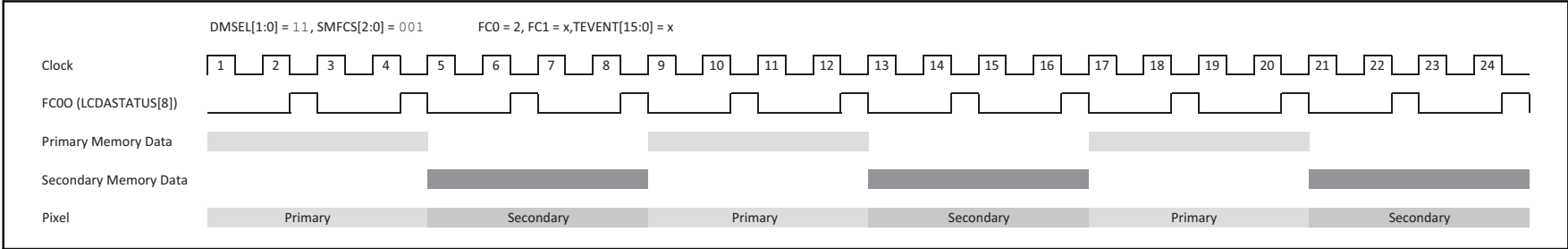


Figure 14-3: Dual Memory Mode with DMSEL[1:0] = 11, SMFCS[2:0] = 001, FC0 = 2, FC1 = x, TEVENT[15:0] = x



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**Register 14-1: LCDACTRL: LCD Automatic Control Register**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SMFCS[2:0] <sup>(1,2,3,4,5)</sup>			BLINKFCS[2:0] <sup>(4,5,6,7)</sup>			BLINKMODE[1:0] <sup>(8,9)</sup>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BLANKFCS[2:0](3,5,6,7,10,11)			BLANKMODE[1:0]		FCCS[1:0]		ELCDEN
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-13      **SMFCS[2:0]:** Frame Counter Selection for Data Memory Selection bits<sup>(1,2,3,4,5)</sup>

When DMSEL[1:0] = 10 (one-time switchover from current display memory to another memory):

000 = Reserved  
001 = Selects Frame Counter 0 (FC0)

When DMSEL[1:0] = 11 (continues to switch over from one memory to another memory):

000 = Reserved  
001 = Selects Frame Counter 0 (FC0)  
010 = Selects Frame Counter 0 (FC0), then continues with Frame Counter 1 (FC1) at the frequency given by the time event  
011 = Reserved

When DMSEL[1:0] = 11 (continues to switch over from one memory to another with a repeated pattern):

100 = Alternates between FC0 and FC1 at the frequency given by the time event  
101 = Reserved  
110 = Reserved  
111 = Reserved

- Note 1:** Secondary memory is selected for pixel enable to Blink or Blank when BLINKMODE[1:0] = 01 | BLANKMODE[1:0] = 01.
- 2: Secondary memory is used to store data to display or select the pixel to Blink or Blank.
  - 3: The FC1 is used when Blink mode is not selected (i.e., BLINKMODE[1:0] = 00 | 11).
  - 4: The FC2 is used when Blank mode is not selected (i.e., BLANKMODE[1:0] = 00 | 11).
  - 5: Frame counter selection switchover based on time event.
  - 6: Pixel will alternate between ON and OFF state at the frequency given by the selected frame counter.
  - 7: The FC0 is used when secondary memory is not selected with switchover function (i.e., DMSEL[1:0] = 00 or 01).
  - 8: Blink mode ON state is effective to the pixel when Blank mode is off.
  - 9: Blink mode OFF state drives '0' to the pixel.
  - 10: One-time Blank continues to Blank until a user changes the Blank mode to enable or disable the enhanced LCD feature (clears ELCDEN) or SBLANK is clear.
  - 11: In One-Time Blank Configuration mode, the pixel continues to Blink (to alternate between on and off) until the timer event happens.



# Liquid Crystal Display (LCD)

## Register 14-1: LCDACTRL: LCD Automatic Control Register (Continued)

bit 12-10	<b>BLINKFCS[2:0]:</b> Frame Counter Selection for Blink Selection bits (BLINKMODE = 01 or 10) <sup>(4,5,6,7)</sup> 000 = Reserved 001 = Selects Frame Counter 1 (FC1) 010 = Selects Frame Counter 0 (FC0), then continues with Frame Counter 1 (FC1) at the frequency given by the time event 011 = Reserved 100 = Alternates between FC0 and FC1 at the frequency given by the time event (repeated pattern) 101 = Reserved 110 = Reserved 111 = Reserved
bit 9-8	<b>BLINKMODE[1:0]:</b> Blink Mode bits <sup>(8,9)</sup> 00 = Blink mode is disabled 01 = Blink mode is enabled with selected pixels (when DMSEL[1:0] = 00) 10 = Blink mode is enabled with all pixels 11 = Reserved
bit 7-5	<b>BLANKFCS[2:0]:</b> Blank Operation Selection from Frame Counter Selection bits <sup>(3,5,6,7,10,11)</sup> (when BLANKMODE[1:0] = 01 or 10) 000 = Reserved 001 = Selects Frame Counter 2 (FC2) 010 = Selects Frame Counter 0 (FC0), then continues with Frame Counter 1 (FC1) at the frequency given by the time event 011 = Reserved 100 = Alternates between FC0 and FC1 at the frequency given by the time event (repeated pattern) 101 = Reserved 110 = One-time Blank selects Frame Counter 2 (FC2) by the time event <sup>(10,11)</sup> 111 = Reserved
bit 4-3	<b>BLANKMODE[1:0]:</b> Blank Mode bits 00 = Blank mode is disabled 01 = Blank mode is enabled with selected pixels (when DMSEL[1:0] = 00) 10 = Blank mode is enabled with all pixels 11 = Reserved
bit 2-1	<b>FCCS[1:0]:</b> Clock Source bits 00 = LCD clock 01 = RTCC 10 = CLC1 11 = CLC2
bit 0	<b>ELCDEN:</b> Enhancement LCD Enable bit 1 = Enhancement function is enabled 0 = Enhancement function is disabled

- Note 1:** Secondary memory is selected for pixel enable to Blink or Blank when BLINKMODE[1:0] = 01 | BLANKMODE[1:0] = 01.
- 2:** Secondary memory is used to store data to display or select the pixel to Blink or Blank.
- 3:** The FC1 is used when Blink mode is not selected (i.e., BLINKMODE[1:0] = 00 | 11).
- 4:** The FC2 is used when Blank mode is not selected (i.e., BLANKMODE[1:0] = 00 | 11).
- 5:** Frame counter selection switchover based on time event.
- 6:** Pixel will alternate between ON and OFF state at the frequency given by the selected frame counter.
- 7:** The FC0 is used when secondary memory is not selected with switchover function (i.e., DMSEL[1:0] = 00 or 01).
- 8:** Blink mode ON state is effective to the pixel when Blank mode is off.
- 9:** Blink mode OFF state drives '0' to the pixel.
- 10:** One-time Blank continues to Blank until a user changes the Blank mode to enable or disable the enhanced LCD feature (clears ELCDEN) or SBLANK is clear.
- 11:** In One-Time Blank Configuration mode, the pixel continues to Blink (to alternate between on and off) until the timer event happens.

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**Register 14-2: LCDASTAT: LCD Automatic Status Register**

U-0	R/C-0	R-0	R-0	R/C-0	R/C-0	R/C-0	R/C-0
—	SBLANK <sup>(1,2,3,4)</sup>	SMEMACT	PMEMACT	TEVENTO	FC2O	FC1O	FC0O
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SMLOCK <sup>(7)</sup>	SMCLEAR	PMLOCK <sup>(5,6)</sup>	PMCLEAR	SMEMEN	PMEMDIS	DMSEL[1:0]	
bit 7							bit 0

<b>Legend:</b>	C = Clearable bit	U = Unimplemented bit, read as '0'
R = Readable bit	W = Writable bit	'0' = Bit is cleared
-n = Value at POR	'1' = Bit is set	x = Bit is unknown

bit 15	<b>Unimplemented:</b> Read as '0'
bit 14	<b>SBLANK:</b> Blank Status bit <sup>(1,2,3,4)</sup> 1 = Pixels are in continuous Blank 0 = Pixels are not in continuous Blank
bit 13	<b>SMEMACT:</b> Secondary Memory Active bit 1 = Data display is from secondary memory 0 = Data display is not from secondary memory
bit 12	<b>PMEMACT:</b> Primary Memory Active bit 1 = Data display is from primary memory 0 = Data display is not from primary memory
bit 11	<b>TEVENTO:</b> Time Event Overflow bit 1 = This flag is set when the time event overflows 0 = Timer event does not overflow
bit 10	<b>FC2O:</b> Frame Counter 2 Overflow bit 1 = This flag is set when Frame Counter 2 overflows 0 = Frame Counter 2 does not overflow
bit 9	<b>FC1O:</b> Frame Counter 1 Overflow bit 1 = This flag is set when Frame Counter 1 overflows 0 = Frame Counter 1 does not overflow
bit 8	<b>FC0O:</b> Frame Counter 0 Overflow bit 1 = This flag is set when Frame Counter 0 overflows 0 = Frame Counter 0 does not overflow
bit 7	<b>SMLOCK:</b> Secondary Memory Lock Enable bit <sup>(7)</sup> 1 = Secondary memory is locked 0 = Secondary memory is unlocked
bit 6	<b>SMCLEAR:</b> Secondary Memory Clear Enable bit 1 = Writing a '1' to this bit clears secondary memory immediately 0 = Writing a '0' to this bit has no effect

- Note 1:** Reflects BLANKFCS[2:0] = 110 status.
- 2:** It is the user's responsibility to clear the bit to make LCD active.
- 3:** This bit is cleared by hardware when user changes Blank mode = 0 or clears the ELCDEN bit.
- 4:** This flag bit is used to generate an enhanced feature interrupt.
- 5:** This bit is effective when SMEMEN = 1; otherwise, the write follows the Write Allow bit, WA (LCDPS[4]).
- 6:** When the PMLOCK bit is set, it does not allow the user to write to the primary memory.
- 7:** When the SMLOCK bit is set, it does not allow user to write to the secondary memory.

# Liquid Crystal Display (LCD)

## Register 14-2: LCDASTAT: LCD Automatic Status Register (Continued)

bit 5	<b>PMLOCK:</b> Primary Memory Lock Enable bit <sup>(5,6)</sup> 1 = Primary memory is locked 0 = Primary memory is unlocked
bit 4	<b>PMCLEAR:</b> Primary Memory Clear Enable bit 1 = Writing a '1' to this bit clears primary memory immediately 0 = Writing a '0' to this bit has no effect
bit 3	<b>SMEMEN:</b> Secondary Memory Clear Enable bit 1 = Secondary memory is enabled 0 = Secondary memory is disabled
bit 2	<b>PMEMDIS:</b> Primary Memory Disable bit 1 = Primary memory is enabled 0 = Primary memory is disabled
bit 1-0	<b>DMSEL[1:0]:</b> Data Memory Selection bits 11 = Continues alternating selection between primary and secondary memories based on SMFCS[2:0] 10 = Alternates selection between primary and secondary memories on SMFCS[2:0] 01 = Selects secondary memory as display memory 00 = Selects primary memory as display memory

- Note 1:** Reflects BLANKFCS[2:0] = 110 status.  
**2:** It is the user's responsibility to clear the bit to make LCD active.  
**3:** This bit is cleared by hardware when user changes Blank mode = 0 or clears the ELCDEN bit.  
**4:** This flag bit is used to generate an enhanced feature interrupt.  
**5:** This bit is effective when SMEMEN = 1; otherwise, the write follows the Write Allow bit, WA (LCDPS[4]).  
**6:** When the PMLOCK bit is set, it does not allow the user to write to the primary memory.  
**7:** When the SMLOCK bit is set, it does not allow user to write to the secondary memory.

## Register 14-3: LCDFC0: LCD Frame Counter 0 Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FC0[15:8] <sup>(1,2,3)</sup>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FC0[7:0] <sup>(1,2,3)</sup>							
bit 7				bit 0			

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15-0 **FC0[15:0]:** Time Base Value bits<sup>(1,2,3)</sup>  
These bits define the overflow value.

- Note 1:** It is recommended to make the FCx values to be multiples of the frame frequency.  
**2:** FCx value must be greater than two.  
**3:** FCx register bits can only be written when Frame Counter x is disabled or ELCDEN = 0.

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**Register 14-4: LCDFC1: LCD Frame Counter 1 Register**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FC1[15:8] <sup>(1,2,3)</sup>							
bit 15							
bit 8							

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FC1[7:0] <sup>(1,2,3)</sup>							
bit 7							
bit 0							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **FC1[15:0]:** Time Base Value bits<sup>(1,2,3)</sup>  
These bits define the overflow value.

- Note 1:** It is recommended to make the FCx values to be multiples of the frame frequency.  
**2:** FCx value must be greater than two.  
**3:** FCx register bits can only be written when Frame Counter x is disabled or ELCDEN = 0.

**Register 14-5: LCDFC2: LCD Frame Counter 2 Register**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FC2[15:8] <sup>(1,2,3)</sup>							
bit 15							
bit 8							

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FC2[7:0] <sup>(1,2,3)</sup>							
bit 7							
bit 0							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **FC2[15:0]:** Time Base Value bits<sup>(1,2,3)</sup>  
These bits define the overflow value.

- Note 1:** It is recommended to make the FCx values to be multiples of the frame frequency.  
**2:** FCx value must be greater than two.  
**3:** FCx register bits can only be written when Frame Counter x is disabled or ELCDEN = 0.

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**Register 14-6: LCDTEVNT: LCD Time Event Selection Register**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TEVENT[15:8] <sup>(1,2,3)</sup>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TEVENT[7:0] <sup>(1,2,3)</sup>							
bit 7				bit 0			

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15:0      **TEVENT[15:0]:** Time Base Event Value bits<sup>(1,2,3)</sup>  
 These bits define the time event value.

- Note 1:** The TEVENTx value should be a multiple of the frame frequency.  
**2:** The TEVENTx value should be greater than the FCx value.  
**3:** The overflow is (TEVENTx \* 16 ±1); the TEVENTx overflow gets ±1 based on the TEVENT ratio with the FCx overflow.

**Register 14-7: LCDSDATAx: LCD SDATAx Register**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
S(n+15)Cy	S(n+14)Cy	S(n+13)Cy	S(n+12)Cy	S(n+11)Cy	S(n+10)Cy	S(n+9)Cy	S(n+8)Cy
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
S(n+7)Cy	S(n+6)Cy	S(n+5)Cy	S(n+4)Cy	S(n+3)Cy	S(n+2)Cy	S(n+1)Cy	S(n)Cy
bit 7				bit 0			

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15:0      **S(n+15)Cy:S(n)Cy:** Pixel Blink/Blank Enable bits (Segment x and Common y)  
If BLINKMODE[1:0] = 01 or BLANKMODE[1:0] = 01:  
 1 = Pixel is selected for Blink or Blank  
 0 = Pixel is not selected for Blink or Blank  
Else:  
**SEGxCOMy:** Pixel Data bits (Segment x and Common y)  
 1 = Pixel on (dark)  
 0 = Pixel off (clear)

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**Table 14-3: LCD SDATA Registers and Bits for Segment and COM Combinations**

COM Lines	Segments			
	0 to 15	16 to 31	32 to 47	48 to 64
0	LCDSDATA0	LCDSDATA1	LCDSDATA2	LCDSDATA3
	S00C0:S15C0	S16C0:S31C0	S32C0:S47C0	S48C0:S63C0
1	LCDSDATA4	LCDSDATA5	LCDSDATA6	LCDSDATA7
	S00C1:S15C1	S16C1:S31C1	S32C1:S47C1	S48C1:S63C1
2	LCDSDATA8	LCDSDATA9	LCDSDATA10	LCDSDATA11
	S00C2:S15C2	S16C2:S31C2	S32C2:S47C2	S48C2:S63C2
3	LCDSDATA12	LCDSDATA13	LCDSDATA14	LCDSDATA15
	S00C3:S15C3	S16C3:S31C3	S32C3:S47C3	S48C3:S63C3
4	LCDSDATA16	LCDSDATA17	LCDSDATA18	LCDSDATA19
	S00C4:S15C4	S16C4:S31C4	S32C4:S47C4	S48C4:S63C4
5	LCDSDATA20	LCDSDATA21	LCDSDATA22	LCDSDATA23
	S00C5:S15C5	S16C5:S31C5	S32C5:S47C5	S48C5:S63C5
6	LCDSDATA24	LCDSDATA25	LCDSDATA26	LCDSDATA27
	S00C6:S15C6	S16C6:S31C6	S32C6:S47C6	S48C6:S63C6
7	LCDSDATA28	LCDSDATA29	LCDSDATA30	LCDSDATA31
	S00C7:S15C7	S16C7:S31C7	S32C7:S47C7	S48C7:S63C7

# Liquid Crystal Display (LCD)

**Register 14-8: LCDREG: LCD Charge Pump Control Register**

RW-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
CPEN	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	RW-0	RW-0
—	—	—	—	—	—	CKSEL1	CKSEL0
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15

**CPEN:** 3.6V Charge Pump Enable bit

1 = The regulator generates the highest (3.6V) voltage

0 = Highest voltage in the system is supplied externally (AVDD)

bit 14-2

**Unimplemented:** Read as '0'

bit 1-0

**CLKSEL[1:0]:** Regulator Clock Select Control bits

11 = SOSC

10 = 8 MHz FRC

01 = 31 kHz LPRC

00 = Disables regulator and floats regulator voltage output

## 15.0 REGISTER MAP

**Table 15-1: Special Function Registers Associated with LCD Driver Module**

Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDCON	LCDEN	—	LCDSIDL	—	—	—	—	—	—	SLPEN	WERR	CS[1:0]		LMUX[2:0]		
LCDPS	—	—	—	—	—	—	—	—	WFT	BIASMD	LCDA	WA	LP[3:0]			
LCDREF	LCDIRE	—	LDCDCST[2:0]			VLCD3PE	VLCD2PE	VLCD1PE	LRLAP[1:0]		LRLBP[1:0]		—	LRLAT[2:0]		
LCDREG	CPEN	—	—	—	—	—	—	—	—	—	BIAS[2:0]			MODE13	CKSEL[1:0]	
LCDSEx	LCD Segment x Pin Enable Registers															
LCDDATAx	LCD Datax Registers															
LCDACTRL	SMFCS[2:0]			BLINKFCS[2:0]			BLINKMODE[1:0]		BLANKFCS[2:0]			BLANKMODE[1:0]		FCCS[1:0]		ELCDEN
LCDASTAT	—	SBLANK	SMEMACT	PMEACT	TEVENTO	FC2O	FC1O	FC0O	SMLOCK	SMCLEAR	PMLOCK	PMCLEAR	SMEMEN	PMEMDIS	DMSEL[1:0]	
LCDFCx	LCD Frame Counter x Registers															
LCDTEVNT	TEVENT[15:0]															
LCDSDATAx	LCD SDATAx Registers															
IFS6	—	—	—	—	—	—	—	—	—	—	LCDATIF	LCDIF	—	—	—	—
IEC6	—	—	—	—	—	—	—	—	—	—	LCDATIE	LCDIE	—	—	—	—
IPC25	—	—	—	—	—	—	—	—	—	LCDATIP[2:0]			—	LCDIP[2:0]		

**Legend:** — = Unimplemented bit.



# Liquid Crystal Display (LCD)

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## 16.0 RELATED DOCUMENTS

This section lists documents that are related to this section of the manual. These documents may not be written specifically for the dsPIC33 or PIC24 product families, but the concepts are pertinent and could be used with modification and possible limitations.

The current documents related to Liquid Crystal Display (LCD) are:

Title	Document #
None.	

<b>Note:</b> Please visit the Microchip website ( <a href="http://www.microchip.com">www.microchip.com</a> ) for additional Application Notes and code examples for the dsPIC33 and PIC24 families of devices.
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# dsPIC33/PIC24 Family Reference Manual

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## 17.0 REVISION HISTORY

### Revision A (December 2010)

This is the initial released revision of this document.

### Revision B (October 2013)

Corrected CS[1:0] bit information in [Register 2-1](#).

Removed MUX from [Figure 5-3](#).

Minor typographical edits throughout document.

### Revision C (February 2019)

Added [Section 14.0 “Enhanced LCD Mode”](#).

Updated [Section 2.0 “LCD Registers”](#).

Updated [Table 3-2](#) and [Table 15-1](#).

### Revision D (April 2019)

Added hyperlinks to [Section 2.0 “LCD Registers”](#).

Added note to [Section 5.1 “Internal Resistor Biasing”](#).

Added text and code example to [Section 5.3.1 “M0 \(Regulator with Boost\)”](#).

Added note to [Figure 5-4](#).

Added hyperlinks to [Section 12.0 “Configuring the LCD Module”](#).

Added note to [Register 14-3](#) through [Register 14-5](#).

Added [Section 14.4.1.2 “LCD Automation Timer Interrupt”](#).

Changes to [Table 15-1](#).

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