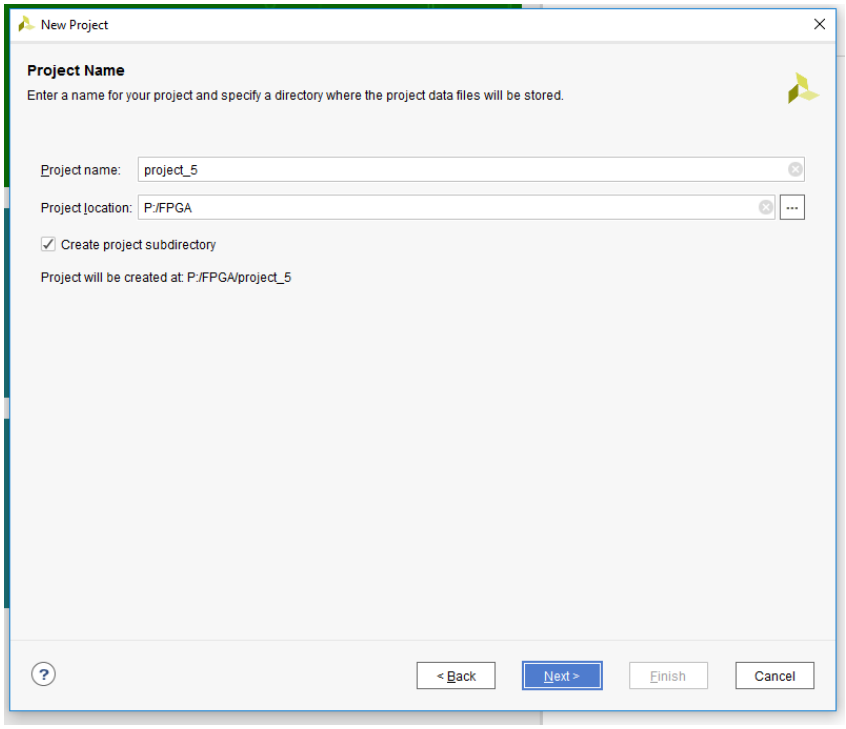
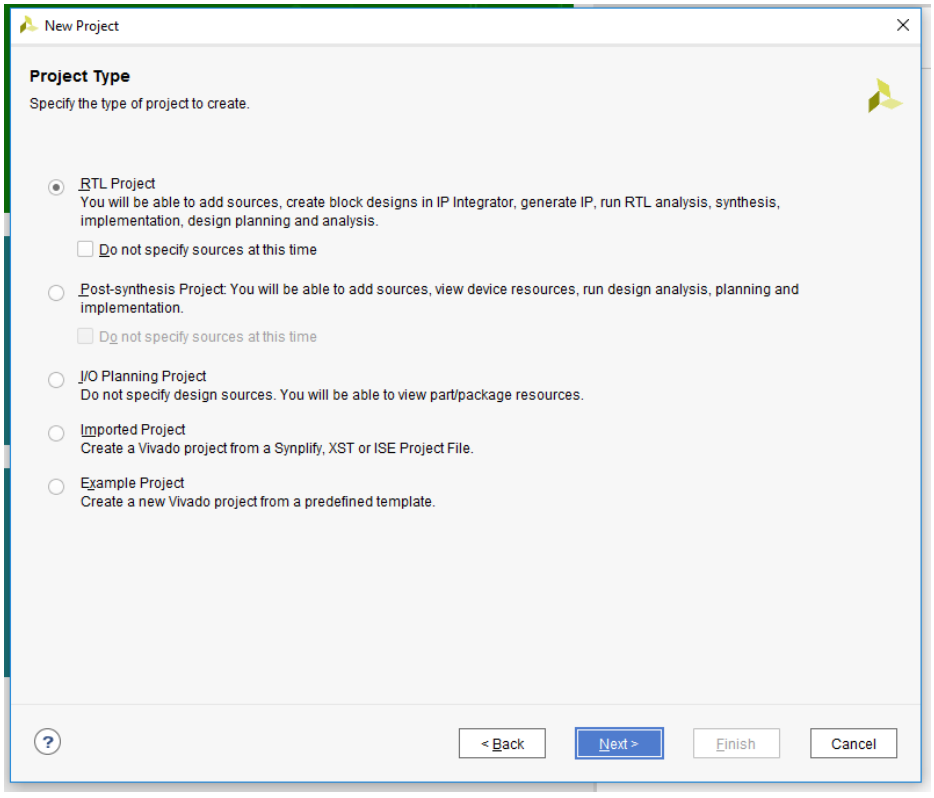
Creating Project

First thing that one needs in vivado is project. Invidividual designs are managed through them. Naming convetion should be clear so that it's easy to deduct which design particular project file is.

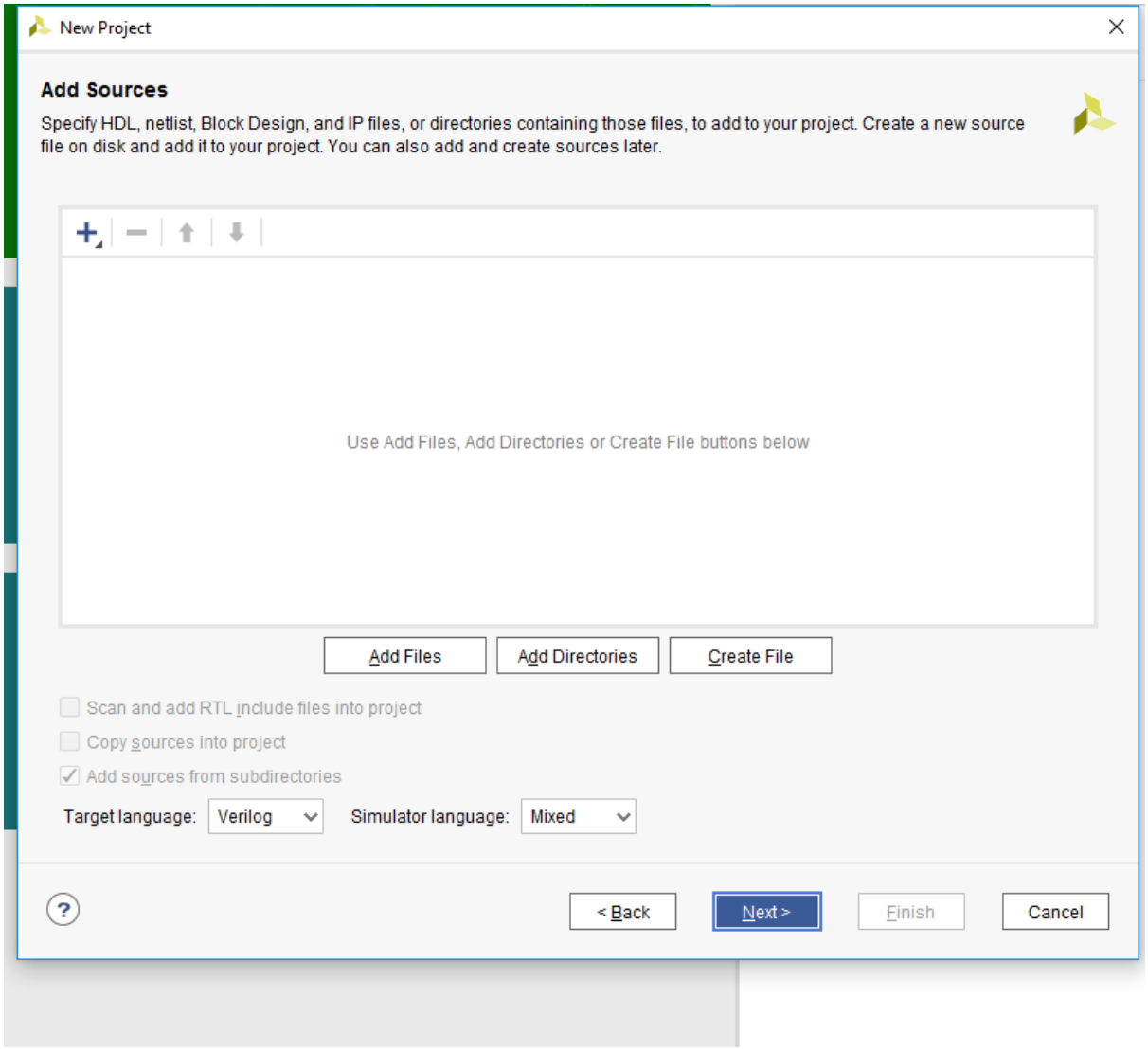


Next is project type. You need to choose RTL as in it.



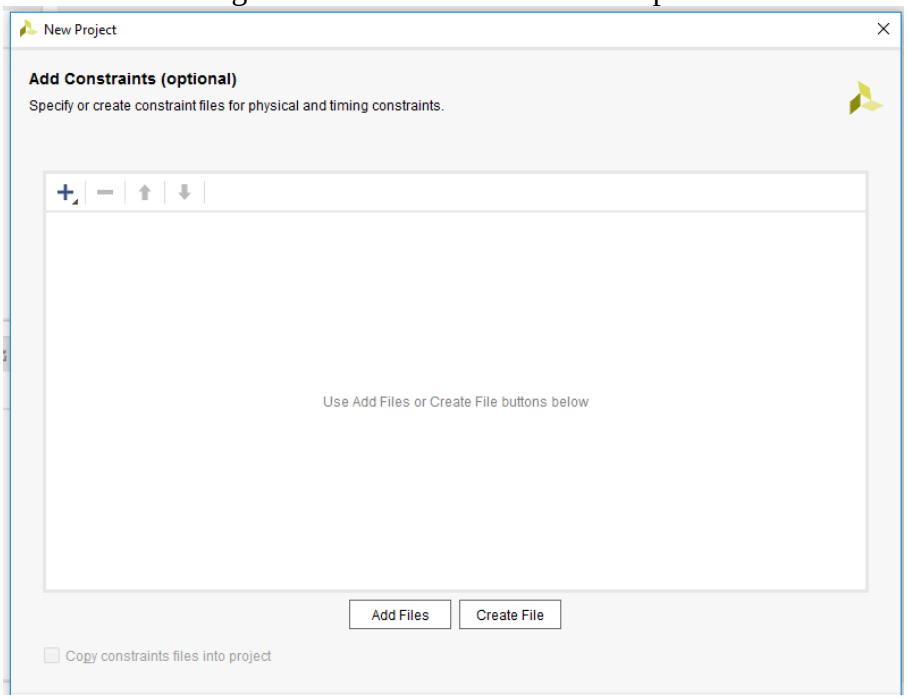
you can either add sources on the project creation or afterwards. If you wish to add them after, you can tag the "Do not Specify sources at this time to bypass 2 next pages.

In Add sources page you add the design files from the HDL designer library to the vivado project. With add files navigate to location of your HDL designer library, go to HDL subfolder and from there add all of the provided vhdl files.



If uncertain what to add, open hdl designer and check the design files from there.after source files add constraint file specified on the task description. This maps the FPGA pins to the

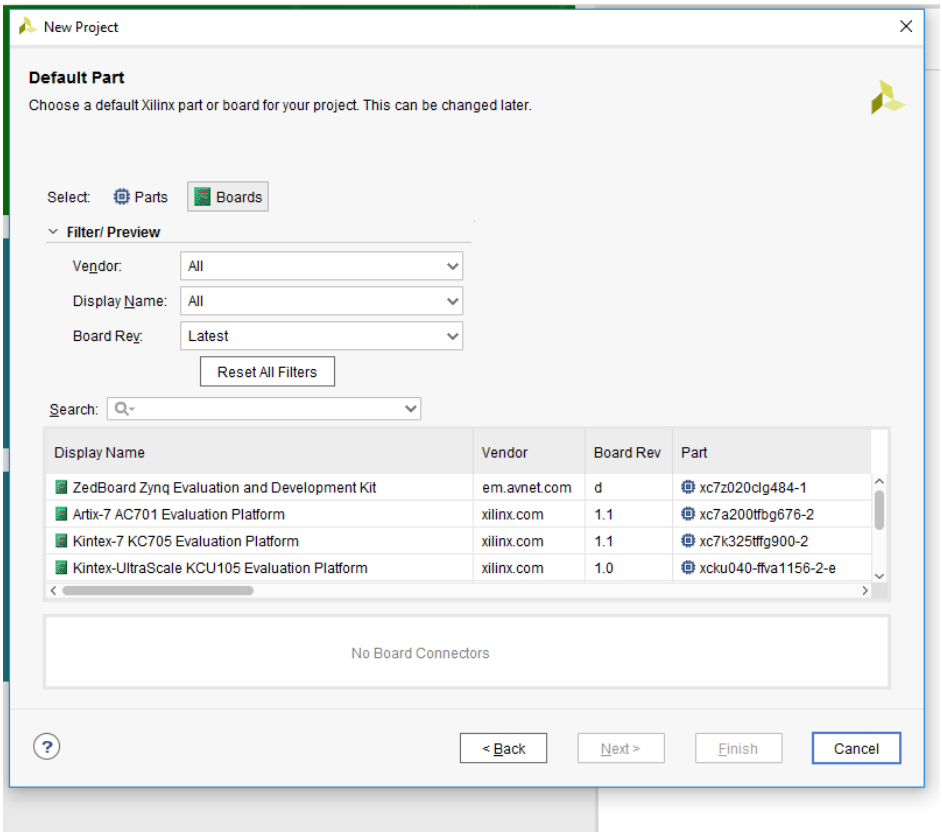
names on the design file and creates clock which operates the circuit.



Device or Target Board Selection

Copy the board definition files to Vivado project folder. Add the line described in .patch file to the project file (.xpr).

Select the PYNQ Board..



Synthesis , Implementation and Bit Stream generation

Now that the project has been configured and sources added, synthesis can start.

Synthesis

When all the files you want have been added, start the sythesis with "Run Synthesis". This will take quite while to complete. Synthesis creates gate network that can be set to the FPGA.

Implementation

When synthesis has been completed, design needs to be implemented on the board. Simply "Run Implementation". This configures the synthesized design to the physical locations on the board and maps all the ports to actual ports.

Bit stream Generate

Last part is to generate bitsream, which is started with "Generate Bitstream". This creates Programming file that contains programming instructions to program the logic on the FPGA.

Bitstream programming

Like with ex 4, you need to copy the file to sd card. the file can be found from project directory as in folder <project>/runs/impl_1/<design_top_name>.bit

You need to copy the .bit file to the sd card and rename it to “Bitstream”. Then you can boot normally and your FPGA design will be programmed during the boot sequence.