ECE 385

Spring 2020

Experiment #1

Introductory Experiment

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Intro

In this lab, we focused on learning what the components in the lab did. We also designed a circuit in order to see a “glitch” in the system. We saw that there were glitches due to gate delay and we managed to fix the glitches by adding “redundant” components in order to cover all possibilities.

Description of Circuit

The goal of our circuit was to output the logic of (B’C + AB). The design of our circuit used only 4 NAND gates. We first designed a KMAP and got this as the design (figure 1).

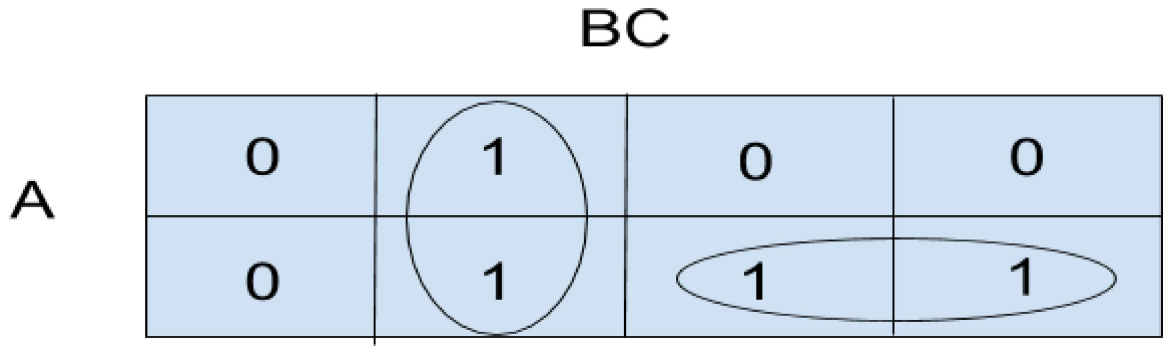

Figure 1

The purpose of this circuit was to show that a glitch would occur when the state transitioned from (ABC) 101 to 111. When it transitions, it should stay with a high output but there is a point in which the design makes the output flip to low for a very small amount of time. We controlled input ABC with switches and used both oscilloscopes and LEDs to see the changes in inputs and output.

Layout Sheet, Circuit Diagram

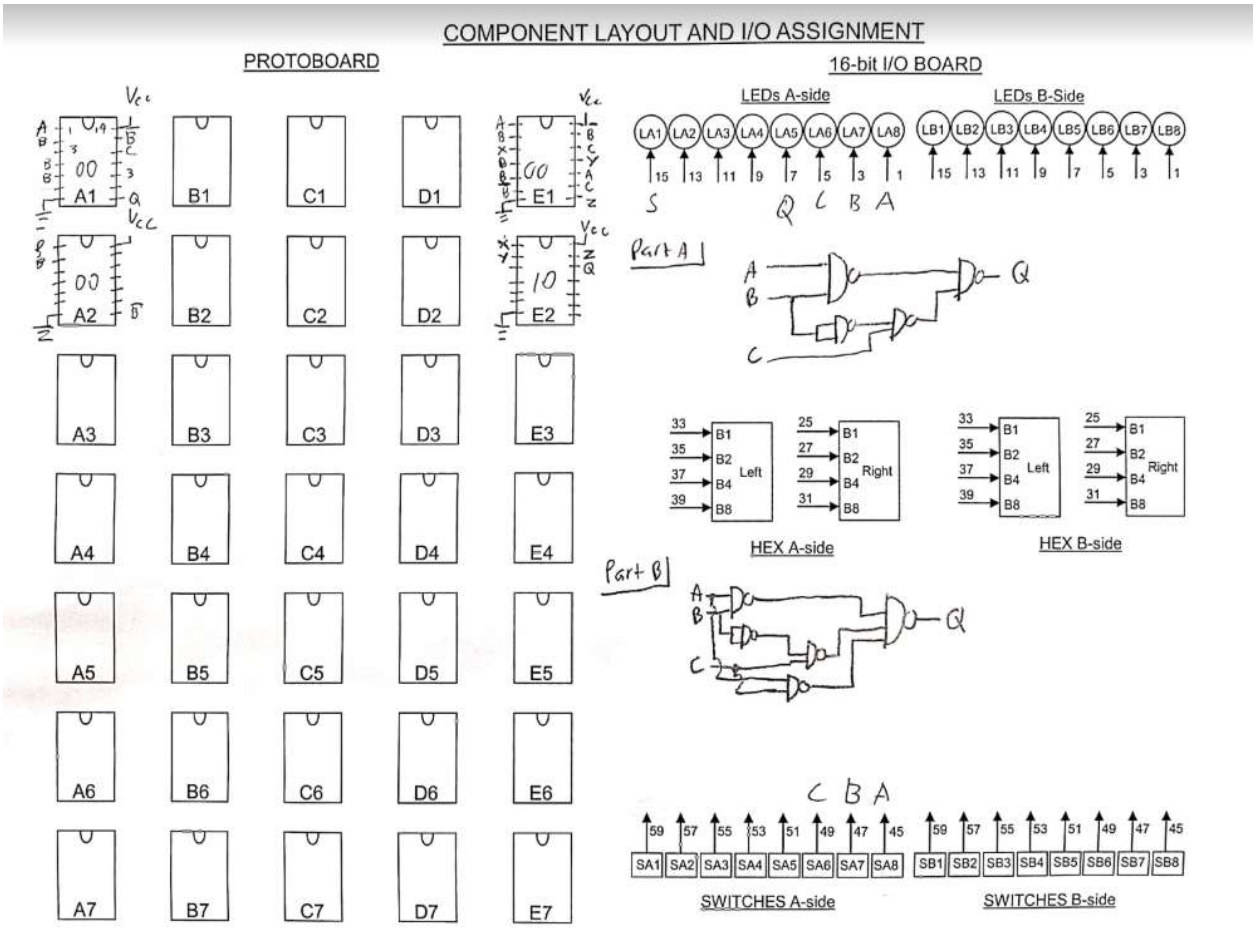

Figure 2

This image (figure 2) contains the protoboard to show which TTL chips we utilized. We also have the circuit diagram for part A and B of the lab included. The 16-bit I/O board shows which switches were used as input and which LEDs were used for output.

Documentation

Part A KMAP:

A \ BC	00	01	11	10
0	0	1	0	0
1	0	1	1	1

Q: Why might some groups not see glitches? Why does adding more inverters make the glitch appear?
A: It is possible for some groups to not see the glitch because the transition is too quick for glitch to be seen. It is possible that it is in an instant. Adding more inverters will lead to greater gate delay which can lead to the glitch becoming visible. With more inverters the oscilloscope will be able to see the glitch occur which is shown on the oscilloscope image attached (figure 3).

Figure 3

As shown in figure 3, the glitch occurs on the falling edge which is because that is the time in which the switch is changed from high to low. This is when the glitch could potentially occur. We then redesigned out circuit into the part B circuit shown on the component layout sheet (figure 2). The new KMAP for the design is as shown in figure 4.

A \ BC				
	0	1	0	0
	0	1	1	1

Figure 4

Q: Does the circuit in part B respond like the circuit in part A?
A: Yes the circuit designed in part B responds exactly like the circuit in part A because it has the same logic except there is an added redundant component.
The circuit in part A had a glitch occur on the falling edge as shown in figure 3. We then tested the circuit built in part B and the oscilloscope displayed the reading shown in figure 5.

Figure 5

This reading displays the glitch no longer existing due to the extra piece of logic. This extra NAND gate (figure 2) prevents the glitch by making sure the B input changing does not affect the output.

Post Lab

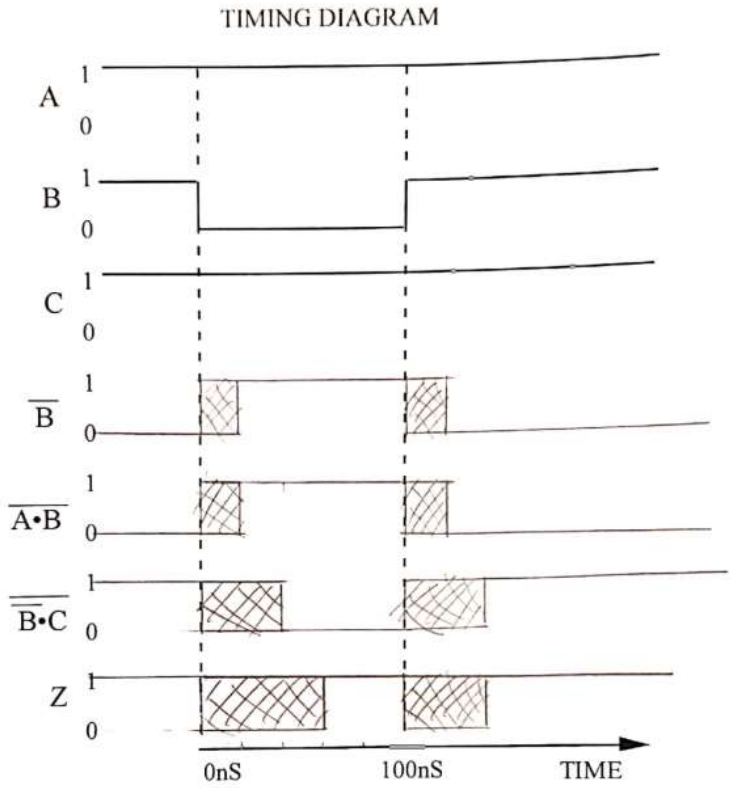

Figure 6

It takes Z a total of 60 nS to stabilize on the falling edge of B. It only takes Z a total of 40 nS to stabilize on the rising edge of B. It is possible to have glitches in Z because there are unknown values of B' , (A AND B)' , and (B' AND C)' which are all used to see the value of Z.
The debouncer given in General Guide Figure 17 is used to prevent any bouncing values between high and low when a switch is closed. It is possible for the switch itself to bounce due to the momentum of the switch closing. In order to prevent this bounce from creating a ripple in input, the main switch is grounded. There are then 2 parts the switch can connect to, A and B. The switch will connect to a single part and it is impossible for it to have the momentum to bounce to the other. This means the input will either be pulled down on one end or pulled high on the other based on where the switch is closed. That means only one output will be high and one will be low based on switch position. This is because the output of one NAND gate is connected to the input of the other which makes it so neither can be the same. There is also no gate delay due to it being only 2 NAND gates working together.

General Guide
The advantage of a larger noise immunity is that your circuit can have more noise and it will not create any bugs or glitches. The last inverter would be observed over the first because the first inverters will be the ones that limit the noise. It is possible that the noise is still too severe but the last inverter should have a solid value because the noise was removed by the previous inverters. Given VOUT and VIN, we could calculate noise immunity by seeing the input voltage and comparing it to the output voltage. We can see where the output voltage changes values

and at what point it does compared to VIN. Measuring VIN when VOUT changes would show how much noise it will take to switch the VOUT value. It is also bad practice to share resistors on two or more LEDs because it is possible for one resistor to start conducting while the others do not. That would mean it only goes down one path which is not the way we want it.

Conclusion

From this lab, I learned about the switch box and the oscilloscope. I learned how the switch box functioned and I was learning more about the oscilloscope functions. From this lab specifically I learned about static hazards and how to prevent them. I learned that gate delay can lead to a static hazard where the output bit has a glitch that makes it not the value that is expected. This can be prevented by using redundant terms in the SOP and using extra gates. The design that we created worked fine but the glitch at first did not show up. We needed to use more inverters to delay the output just enough to make the glitch truly appear. I do not think there was anything that could be done to make our circuit better due to the nature of this lab.