Logic Type Rock
MP4 CP1 Progress Report and Road Map
dbycul2, danielp7, jayhp2

Progress Report

Advanced RV32I Pipelined Design:

- Advanced Hardware Prefetching:
  - Design (dbycul2 & danielp7): For CP3, we implemented an advanced hardware prefetcher that took the stride based on the differences in addresses of load instructions. We connected the prefetcher between the cache and arbiter in order to make sure it was able to assist with prefetching instructions.
  - Verification (dbycul2 & danielp7): We used the prefetching design we had created along with the textbook to help us formulate our plan. We then traced through the pipeline and waveform to make sure everything was correct and functioning.
- Eviction Writeback Buffer:
  - Design (danielp7): We used logic similar to the prefetcher for this except we focused on data. We would evict dirty data from the cache and we would place this eviction writeback buffer between the arbiter and cache to make sure there were faster accesses.
  - Verification (danielp7 & dbycul2): We traced through the pipeline to make sure the values were correct and used the waveform to make sure our finalized values were correct. Similarly to the prefetching design we used the premade designs to make sure that we had the correct logic.
- Memory stage leapfrogging:
  - Design (jayhp2): TBD
  - Verification (All): TBD

Road Map

1. Get the design up and running with the competition code to make sure it works properly. (Implementation and Verification =all)
2. Presentation will be done and it will follow the guidelines provided (Implementation and Verification =all)
3. The final report will be a culmination of our work in a condensed, more readable and technical format following basic guidelines. (Implementation and Verification =all)